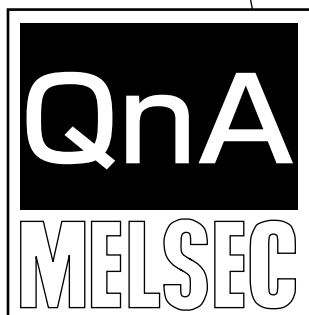


MITSUBISHI

QnA SERIES

Q2ACPU(S1)/Q3ACPU/Q4ACPU

User's Manual



Mitsubishi Programmable Controller

● SAFETY PRECAUTIONS ●

(Be sure to read these instructions before use.)

Before using the product, read this and relevant manuals carefully and handle the product correctly with full attention to safety.

In this manual, ●SAFETY PRECAUTIONS● are classified into 2 levels: "DANGER" and "CAUTION".



Indicates that incorrect handling may cause hazardous conditions, resulting in death or severe injury.



Indicates that incorrect handling may cause hazardous conditions, resulting in minor or moderate injury and/or property damage.

Under some circumstances, failure to observe the ⚠ CAUTION level instructions may also lead to serious results.

Be sure to observe the instructions of both levels to ensure the safety.

Please keep this manual in a safe place for future reference and also pass this manual on to the end user.

[DESIGN PRECAUTIONS]

⚠ DANGER

- Create a safety circuit outside the PLC to ensure the whole system will operate safely even if an external power failure or a PLC failure occurs. Otherwise, incorrect output or malfunction may cause an accident.
 - (1) For an emergency stop circuit, protection circuit and interlock circuit that is designed for incompatible actions such as forward/reverse rotation or for damage prevention such as the upper/lower limit setting in positioning, any of them must be created outside the PLC.
 - (2) When the PLC detects the following error conditions, it stops the operation and turn off all the outputs.
 - The overcurrent protection device or overvoltage protection device of the power supply module is activated.
 - The PLC CPU detects an error such as a watchdog timer error by the self-diagnostics function.In the case of an error of a part such as an I/O control part that cannot be detected by the PLC CPU, all the outputs may turn on. In order to make all machines operate safely in such a case, set up a fail-safe circuit or a specific mechanism outside the PLC. For fail-safe circuit example, refer to "LOADING AND INSTALLATION" of this manual.
 - (3) Depending on the failure of the output module's relay or transistor, the output status may remain ON or OFF incorrectly. For output signals that may lead to a serious accident, create an external monitoring circuit.

[DESIGN PRECAUTIONS]



DANGER

- If load current more than the rating or overcurrent due to a short circuit in the load has flowed in the output module for a long time, it may cause a fire and smoke. Provide an external safety device such as a fuse.
- Design a circuit so that the external power will be supplied after power-up of the PLC.
Activating the external power supply prior to the PLC may result in an accident due to incorrect output or malfunction.
- For the operation status of each station at a communication error in data link, refer to the respective data link manual.
Otherwise, incorrect output or malfunction may cause an accident.
- When controlling a running PLC (data modification) by connecting a peripheral device to the CPU module or a PC to a special function module, create an interlock circuit on sequence programs so that the whole system functions safely all the time.
Also, before performing any other controls (e.g. program modification, operating status change (status control)), read the manual carefully and ensure the safety.
In these controls, especially the one from an external device to a PLC in a remote location, some PLC side problem may not be resolved immediately due to failure of data communications.
To prevent this, create an interlock circuit on sequence programs and establish corrective procedures for communication failure between the external device and the PLC CPU.
- When setting up the system, do not allow any empty slot on the base unit.
If any slot is left empty, be sure to use a blank cover (AG60) or a dummy module (AG62) for it.
When using the extension base unit, A52B, A55B or A58B, attach the included dustproof cover to the module in slot 0.
Otherwise, internal parts of the module may be flied in the short circuit test or when an overcurrent or overvoltage is accidentally applied to the external I/O section.

[DESIGN PRECAUTIONS]

CAUTION

- Do not install the control lines or communication cables together with the main circuit or power lines, or bring them close to each other.
Keep a distance of 100mm (3.94inch) or more between them.
Failure to do so may cause malfunctions due to noise.
- If having read register R outside the allowable range with the MOV instruction, the file register data will be FFFFH. Using this as it is may cause malfunctions. Pay attention not to use any out-of-range file register when designing sequence programs. For instruction details, refer to the programming manual.
- When an output module is used to control the lamp load, heater, solenoid valve, etc., a large current (ten times larger than the normal one) may flow at the time that the output status changes from OFF to ON. Take some preventive measures such as replacing the module with the one of a suitable current rating.

[INSTALLATION PRECAUTIONS]

CAUTION

- Use the PLC under the environment specified in the user's manual.
Otherwise, it may cause electric shocks, fires, malfunctions, product deterioration or damage.
- Insert the module fixing projection into the fixing hole in the base unit to mount the module.
Incorrect mounting may cause malfunctions, a failure or a drop of the module.
In an environment of frequent vibrations, secure the module with the screw.
Tighten the screw within the specified torque range.
If the screw is too loose, it may cause a drop of the module, a short circuit or malfunctions.
Tightening the screw excessively may damage the screw and/or the module, resulting in a drop of the module, a short circuit or malfunctions.
- Connect the extension cable to the connector of the base unit or module.
Check for incomplete connection after installing it.
Poor electrical contact may cause incorrect inputs and/or outputs.
- Insert the memory card and fully press it to the memory card connector.
Check for incomplete connection after installing it.
Poor electrical contact may cause malfunctions.
- Be sure to shut off all phases of the external power supply used by the system before mounting or removing the module.
Failure to do so may damage the module.
- Do not directly touch the conductive part or electronic components of the module.
Doing so may cause malfunctions or a failure of the module.

[WIRING PRECAUTIONS]



DANGER

- Be sure to shut off all phases of the external power supply used by the system before wiring.
Failure to do so may result in an electric shock or damage of the product.
- Before energizing and operating the system after wiring, be sure to attach the terminal cover supplied with the product.
Failure to do so may cause an electric shock.



CAUTION

- Ground the FG and LG terminals correctly.
Failure to do so may cause an electric shock or malfunctions.
- Wire the module correctly after confirming the rated voltage and terminal layout.
Connecting a power supply of a different voltage rating or incorrect wiring may cause a fire or failure.
- Do not connect multiple power supply modules to one module in parallel.
The power supply modules may be heated, resulting in a fire or failure.
- Press, crimp or properly solder the connector for external connection with the specified tool.
Incomplete connection may cause a short circuit, fire or malfunctions.
- Tighten terminal screws within the specified torque range.
If the screw is too loose, it may cause a short circuit, fire or malfunctions.
If too tight, it may damage the screw and/or the module, resulting in a short circuit or malfunctions.
- Carefully prevent foreign matter such as dust or wire chips from entering the module.
Failure to do so may cause a fire, failure or malfunctions.
- Install our PLC in a control panel for use.
Wire the main power supply to the power supply module installed in a control panel through a distribution terminal block.
Furthermore, the wiring and replacement of a power supply module have to be performed by a maintenance worker who acquainted with shock protection.
(For the wiring methods, refer to Section 19.7.)

[STARTUP AND MAINTENANCE PRECAUTIONS]



DANGER

- Do not touch any terminal during power distribution.
Doing so may cause an electric shock.

- Properly connect batteries.
Do not charge, disassemble, heat or throw them into the fire and do not make them short-circuited and soldered.
Incorrect battery handling may cause personal injuries or a fire due to exothermic heat, burst and/or ignition.

- Be sure to shut off all phases of the external power supply used by the system before cleaning or retightening the terminal screws or module mounting screws.
Failure to do so may result in an electric shock.
If they are too loose, it may cause a short circuit or malfunctions.
Tightening the screw excessively may damage the screw and/or the module, resulting in a drop of the module, a short circuit or malfunctions.

[STARTUP AND MAINTENANCE PRECAUTIONS]

CAUTION

- When performing online operations (especially, program modification, forced output or operating status change) by connecting a peripheral device to the running CPU module, read the manual carefully and ensure the safety.
Incorrect operation will cause mechanical damage or accidents.
- Do not disassemble or modify each of modules.
Doing so may cause failure, malfunctions, personal injuries and/or a fire.
- When using a wireless communication device such as a mobile phone, keep a distance of 25cm (9.84inch) or more from the PLC in all directions.
Failure to do so may cause malfunctions.
- Be sure to shut off all phases of the external power supply used by the system before mounting or removing the module.
Failure to do so may result in failure or malfunctions of the module.
- When replacing the fuse, use a fuse specified by the manufacturer.
Using the one for the high-rated current or an electric wire may cause a fire.
- Do not drop or apply any impact to the battery.
Doing so may damage the battery, resulting in electrolyte spillage inside the battery.
If any impact has been applied, discard the battery and never use it.
- Before handling modules, touch a grounded metal object to discharge the static electricity from the human body.
Failure to do so may cause failure or malfunctions of the module.

[DISPOSAL PRECAUTIONS]

CAUTION

- When disposing of the product, treat it as an industrial waste.

[TRANSPORTATION PRECAUTIONS]

CAUTION

- When transporting lithium batteries, make sure to treat them based on the transportation regulations.
(Refer to Appendix 10 for details of the relevant models.)

REVISIONS

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Japanese Manual Version SH-3532-H

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Introduction

Thank you for purchasing the Mitsubishi programmable logic controller MELSEC-QnA series.

Before using your new PLC, please read this manual thoroughly to gain an understanding of its functions so that you can use it properly.

Please forward a copy of this manual to the end user.

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APPENDIX 10 TRANSPORTATION PRECAUTIONS	App - 190
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About This Manual

The following manuals are related to this product.
Please order those you require.

Related Manuals

Manual Name	Manual No. (Model Code)
QnACPU Programming Manual (Fundamentals) Explains the programming procedures, device names and program types required for program creation. (Sold separately)	IB-66614 (13JF46)
QCPU (Q mode)/QnACPU Programming Manual (Common Instructions) Explains how to use the sequence instructions, basic instructions and application instructions. (Sold separately)	SH-080039 (13JF58)
QnACPU Programming Manual (Special Function Module) Explains the dedicated instructions used with special function modules. (Sold separately)	SH-4013 (13JF56)
QnACPU Programming Manual (AD57 Instructions) Explains the dedicated instructions for controlling an AD57 (S1) type CRT controller module. (Sold separately)	IB-66617 (13JF49)
QCPU (Q mode)/QnACPU Programming Manual (PID Control Instructions) Explains the dedicated instructions to execute PID control. (Sold separately)	SH-080040 (13JF59)
QCPU (Q mode)/QnACPU Programming module (SFC) Explains MELSAP3 system configuration, performance specifications, functions, programming, debugging and error codes. (Sold separately)	SH-080041 (13JF60)
Building Block Type I/O Module User's Manual Explains the specifications of building block type I/O modules. (Sold separately)	IB-66140 (13J643)
MELSECNET/10 Network System (for QnA/Q4AR) Reference Manual Describes the general concept, specifications, and part names and settings, for MELSECNET/10. (Sold separately)	IB-66690 (13JF78)
MELSECNET, MELSECNET/B Data Link System Reference Manual Explains overviews, specifications, part names, and settings of MELSECNET (II) and MELSECNET/B. (Sold separately)	IB-66350 (13JF70)
GX Developer Version 8 Operating Manual Explains the methods of programming, print out, monitoring, and debugging of Developer. (Sold separately)	SH-080373E (13JU41)
SW2IVD-GPPQ GPP Software package Operating Manual (Offline) Explains offline functions such as the methods of programming, print out and file maintenance of SW2IVD-GPPQ. (Included with product)	IB-66774 (13J921)
SW2IVD-GPPQ GPP Software package Operating Manual (Online) Explains online functions such as methods of monitoring and debugging of SW2IVD-GPPQ. (Included with product)	IB-66775 (13J922)
Type SW2IVD-GPPQ GPP Software package Operating Manual (SFC) Describes MELSAP-3 system components, performance specifications, functions, system start-up procedure, SFC program editing method, monitoring method, printout method and error messages. (Included with product)	IB-66776 (13J923)

Manual Name	Manual No. (Model Code)
Type SW2IVD-GPPQ GPP Software package Operating Manual (Q6TEL) Describes Q6TEL system configuration, operating methods, etc. (Included with product)	IB-66777 (13J924)

User Precautions

Precautions when using QnACPU

When using a CPU module, format the memory using a peripheral device.

For details of memory format, refer to the following manuals.

- GX Developer Operating Manual
- SW□IVD-GPPQ Software package Operating Manual (Online)

Precautions for Battery

- (1) The operation after removal of a battery
After removing a battery of the CPU module, format the memory using a peripheral device to start next operation. (Refer to Section 21.5)
- (2) The operation after excess of a battery life
After removing a battery of the CPU module due to its excess life, format the memory using a peripheral device to start next operation. (Refer to Section 21.6)

1 ABOUT THIS MANUAL

1.1 About this Manual

This manual serves to explain the specifications and functions of the Q2ACPU(S1), Q3ACPU, and Q4ACPU (abbreviated as QnACPU hereafter), the specifications of other modules, and the maintenance required for smooth system operation, to users of MELSEC-QnA series programmable controllers.

It is divided into the following three main parts:

- (1) Sections 2 and 3 These sections give the general description and system configuration for the QnACPU.
Read them to learn the features of QnACPU, and the modules that can be used and points to note when configuring a system.
- (2) Sections 4 to 15 These sections give the specifications and functions of QnACPU.
They describe each QnACPU function to enable you to use the QnACPU effectively.
- (3) Sections 16 to 18 These sections describe the specifications and handling of units/modules other than the CPU module (power supply module, base units, etc.).
Read them to learn how to handle the power supply module, base units, memory cards, etc.
- (4) Sections 19 to 20 These sections describe the loading and installation, EMC and low voltage directives.
- (5) Sections 21 to 22 These sections describe all aspects of maintenance, from installing the QnACPU to daily inspections and troubleshooting.
Read them to learn how to install the QnACPU so as to ensure smooth operation, and how to carry out daily inspections and corrective action in the event of trouble.

REMARK

This manual does not cover MELSECNET(II) data link systems, MELSECNET/B data link systems, MELSECNET/10 networks, or the SFC function.

For details on each function, refer to the following manuals.

- MELSECNET(II), MELSECNET/B Data Link
MELSECNET, MELSECNET/B Data Link System Reference Manual
- MELSECNET/10 Network
MELSECNET/10 Network System Manual for QnA/Q4AR
- SFC Function
QCPU (Q Mode)/QnACPU Programming Manual (SFC)

1.2 Abbreviations and Generic Terms Used in this Manual

The following abbreviations and generic terms are used in this manual.

(1) QnACPU.....	Abbreviation for Q2ACPU, Q2ACPU-S1, Q3ACPU, and Q4ACPU type CPU modules.
(2) Network module.....	Abbreviation of AJ71QLP21(G), AJ71QLP21S, AJ71QLR21, AJ72QLP25 (G), AJ71QBR11, AJ72QBR15 and AJ72QLR25 type MELSECNET/10 network modules.
(3) Ethernet module.....	Abbreviation of AJ71QE71N-B2 and AJ71QE71N-B5T type Ethernet interface modules.
(4) Serial communication module....	Abbreviation of AJ71QC24 (N), AJ71QC24 (N)-R2 type serial communication module.
(5) CC-Link.....	Abbreviation of Control & Communication Link
(6) GPP function.....	Abbreviations for the SW□IVD-GPPQ type GPP function software package, GX Developer.
(7) Personal computer.....	IBM's PC/AT or completely compatible computers.
(8) Peripheral device capable of GPP functions	Generic term for a peripheral device capable of running the GPP function software, for example an IBM PC/AT.
(9) Q6PU.....	Abbreviation for Q6PU programming unit.
(10) Peripheral device.....	Generic term for a device that is connected to a QnACPU and can be used to operate it, for example a IBM-PC/AT-compatible personal computer or Q6PU.
(11) Built-in RAM.....	A RAM incorporated in the QnA CPU that stores sequence programs and other data.
(12) Memory card.....	Abbreviation for Q1MEM-□□□ type memory card
(13) ACPU.....	Generic term for a MELSEC-A series programmable controller

2 OVERVIEW

2.1 Features

QnACPU has the following features.

- (1) Large memory capacity
 - (a) Q4ACPU has a program capacity of 124k steps, which means that 124k steps can be used for a single program (Q2ACPU: 28k steps, Q2ACPU-S1: 60k steps, Q3ACPU: 92k steps).
 - (b) The device memory capacity is 32k words and the user can change the number of points as required.
For example, the default number of points for internal relays (M) is 8k points, but this can be expanded up to 32k points.
 - (c) Two memory cards of a maximum of 2M bytes can be installed.
Memory cards are used to store programs, comments, statements, and file registers.
(Programs can be stored in the CPU module itself, so a memory card is not essential to run a CPU module.)
- (2) High-speed processing
 - (a) Higher operation processing speeds have been achieved for basic instructions and application instructions.

	A4UCPU	Q4ACPU
Basic instruction	0.15 μ s	→ 0.075 μ s
Application instruction	0.90 μ s	→ 0.225 μ s
 - (b) The access time for expansion data memory (file registers: R) has been conformed with the internal devices of the QnACPU (data registers: D, and link registers: W).
 - (c) Reading/writing of the buffer memories of special function modules dedicated to QnA (serial communication modules) have been realised processing speed-up by six times compared to AnUCPU.
(The processing speed of the existing special function modules for ACPU use is about the same as that when using AnUCPU.)
 - (d) A high-speed access base unit (A38HB/A38HBEU) is available to speed up the processing time for accessing special function modules such as network modules and serial communication modules that handle large quantities of data. Simply by mounting the special function module on the high-speed access base unit, the access processing speed is increased when the QnACPU accesses the special function module.

- (3) Selection of program execution type that is appropriate for the control has been realised.

There are four program execution types to be selected as follows.

- (a) Initial execution type

This program type is executed once only when the QnACPU is set to RUN.

- (b) Scan execution type

This program type is run continually while the QnACPU is in the RUN status.

This is equivalent to a conventional program that runs from step 0 to END instruction. It is possible to create subroutine programs and interrupt programs for this type of program.

- (c) Low-speed execution type

This is a program type which is executed only during the surplus constant scan time (process to preset the program execution time for constant scan time) or during the set execution time of the low-speed execution program.

- (d) Stand-by type

This type of program consists entirely of a subroutine program or interrupt program.

- (4) The SFC language MELSAP3 has been supplied.

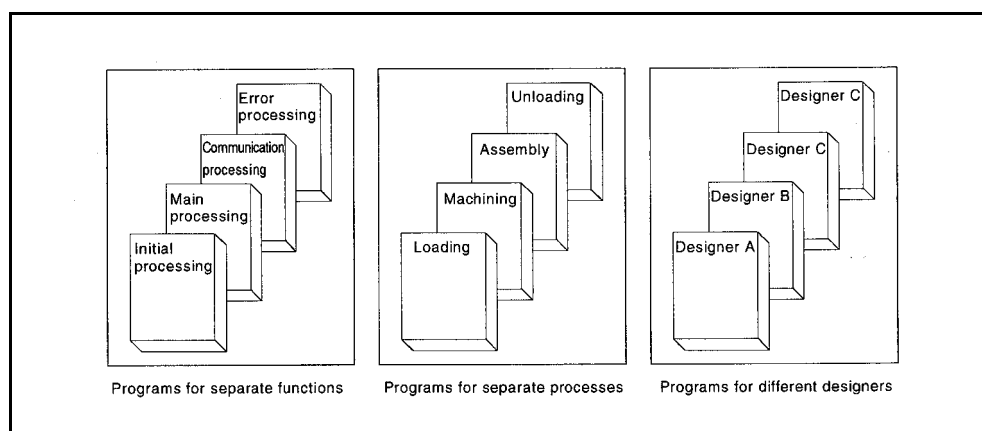
With enhancement of step attributes and SFC control instructions, MELSAP3 makes SFC programming even easier.

- (5) A software development environment that improves program productivity has been realized.

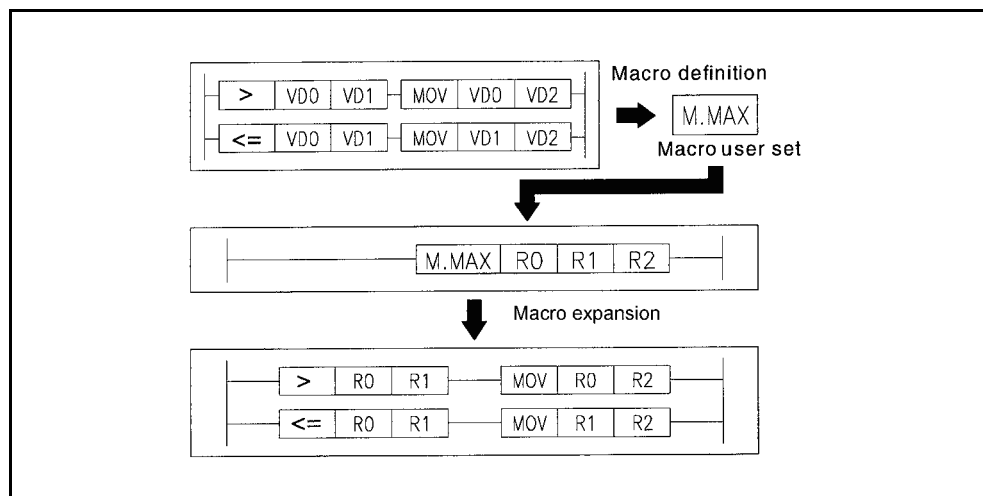
- (a) In order to enable the design of structured programs, a file format has been adopted for programs.

What would conventionally have been a single continuous program can now be handled in a structured way as a number of files.

This allows for design work to be shared by several designers, and allows management of programs in accordance with functions, processes, or designers, etc.



- (b) The user can standardize and simplify programs by creating and using macro instructions corresponding to functions.



- (c) Devices can be used without restrictions.
- 1) Word device bit operations are possible.
 - 2) Differential contacts can be used.
 - 3) Buffer memories of special function modules can be accessed directly from a program as devices.
 - 4) The link data of network modules can be accessed directly from a program as devices.
- (d) Ease of operation for GPP function program editing has been improved.
- 1) Up to four programs, data, etc., can be edited simultaneously.
Programs and data can be cut and pasted between edited objects.
 - 2) Ladder editing is possible while the ladder is displayed with comments.
 - 3) Familiar operations can be performed with pull-down menus and dialog boxes.
- (e) The debugging function at start-up has been perfected.
- 1) Ladder modification while performing monitoring is possible.
 - 2) Coil ON/OFF causes can be searched for.
 - 3) The timing for monitoring can be set using a step number or device status, allowing debugging to be conducted under the optimum conditions.
 - 4) Devices for which index qualifications have been set can be monitored.
- (f) The GPP function document creation function has been strengthened.
- 1) Since comments can now comprise 32 characters, they can be more detailed than before.
 - 2) Comments can now be set for all devices.
 - 3) The statements and notes appended to programs can now be managed as an integral part of the program, which makes program modifications and utilization easier.
 - 4) Printout data can be saved in a file.

- (g) A powerful array of support software packages is available for program creation.
 - 1) Data conversion package
Comment data, device data, etc., which is created with spreadsheet software and text editors available on the market, can be converted to files for GPP function use.
Conversely, files created for GPP function use can be converted to data for spreadsheets or text editors.
 - 2) Macro/library package
The basic programs for accessing special function modules, and standard programs for error detection, alarm processing, etc., have been brought together as a package of macro and library data.
 - 3) Ladder sequence linking package
This package is used to link multiple programs to make a single program.
This has an automatic allocation function that ensures that devices from each program without duplicating in the created program.
 - 4) CAD interface program
This package is used to handle sequence ladders, instruction lists, comment data and SFC diagrams as CAD data and communicate these data to CAD systems.

2.2 Additional Functions of QnACPU

New functions and instructions for special function module are added to the QnACPU.

[Additional functions]

- Variety of local devices..... Refer to Section 2.2.1 (1).
 Monitor test of local device..... Refer to Section 8.2.2.
 Use of local device at the subroutine/interrupt
 program storage destination..... Refer to Appendix 7.
- Auto refresh setting of CC-Link..... Refer to Section 2.2.1 (2),
 Section 7.2.
- MELSECNET/10 relay communication from the
 Ethernet module (Network relay)..... Refer to Section 2.2.1 (3),
 Appendix 8.
- Addition of AJ71QC24N-compatible commands Section 2.2.1 (4)

[Added instructions for special function module]

The following instructions have been added for function version "B" of the QnACPU:

- AJ61QBT11 control instructions..... 13
- AD75 control instructions..... 19
- AJ71D□-R4 control instructions..... 12
- AJ71QE71 control instructions..... 10

Additional function/special function module instructions can be used for the QnACPU described function version B in the date column of the rating plate.

Check that function version B is described on the QnACPU rating plate before using the additional function/special function module instructions.

If your QnACPU does not have indication of function version B, skip this item and the description of additional functions.



Date of manufacture

Function version

When using additional function/special function module instructions of the QnACPU, it is necessary to match the GPP function model and the function version/version of the applicable special function module. (Refer to Table 2.1.)

Table 2.1 List of combination between QnACPU and function version/version of special function module

Module/package Name		QnACPU	SW01VD- GPPQ SW11VD- GPPQ	SW21VD- GPPQ	AJ71QE71 (B2), (B5)	AD75P-S3	AJ71 ID□-R4	AJ61QBT11	AJ71QC24 (N)(R2)
Condition	Function version	9707B and later	—	—	9707B and later	—	—	9707B and later	—
	Version	—	No restriction	No restriction	—	No restriction	BC and later	—	No restriction
Local device monitor test		○	×	○	—	—	—	—	—
Local device switching of subroutine/interrupt program		○	—		—	—	—	—	—
Auto refresh function of CC-Link		○	×	○	—	—	—	○	—
AJ61QBT11 control instructions		○	○		—	—	—	○	—
MELSECNET/10 relay communication from Ethernet		○	×	△	○	—	—	—	—
AJ71QE71 control instructions		○	○		○	—	—	—	—
AD75 control instructions		○	○	○	—	○	—	—	—
ID interface module instructions		○	○		—	—	○	—	—
Compatibility with AJ71QC24N commands		○	—		—	—	—	—	○

REMARK

- 1) Marks ○, —, △ and × in Table 2.1 indicate as follows:
 - : Essential for use of function and instruction
 - : Irrelevant to function and instruction
 - △: Required in the case of access to the QnACPU in other stations from the peripheral device via Ethernet
 - ×: Not available on peripheral devices.
- 2) GX Developer complies with functions of function version B.

2.2.1 Overview of added functions

This section shows an overview of the added functions.

- (1) Variety of local device
 - (a) The device set as the local device at "Device" in Parameter can be monitored and tested with a peripheral device.

This function allows checking and debug of the local device in the program monitored with a peripheral device.
 - (b) The local device of the file where the subroutine program/interrupt program is stored has made it possible to be used during execution of the subroutine program/interrupt program.

For this function, even if an operation using the local device of the subroutine program is carried out, the original local device cannot be overwritten. In addition, even if an operation using the local device of the interrupt program, the local device which is executed before starting up the interrupt program cannot be overwritten.
 - (c) The following GPP function software packages are required to perform the monitor test of the local device:
 - Personal computer
 - GX Developer, SW2IVD-GPPQ type GPP function software package
- (2) Auto refresh setting of CC-Link
 - (a) When setting auto refresh of the CC-Link on the peripheral function, cyclic communication with other stations connected to the CC-Link can be automatically performed according to the set auto refresh data.
 - Remote I/O station (Communication in ON/OFF data)
 - Remote device station (Communication in ON/OFF data and Word data)
 - Intelligent device station (Communication in ON/OFF data and Word data)
 - Local station/master station (Communication in ON/OFF data and Word data)

The auto refresh setting of the CC-Link allows communication with other stations using the FROM/TO instruction without communicating with the master station of the CC-Link.
 - (b) Auto refresh is available for up to 8 CC-Link modules for each unit of QnACPU. Communication for 9th CC-Link module and more can be performed with the CC-Link module using the FROM/TO instruction.
 - (c) The following GPP function software packages are required to perform the auto refresh setting of the CC-Link:
 - Personal computer:

GX Developer, SW2IVD-GPPQ type GPP function software package

It is necessary to upgrade the master station•local station module of CC-Link to function version B or later.

- (3) Network relay from Ethernet module
 - (a) In the network system with mixture of Ethernet and MELSECNET/10, data can be communicated with the QnACPU of other stations via multiple Ethernets or MELSECNET/10 modules.
 - (b) For the network relay from the Ethernet module, the function version of the Ethernet module should be upgraded to "B" or later.
- (4) AJ71QC24N-compatible commands are possible.
 - (a) The following AJ71QC24N commands are available:
 - Multiple blocks batch read: Command "0406"
 - Multiple blocks batch write: Command "1406"
 - (b) Multiple blocks batch read/batch write is available with AJ71QC24N (-R2, R4). Multiple blocks batch read/batch write is not available with AJ71QC24 (-R2, R4). For commands of multiple blocks batch read/batch write, refer to the following manual:
 - Corresponding Additional Explanation for AJ71QC24N (-R2/R4)

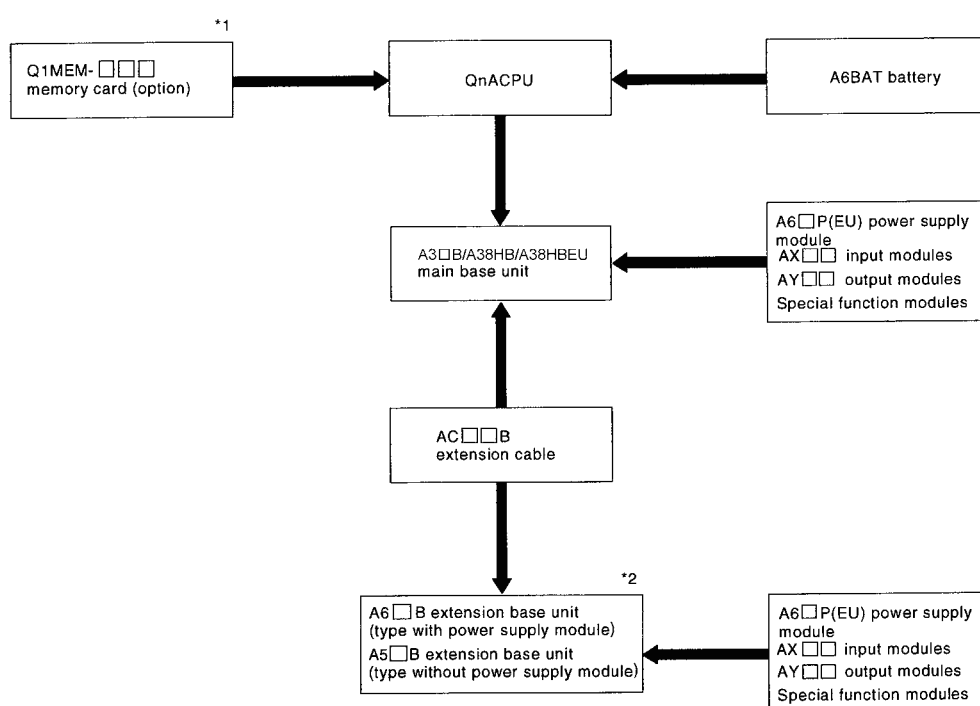
3 SYSTEM CONFIGURATION

This section describes the system configurations that can be used for a system centered on a QnACPU, cautions on configuring the system, and the system equipment.

3.1 System Configuration

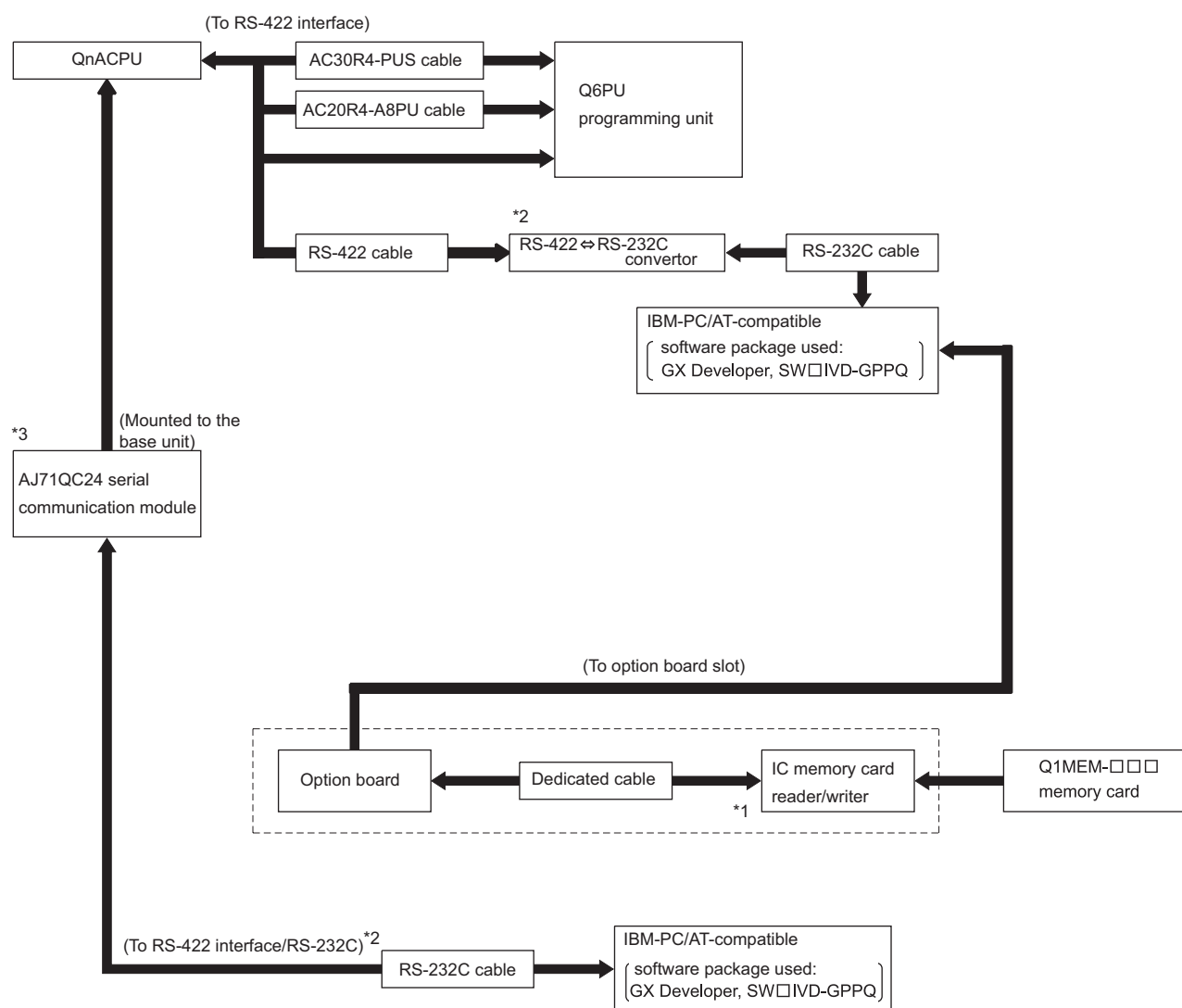
The following shows the configuration of equipment and peripheral device when a QnACPU is used in a stand-alone system.

3.1.1 Equipment configuration in a stand-alone system



POINT
*1 Up to two memory cards can be installed, if required. SRAM and E²PROM memory cards allow file read/write when mounted on the CPU module. *2 When using an A5□B extension base unit, pay particular attention to the power supply capacity of the main base unit. In the case of I/O modules and the special function module with a high internal current consumption, mounting on an A6□B extension base unit is recommended. (Refer to Section 16.1 and Section 17.3 for details.)

3.1.2 Configuration of peripheral devices capable of QnACPU



*1 For details on the IC memory card reader/writer setting, refer to Operating Manual for the peripheral device capable of GPP functions.

*2 For connection to RS-422 interface, use the RS-422 ⇔ RS-232C converter.

*3 When connecting the serial communication module and the peripheral devices capable of GPP function, see User's Manual of the serial communication modules.

REMARK

1. For details on the system configuration for each peripheral device, refer to the Operating Manual for each.
2. QnACPU can connect a peripheral device capable of ACPU only when accessing an ACPU in another station via a MELSECNET/10 or MELSECNET data link. (However, QnACPU cannot be accessed.) In this case, set SW2 of system setting switch 2 on the CPU module ON.

3.2 System Configuration Overview

(a) Q2ACPU system

System configuration	* An example when the 16-point module is installed to each slot is shown.
Maximum number of extension stages	3rd extension stage
Maximum number of I/O modules	32 modules
Maximum number of I/O points	512 points
Main base unit model name	A32B, A32B-S1, A35B, A38B, A38HB, A38HBEU
Extension base unit model name	A62B, A65B, A68B, A52B, A55B, A58B
Extension cable model name	AC06B, AC12B, AC30B
Precautions	(1) It is not possible to connect an extension base unit to an A32B main base unit. For an extension base, use A32B-S1. (2) When using the extension base unit A52B, A55B, A58B, 5VDC is supplied from the power supply module of the main base unit. Before use, refer to Section 17.3 and examine if it can be used. (3) The overall distance of the extension cable must be 6.6m (21.65ft.) or shorter. (4) When using the extension cable, do not tie it with the main circuit cables, which has high voltage, large current, or install them close to each other.
I/O number assignment	(1) I/O numbers are allocated in accordance with the order of the numbers set for the extension base stages, regardless of the order in which the extension cables are connected. (2) Assign I/O numbers as if both main base unit and extension base unit have 8 slots each. Consequently, allocations of 16 points per slot are made for the parts of the system configuration drawing indicated with dotted lines. (3) 16 points are assigned to an empty slot. (4) Extension stage numbers do not need to be sequential, but any extension stage omitted from the system will occupy 8 (slots) × 16 I/O points. (5) With regard to items (2) to (4) above, the I/O allocations can be changed by setting I/O allocations in the parameters.(Refer to Section 5.3)

(b) Q2ACPU-S1 system

System configuration	Main base unit (A38B) Slot No. Extension cable 1st extension stage 2nd extension stage 3rd extension stage 4th extension stage 5th extension stage 6th extension stage 7th extension stage * An example when the 16-point module is installed to each slot is shown.
Maximum number of extension stages	7th extension stage
Maximum number of I/O modules	64 modules
Maximum number of I/O points	1024 points
Main base unit model name	A32B, A32B-S1, A35B, A38B, A38HB, A38HBEU
Extension base unit model name	A62B, A65B, A68B, A52B, A55B, A58B
Extension cable model name	AC06B, AC12B, AC30B
Precautions	(1) It is not possible to connect an extension base unit to an A32B main base unit. For an extension base, use A32B-S1. (2) When using extension base units A52B, A55B, A58B, 5VDC is supplied from the power supply module of the main base. Before use, refer to Section 17.3 and examine if it can be used. (3) The overall distance of the extension cable must be 6.6m (21.65ft.) or shorter. (4) When using the extension cable, do not tie it with the main circuit cables, which has high voltage, large current, or install them close to each other.
I/O number assignment	(1) I/O numbers are allocated in accordance with the order of the numbers set for the extension base stages, regardless of the order in which the extension cables are connected. (2) Assign I/O numbers as if both main base unit and extension base unit have 8 slots each. Consequently, allocations of 16 points per slot are made for the parts of the system configuration drawing indicated with dotted lines. (3) 16 points are assigned to an empty slot. (4) Extension stage numbers do not need to be sequential, but any extension stage omitted from the system will occupy 8 (slots) × 16 I/O points. (5) With regard to items (2) to (4) above, the I/O allocations can be changed by setting I/O allocations in the parameters. (Refer to Section 5.3)

(c) Q3A/Q4ACPU system

System configuration	Main base unit (A38B) Slot No. 0 1 2 3 4 5 6 7 C 00 10 20 30 40 50 60 70 P to to to to to to to to U 0F 1F 2F 3F 4F 5F 6F 7F * An example when the 16-point module is installed to each slot is shown. 1st extension stage A58B extension base unit 8 9 10 11 12 13 14 15 80 90 A0 B0 C0 D0 E0 F0 to to to to to to to to 8F 9F AF BF CF DF EF FF 2nd extension stage A55B extension base unit 16 17 18 19 20 (21)(22) (23) 100 110 120 130 140 150 160 170 to to to to to to to to 10F 11F 12F 13F 14F 15F 16F 17F 3rd extension stage A68B extension base unit 24 25 26 27 28 29 30 31 180 190 1A0 1B0 1C0 1D0 1E0 1F0 to to to to to to to to 18F 19F 1AF 1BF 1CF 1DF 1EF 1FF 4th extension stage A65B extension base unit 32 33 34 35 36 37 38 39 200 210 220 230 240 250 260 270 to to to to to to to to 20F 21F 22F 23F 24F 25F 26F 27F 5th extension stage A65B extension base unit 40 41 42 43 44 (45)(46) (47) 280 290 2A0 2B0 2C0 2D0 2E0 2F0 to to to to to to to to 28F 29F 2AF 2BF 2CF 2DF 2EF 2FF 6th extension stage A65B extension base unit 48 49 50 51 52 53 54 55 300 310 320 330 340 350 360 370 to to to to to to to to 30F 31F 32F 33F 34F 35F 36F 37F 7th extension stage A65B extension base unit 56 57 58 59 60 61 62 63 380 390 3A0 3B0 3C0 3D0 3E0 3F0 to to to to to to to to 38F 39F 3AF 3BF 3CF 3DF 3EF 3FF
Maximum number of extension stages	7th extension stage
Maximum number of I/O modules	64 modules
Maximum number of I/O points	Q3A...2048 points/Q4A...4096 points
Main base unit model name	A32B, A35B, A38B, A38HB, A38HBEU
Extension base unit model name	A62B, A65B, A68B, A52B, A55B, A58B
Extension cable model name	AC06B, AC12B, AC30B
Precautions	(1) It is not possible to connect an extension base unit to an A32B main base unit. For an extension base, use A32B-S1. (2) When extension base unit A52B, A55B, A58B is used, 5VDC power supply is supplied from the power supply module of the main base. Before use, refer to Section 17.3 and examine if it can be used. (3) The overall distance of the extension cable must be 6.6m (21.65ft.) or shorter. (4) When using the extension cable, do not tie it with the main circuit cables, which has high voltage, large current, or install them close to each other.
I/O number assignment	(1) I/O numbers are allocated in accordance with the order of the numbers set for the extension base stages, regardless of the order in which the extension cables are connected. (2) Assign I/O numbers as if both main base unit and extension base unit have 8 slots each. Consequently, allocations of 16 points per slot are made for the parts of the system configuration drawing indicated with dotted lines. (3) 16 points are assigned to an empty slot. (4) Extension stage numbers do not need to be sequential, but any extension stage omitted from the system will occupy 8 (slots) × 16 I/O points. (5) With regard to items (2) to (4) above, the I/O assignment can be changed by setting I/O assignments in the parameters. (Refer to Section 5.3)

3. SYSTEM CONFIGURATION

MELSEC-QnA

3.3 System Equipment

3.3.1 System equipment list

The following shows the system equipment (modules and peripheral devices) that can be used in a QnACPU system.

(1) For QnA module

Product Name	Model Name	Description	Number of Occupied Points (points) [I/O Allocation Module Type]	Current Consumption		Remark
				5VDC(A)	24VDC(A)	
CPU module	Q2ACPU	Number of I/O points: 512, built-in RAM: 28k steps	—	0.4	—	Memory card procured separately. Including memory card current consumption.
	Q2ACPU-S1	Number of I/O points: 1024, built-in RAM: 60k steps		0.4	—	
	Q3ACPU	Number of I/O points: 2048, built-in RAM: 92k steps		0.4	—	
	Q4ACPU	Number of I/O points: 4096, built-in RAM: 124k steps		0.9	—	
Memory card	Q1MEM-64S	SRAM, 64k bytes	—	—	—	For use with QnACPU only
	Q1MEM-128S	SRAM, 128k bytes				
	Q1MEM-256S	SRAM, 256k bytes				
	Q1MEM-512S	SRAM, 512k bytes				
	Q1MEM-1MS	SRAM, 1M bytes				
	Q1MEM-2MS	SRAM, 2M bytes				
	Q1MEM-64SE	SRAM, 32k bytes, E ² PROM, 32k bytes				
	Q1MEM-128SE	SRAM, 64k bytes, E ² PROM, 64k bytes				
	Q1MEM-256SE	SRAM, 128k bytes, E ² PROM, 128k bytes				
	Q1MEM-512SE	SRAM, 256k bytes, E ² PROM, 256k bytes				
	Q1MEM-1MSE	SRAM, 512k bytes, E ² PROM, 512k bytes				

3. SYSTEM CONFIGURATION

MELSEC-QnA

Product Name	Model Name	Description	Number of Occupied Points (points) [I/O Allocation Module Type]	Current Consumption		Remark
				5VDC(A)	24VDC(A)	
Input module	AX10	16-input 100VAC input module	16 (16 inputs)	0.055	—	
	AX11	32-input 100VAC input module	32 (32 inputs)	0.11	—	
	AX11EU	32-input 100VAC input module CE-compliant	32 (32 inputs)	0.15	—	
	AX20	16-input 200VAC input module	16 (16 inputs)	0.055	—	
	AX21	32-input 200VAC input module	32 (32 inputs)	0.11	—	
	AX21EU	32-point 200VAC input module CE-compliant	32 (32 inputs)	0.15	—	
	AX31	32-input 12/24VAC/DC input module	32 (32 inputs)	0.11	—	
	AX31-S1	32-input 24VDC input module	32 (32 inputs)	0.11	—	
	AX40	16-input 12/24VDC input module	16 (16 inputs)	0.055	—	
	AX41	32-point 12/24VDC input module	32 (32 inputs)	0.11	—	
	AX41-S1	32-point 12/24VDC input module	32 (32 inputs)	0.11	—	
	AX42	64-input 12/24VDC input module	64 (64 inputs)	0.12	—	
	AX50	16-input 48VDC sink input module	16 (16 inputs)	0.055	—	
	AX50-S1	16-input 48VDC sink/source input module	16 (16 inputs)	0.055	—	
	AX60	16-input 100/110/125VDC sink input module	16 (16 inputs)	0.055	—	
	AX60-S1	16-input 100/110/125VDC sink/source input module	16 (16 inputs)	0.055	—	
	AX70	16-input input module for sensor	16 (16 inputs)	0.055	—	
	AX71	32-input input module for sensor	32 (32 inputs)	0.11	—	
	AX80	16-input 12/24VDC source input module	16 (16 inputs)	0.055	—	
	AX80E	16-input 12/24VDC source input module	16 (16 inputs)	0.055	—	
	AX81	32-input 12/24VDC source input module	32 (32 inputs)	0.11	—	
	AX81-S1	32-input 12/24VDC source input module	32 (32 inputs)	0.105	—	
	AX81-S2	32-input 48/60VDC source input module	32 (32 inputs)	0.11	—	
	AX81-S3	32-input 12/24VDC source input module	32 (32 inputs)	0.11	—	
	AX81B	32-input 24VDC sink/source input module	64 (64 inputs)	0.125	—	
	AX82	64-point 12/24VDC source input module	64 (64 inputs)	0.12	—	

3. SYSTEM CONFIGURATION

MELSEC-QnA

Product Name	Model Name	Description	Number of Occupied Points (points) [I/O Allocation Module Type]	Current Consumption		Remark
				5VDC(A)	24VDC(A)	
Output module	AY10	16-output relay contact output module (2A)	16 (16 outputs)	0.115	0.15	The short protection and overheat protection functions of the AY40P, AY41P, AY60EP, AY80EP, AY81EP, and AY82EP are described below:
	AY10A	16-output relay contact output module, for independent contact output	16 (16 outputs)	0.115	0.15	
	AY11	16-output relay contact output module, with surge suppressor	16 (16 outputs)	0.115	0.15	
	AY11A	16-output relay contact output module, for independent contact output, with surge suppressor	16 (16 outputs)	0.115	0.15	
	AY11AEU	16-output relay contact output module, for independent contact output, with surge suppressor	16 (16 outputs)	0.115	0.15	
	AY11E	16-output relay contact output module (fused)	16 (16 outputs)	0.115	0.15	
	AY11EEU	16-output relay contact output module (fused)	16 (16 outputs)	0.115	0.15	
	AY13	32-point relay contact output module (2A)	32 (32 outputs)	0.23	0.29	
	AY13E	32-point relay contact output module	32 (32 outputs)	0.23	0.29	
	AY13EU	32-output relay contact output module (fused)	32 (32 outputs)	0.23	0.29	
	AY15EU	24-point relay contact output module (2A) CE-compliant	32 (32 outputs)	0.15	0.22	Function that protects the transistors from overcurrents occurring, for example, due to short circuits in external wiring.
	AY22	16-point triac output module (2A, fused)	16 (16 outputs)	0.305	—	
	AY23	32-point triac output module (0.6A, fused)	32 (32 outputs)	0.59	—	
	AY40	16-output 12/24VDC transistor output module (0.1A)	16 (16 outputs)	0.115	0.016	
	AY40A	16-point 12/24VDC transistor output module, for independent contact output (0.3A)	16 (16 outputs)	0.19	—	
	AY41	32-output 12/24VDC transistor output module (0.1A)	32 (32 outputs)	0.23	0.04	
	AY42	64-output 12/24VDC transistor output module (0.1A)	64 (64 outputs)	0.29	0.08	
	AY42-S1	64-output 12/24VDC transistor output module (0.1A)	64 (64 outputs)	0.29	0.08	
	AY42-S3	64-output 12/24 VDC transistor output module (fused)	64 (64 outputs)	0.29	0.08	
	AY42-S4	64-output 12/24VDC transistor output module, zener diode with built-in photocoupler	64 (64 outputs)	0.50	—	

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MELSEC-QnA

Product Name	Model Name	Description	Number of Occupied Points (points) [I/O Allocation Module Type]	Current Consumption		Remark
				5VDC(A)	24VDC(A)	
Output module	AY50	16-point 12/24VDC transistor output module (0.5A, fused)	16 (16 outputs)	0.115	0.13	*1: Indicates a source load module. Other modules are sink load modules.
	AY51	32-output 12/24VDC transistor output module (0.5A)	32 (32 outputs)	0.23	0.10	
	AY51-S1	32-point 12/24VDC transistor output module (0.3A, fused)	32 (32 outputs)	0.31	0.02	
	AY60	16-output 12/24/48VDC transistor output module (2A, fused)	16 (16 outputs)	0.115	0.13	
	AY60S	16-output 12/24/48VDC transistor output module (2A)	16 (16 outputs)	0.075	0.006	The short protection and overheat protection functions of the AY40P, AY41P, AY60EP, AY80EP, AY81EP, and AY82EP are described below:
	AY60EP *1	16-output 12/24 VDC transistor output module (2A), with short protection function and overheat protection function	16 (16 outputs)	0.115	0.22	
	AY70	16-output, CMOS (5/12VDC) output module (16mA)	16 (16 outputs)	0.10	12VDC 0.11	
	AY71	32-output, CMOS (5/12VDC) output module (16mA)	32 (32 outputs)	0.20	12VDC 0.20	
	AY72	64-output, CMOS (5/12VDC) output module (16mA)	64 (64 outputs)	0.30	12VDC 0.60	Short protection function
	AY80 *1	16-output 12/24/48VDC transistor output module (0.5A, fused)	16 (16 outputs)	0.115	0.12	
	AY81 *1	32-output 12/24VDC transistor output module (0.5A)	32 (32 outputs)	0.23	0.10	Overheat protection function
	AY82EP *1	64-output 12/24VDC transistor output module (0.1A), with short protection function and overheat protection function	64 (64 outputs)	0.29	0.10	
Dynamic input/output combination module	A42XY	64 inputs, 64 outputs, dynamic scanning mode	64 (64 outputs)	0.11	0.235	Performs I/O processing in 8-point units independently of the CPU module, while scanning.
Input/output combination module	AH42	32 inputs, 32 outputs, 12/24VDC transistor output module (0.1A)	64 (64 outputs)	0.245	0.04	The first half 32 points are inputs and the second half 32 points are outputs.

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MELSEC-QnA

Product Name		Model Name	Description	Number of Occupied Points (points) [I/O Allocation Module Type]	Current Consumption		Remark
					5VDC(A)	24VDC(A)	
Special function module	1-axis positioning module	AD70	1-axis positioning control, speed control and speed-positioning control, analog voltage output for speed-positioning control (0 to $\pm 10V$)	32 (special 32 points)	0.3	—	
		AD70D-S2	1-axis, digital output, for MR-SB(K)/SD	32 (special 32 points)	0.8	—	
	Positioning module	AD72	For positioning control analog voltage output for speed-positioning control (0 to $\pm 10V$) 2-axis (independent control, simultaneous 2-axis control, linear interpolation control).	48 $\left\{ \begin{array}{l} \text{First half:} \\ \text{empty 16 points} \\ \text{Second half:} \\ \text{special 32 points} \end{array} \right\}$	0.9	—	
		AD75P1-S3	For positioning control, pulse output P1: 1 axis P2: 2 axes (Independent, simultaneous 2 axes, linear interpolation, circular interpolation) P3: 3 axes (Independent, simultaneous 3 axes, linear interpolation 2 axes, circular interpolation 2 axes)	32 (special 32 points)	0.7	—	* When differential driver is connected: 0.78
		AD75P2-S3			0.7		
		AD75P3-S3			0.7 *		
		AD75M1	Digital output for positioning control, for MR-H-B/MR-JB/ MR-J2-B P1: 1 axis P2: 2 axes (Independent, simultaneous 2 axes, linear interpolation, circular interpolation) P3: 3 axes (Independent, simultaneous 3 axes, linear interpolation 2 axes, circular interpolation 2 axes)	32 (special 32 points)	0.7	—	
		AD75M2					
		AD75M3					
	Positioning detection module	A61LS	Absolute detection method. Resolution: One resolver revolution = 4096 divisions. Response speed: within 6ms	48 $\left\{ \begin{array}{l} \text{First half:} \\ \text{special 32 points} \\ \text{Second half:} \\ \text{empty 16 points} \end{array} \right\}$	0.8	—	
		A62LS-S5	Absolute detection method, multiple rotation type, linear type Resolution: 4096 divisions $\times$ 32 rotations to 409.6 divisions $\times$ 320 rotations Response speed: 2ms, 8 channels	48 $\left\{ \begin{array}{l} \text{First half:} \\ \text{empty 16 points} \\ \text{Second half:} \\ \text{special 32 points} \end{array} \right\}$	1.5	—	The resolution depends on the connected resolver.
		A63LS	Absolute detection method, multiple rotation type Resolution: 4096 divisions $\times$ 32 rotations to 409.6 divisions $\times$ 320 rotations Response speed: 2ms, 8 channels	32 (special 32 points)	0.9	—	When setting module is connected: 5VDC current consumption: 1.35A
	Ultrasonic linear scale module	A64BTL	Measuring range: 0.000 to 3,550,000 mm Resolution: 0.025mm, 4 channels	32 (special 32 points)	1.05	—	

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Product Name		Model Name	Description	Number of Occupied Points (points) [I/O Allocation Module Type]	Current Consumption		Remark
					5VDC(A)	24VDC(A)	
Special function module	High-speed counter module	AD61	24-bit binary, 1/2 phase input, reversible counter, 50kPPS, 2 channels	32 (special 32 points)	0.3	—	
		AD61S1	24-bit binary, 1/2 phase input, reversible counter, 1 phase ... 10kPPS, 2 phases ... 7kPPS, 2 channels	32 (special 32 points)	0.3	—	
	A/D converter module	A68AD	4 to 20mA/0 to ± 10 V, Analog input, 8 channels	32 (special 32 points)	0.9	—	
		A68AD-S2					
		A68ADN	0 to ± 20 mA/0 to ± 10 V, Analog input, 8 channels	32 (special 32 points)	0.4	—	
		A616AD	4 to 20mA/0 to ± 10 V, Analog input, 16 channels Expansion to maximum of 121 channels possible by using A60MX(R)	32 (special 32 points)	1.0	—	
		A60MX	Multiplex module (IC relay) Analog input, 16 channels	16 (empty 16 points)	0.65	—	Used in combination with A616AD or A616TD.
		A60MXR	Multiplex module (mercury relay) Analog input, 16 channels	16 (empty 16 points)	0.5	—	
		A60MXRN	Multiplex module (photo MOS relay) Analog input, 16 channels	16 (empty 16 points)	0.35	—	
	Temperature digital converter module	A616TD	For temperature detection by thermocouple (when connected to A60MXT). 0 to ± 10 V/0 to 20mA (when connected to A60MX(R))	32 (special 32 points)	1.0	—	
		A60MXT	Multiplex module (mercury relay) Temperature input: 15 channels. Temperature detection by thermocouple when used in combination with A616TD.	32 $\left\{ \begin{array}{l} \text{First half:} \\ \text{empty 16 points} \\ \text{Second half:} \\ \text{empty 16 points} \end{array} \right\}$	0.8	—	Used in combination with A616TD.
		A60MXTN	Multiplex module (photo MOS relay) Temperature input: 15 channels. Temperature detection by thermocouple when used in combination with A616TD.	32 $\left\{ \begin{array}{l} \text{First half:} \\ \text{empty 16 points} \\ \text{Second half:} \\ \text{empty 16 points} \end{array} \right\}$	0.64	—	
		A68RD3	-180 to 600°C temperature input module (For 3-wire type platinum resistor)	32 (special 32 points)	0.94	—	
		A68RD4	-180 to 600°C temperature input module (For 4-wire type platinum resistor)		0.75	—	

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Product Name		Model Name	Description	Number of Occupied Points (points) [I/O Allocation Module Type]	Current Consumption		Remark
					5VDC(A)	24VDC(A)	
Special function module	D/A converter module	A68DAV	0 to ± 10V, analog output, 8 channels.	32 (special 32 points)	0.15	0.5	
		A68DAI-S1	0 to 20mA, analog output, 8 channels.	32 (special 32 points)	0.15	0.4	
		A62DA	4 to 20mA/0 to ± 10V Analog output 12 bits, 2 channels	32 (special 32 points)	0.6	0.35	
		A62DA-S1	4 to 20mA/0 to ± 10V Analog output, 2 channels				
		A616DAI	4 to 20mA. Resolution: 1/4000 Analog output, 16 channels	32 (special 32 points)	0.3	—	15VDC (A68P) +0.53A -0.125A is required.
		A616DAV	0 to ± 10 V/0 to ± 5 V. Resolution: 1/4000 Analog output, 16 channels	32 (special 32 points)	0.38	—	15VDC (A68P) +0.2A -0.17A is required.
	Memory card, Centronics interface module	AD59*4	32k byte-memory battery backup Can be connected to printer conforming to Centronics standards	32 (special 32 points)	0.3	—	0.35A when connected to AD59MEF.
		AD59-S1*4			0.32		
		Voice output module	A11VC*4	Messages can be recorded and played back on a maximum of 60 channels. The following recording times can be selected for each channel: 1 second, 2 seconds, 4 seconds, 8 seconds. The total recording time is 64 seconds	16 (special 16 points)	0.6	0.38
Network module		AJ71QLP21	For MELSECNET/10 optical loop networks (compatible with SI cable)	32 (special 32 points)	0.65	—	• For Use with QnACPU Only • Maximum 4 units including AJ71QE71 can be used for one CPU module.
		AJ71QLP21G	For MELSECNET/10 optical loop network (compatible with GI cable)				
		AJ71QLP21S	For MELSECNET/10 optical loop networks. Network backup by external power supply	32 (special 32 points)	0.65	0.2	
		AJ71QBR11	For MELSECNET/10 coaxial bus networks	32 (special 32 points)	0.8	—	
		AJ71QLR21	For MELSECNET/10 coaxial loop network		1.14		
		AJ72QLP25	For MELSECNET/10 optical loop network remote I/O stations (compatible with SI cable)	—	0.8	—	
		AJ72QLP25G	For MELSECNET/10 optical loop network remote I/O station (compatible with GI cable)				
		AJ72QBR15	For MELSECNET/10 coaxial bus network remote I/O stations	—	0.9	—	
		AJ72QLR25	For MELSECNET/10 coaxial loop network remote I/O station		1.3		

*4 Models to be discontinued

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Product Name	Model Name	Description	Number of Occupied Points (points) [I/O Allocation Module Type]	Current Consumption		Remark
				5VDC(A)	24VDC(A)	
Data link module	AJ71AP21 *2	For MELSECNET II optical data links	32 (special 32 points)	0.5	—	Maximum 2 modules can be used for one CPU module.
	AJ71AP21-S3 *1	For MELSECNET II optical data link (compatible with GI cable)				
	AJ71AR21 *2	For MELSECNET II coaxial data links				
	AJ71AT21B *2	For MELSECNET/B data links				
	AJ72P25 *2	For MESLECNET optical data link remote I/O station	—	0.23	—	
	AJ72P25-S3	For MESLECNET optical data link remote I/O station (compatible with GI cable)				
	AJ72R25 *2	For MESLECNET coaxial data link remote I/O station				
	AJ72T25B *2	For MELSECNET/B data link remote I/O stations				
Serial communications module	AJ71QC24N	Link module that communicates data with a computer. Transmission speed: 300bps to 19.2kbps RS-232, RS-422/485: one channel each	32 (special 32 points)	0.3	—	• For use with QnACPU only
	AJ71QC24 N-R2	Link module that communicates data with a computer. Transmission speed: 300bps to 19.2kbps RS-232C: 2 channels	32 (special 32 points)	0.2	—	
	AJ71QC24 N-R4	Link module that communicates data with a computer. Transmission speed: 300bps to 19.2kbps RS-422: 2 channels	32 (special 32 points)	0.38	—	
Ethernet interface module	AJ71QE71-B2	10BASE2 specification Transmission speed: 10Mbps	32 (special 32 points)	0.56	—	• For use with QnACPU only • Maximum 4 units including the network module can be used for one CPU module.
	AJ71QE71N-B5	10BASE5 specification Transmission speed: 10 Mbps		0.40		
	AJ71QE71N3-T	10BASE-T specification Transmission speed: 10Mbps		0.53		
	AJ71E71N-B2 *2	10BASE2 specification, Transmission speed: 10 Mbps		0.67	—	
	AJ71E71N-B5 *2	10BASE5 specification, Transmission speed: 10Mbps		0.55		
	AJ71E71N3-T *2	10BASE-T specification Transmission speed: 10Mbps		0.69		

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Product Name	Model Name	Description	Number of Occupied Points (points) [I/O Allocation Module Type]	Current Consumption		Remark
				5VDC(A)	24VDC(A)	
Computer link module	AJ71UC24 *2	Link module that communicates data with a computer. Transmission speed: 300bps to 19.2kbps RS-232C, RS-422: one channel each, compatible with RS485	32 (special 32 points)	0.3	—	Maximum 6 modules can be used for one CPU module.
Intelligent communication module	AD51H-S3	AD51H-BASIC, maximum of 8 tasks executes data communication with a PLC or a computer, and monitoring control status. Data communication with a computer can be executed by any format. RS-232C: 2 channels, RS-422, Parallel: one channel each	48 $\left\{ \begin{array}{l} \text{First half:} \\ \text{empty 16 points} \\ \text{Second half:} \\ \text{special 32 points} \end{array} \right\}$	1.0	—	
Host controller high-speed link module	AJ71C23-S3 *2	Link module that sends/receives data at high speed to/from a computer. Transmission speed: 500kbps RS-422: one channel each	32 (special 32 points)	1.5	—	
Multidrop data link module	AJ71C22-S1	Sends and receives bit data to maximum 8 slave stations to which it is connected in a multidrop system. Used for the master station of a multidrop link. Transmission speed: 38.4kbps RS-422: one channel each	32 (special 32 points)	1.4	—	
	A0J2C25	Used for a remote I/O station of a multidrop link.	—	—	—	
	A0J2C214(S1)	Used for a local station in a multidrop link. (In A0J2CPU and A0J2HCPU systems, A0J2C214 can also be used as the master station in computer links and multidrop data links)	64 points	0.3	—	
CC-Link system master/local module	AJ61QBT11	For CC-Link system master and local stations When used as the master station, the module controls maximum 64 remote I/O stations. When a local station is used, the module occupies 1 or 4 station(s).	32 (special 32 points)	0.45	—	For use with QnACPU only
MELSECNET/ MINI-S3 data link module	AJ71PT32-S3	For MELSECNET/MINI-S3 master stations (max. 64 stations). Performs remote I/O and remote terminal control of a total of 512 I/O points.	I/O dedicated mode 32 (special 32 points)	0.34	—	
	AJ71T32-S3		Expanded mode 48 (special 48 points)			
B/NET interface module	AJ71B62-S3	Used for B/NET transmission terminal control. Up to 63 stations can be controlled per module.	32 (special 32 points)	0.17	—	
Interrupt module	AI61	Used to designate execution of interrupt programs (16 interrupt inputs).	32 (special 32 points)	0.14	—	Only one module can be used per CPU.
	AI61-S1	Product for changing time to turn ON/OFF AI61				

*2 Only internal devices within the AnACPU range can be accessed (file registers cannot be accessed).

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Product Name	Model Name	Description	Number of Occupied Points (points) [I/O Assignment Module Type]	Current Consumption		Remark
				5VDC(A)	24VDC(A)	
Device Net interface module	AJ71DN91	Device Net master module Total I/O points: 4096 points	32 (special 32 points)	0.24	–	
PROFIBUS-DP interface module	AJ71PB92D	PROFIBUS-DP master module Sendable data Regular service: 32 bytes Extension service: 244 bytes	32 (special 32 points)	0.54	–	
PROFIBUS-FMS interface module	AJ71PB96F	PROFIBUS-FMS master/client/server module Total I/O points: 241241 points	32 (special 32 points)	0.54	–	
MODBUS serial communication module	AJ71UC24-R2 *2	MODBUS serial communication module Transmission speed: 300bps to 19200bps	32 (special 32 points)	1.4	–	
PLC easier monitoring module	AS91	PLC easier monitoring module	16 (16 outputs)	0.08	–	With simulation switch 16 points
Dummy module	AG62	Module allows selection of 16, 32, 48, or 64 points.	Setting range [Input Set number of points]	0.07	–	
Blank cover	AG60	Dust-proof cover for unused slot	16 (empty 16 points)	–	–	CE-compliant

*2 Only internal devices within the AnACPU range can be accessed (file registers cannot be accessed).

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Product Name	Model Name	Description	Number of Occupied Points (points) [I/O Assignment Module Type]	Current Consumption		Remark
				5VDC(A)	24VDC(A)	
Graphic operation terminal	A985GOT	Large-size graphic operation terminal 256 colors, TFT color, 800 × 600 dots, high intensity	32 (special 32 points)*	0.22 *	—	*When bus connected
	A975GOT	Large-size graphic operation terminal 256 colors, TFT color, 640 × 480 dots, high intensity/256 colors, TFT color, 640 × 480 dots, wide viewing angle				
	A970GOT	Large-size graphic operation terminal 16 colors, TFT color, 640 × 480 dots, high intensity/16 colors, TFT color, 640 × 480 dots, wide viewing angle/8 colors, STN color, 640 × 480 dots/2 colors, STN monochrome, 640 × 480 dots				
	A960GOT	Large-size graphic operation terminal 2 colors, EL, 640 × 400 dots				
	A956GOT	Medium-size graphic operation terminal 8 colors, STN color, 320 × 240 dots/ STN monochrome, 320 × 240 dots/ 256 colors, TFT color, 320 × 240 dots, high intensity				
	A956WGOT	Medium-size graphic operation terminal 256 colors, TFT color, 320 × 240 dots, high intensity				
	A953GOT	Medium-size graphic operation terminal 8 colors, STN color, 320 × 240 dots/ STN monochrome, 320 × 240 dots/ 256 colors, TFT color, 320 × 240 dots, high intensity With handheld type	—	—	—	For RS-232C connected only
	A951GOT	Medium-size graphic operation terminal 8 colors, STN color, 320 × 240 dots/ STN monochrome, 320 × 240 dots/ 256 colors, TFT color, 320 × 240 dots, high intensity	32 (special 32 points)*	0.22 *	—	*When bus connected
	A950GOT	Medium-size graphic operation terminal 8 colors, STN color, 320 × 240 dots/ STN monochrome, 320 × 240 dots/ 256 colors, TFT color, 320 × 240 dots, high intensity With handheld type	—	—	—	Dedicated to RS-422 connection
	GT1565-VTBA	Large-size graphic operation terminal 8.4" 256 colors, TFT color, 640 × 480 dots (When installing a multi color display board, 65536 colors can be displayed.)	32 (special 32 points)*	0.12	—	*When bus connected
	GT1575-VTBA	Large-size graphic operation terminal 10.4" 256 colors, TFT color, 640 × 480 dots (When installing a multi color display board, 65536 colors can be displayed.)				

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Product Name		Model Name	Description	Number of Occupied Points (points) [I/O Assignment Module Type]	Current Consumption		Remark
					5VDC(A)	24VDC(A)	
Power supply module	Power supply slot mounting position	A61P A61PN	100/200VAC input Output: 5VDC 8A		-	-	
		A61PEU					CE-compliant
		A62P	100/200VAC input				
		A62PEU	Output: 5VDC 5A, 24VDC 0.8A				CE-compliant
		A63P	24VDC input Output: 5VDC 8A				
	I/O slot mounting position	A66P	100/200VAC input Output: 24VDC 1.2A	16 (empty 16 points)			Power supply for AD70, A616DAV, A616DAI
		A68P	100/200VAC input Output: +15VDC 1.2A, -15VDC 0.7A	32 $\left\{ \begin{array}{l} \text{First half:} \\ \text{empty 16 points} \\ \text{Second half:} \\ \text{empty 16 points} \end{array} \right\}$			
Base unit	Main base unit	A38HB	8 I/O modules can be installed.	-	-	-	For high-speed access (dedicated to QnACPU)
		A38HBEU	8 I/O modules can be installed.				For high-speed access (dedicated to QnACPU) CE-compliant
		A38B	8 I/O modules can be installed.				
		A35B	5 I/O modules can be installed.				
		A32B	2 I/O modules can be installed.				No connector for extension.
		A32B-S1	2 I/O modules can be installed.				With connector for extension.
	Extension base unit	A68B	8 I/O modules can be installed.	-	-	-	The power supply module is required.
		A65B	5 I/O modules can be installed.				
		A62B	2 I/O modules can be installed.				
		A58B	8 I/O modules can be installed.	-	-	-	A61P, A61PN, A62P, A63P, and A65P cannot be mounted.
		A55B	5 I/O modules can be installed.				
		A52B	2 I/O modules can be installed.				
Extension cable	AC06B		600mm (23.62inch) long	-	-	-	
	AC12B		1200mm (47.24inch) long				
	AC30B		3000mm (118.11inch) long				

3. SYSTEM CONFIGURATION

MELSEC-QnA

Product Name	Model Name	Description	Number of Occupied Points (points) [I/O Assignment Module Type]	Current Consumption		Remark
				5VDC(A)	24VDC(A)	
Simulation switch	A6SW16	16-point simulation switch	—	—	—	Installed in an input module.
	A6SW32	32-point simulation switch				
Battery	A6BAT	Built-in RAM memory backup	—	—	—	Mounting to QnACPU module
Fuse	For AY11E, AY13E	MF51NM8 FGMA250V 8A	—	—	—	
	For AY22	HP-70K				
	For AY23	HP-32				
	For AY50, AY80	MP-20				
	For AY60	MP-32				
	For AY60E	MP-50				
	For power supply	GTH4 FGTA250V 4A				
	For A63P	SM6.3A FGTA250V 6A				

3. SYSTEM CONFIGURATION

MELSEC-QnA

Product Name	Model Name	Description	Applicable Model
Connector/terminal block converter module	A6TBXY36	For sink-type input module and sink-type output module (standard type)	AX42(S1), AY42(S1/S3/S4), AH42
	A6TBXY54	For sink-type input module and sink-type output module. (2-wire type)	
	A6TBX70	For sink-type input module (3-wire type)	AX42(S1), AH42
	A6TBX36-E	For source-type input module (standard type)	AX82
	A6TBY36-E	For source-type output module (standard type)	AY82EP
	A6TBX54-E	For source-type input module (2-wire type)	AX82
	A6TBY54-E	For source-type output module (2-wire type)	AY82EP
	A6TBX70-E	For source type input modules (3-wire type)	AX82
Cable for connector/terminal block converter module	AC05TB	For 0.5m (1.64ft.) sink module	A6TBXY36 A6TBXY54 A6TBX70
	AC10TB	For 1m (3.28ft.) sink module	
	AC20TB	For 2m (6.56ft.) sink module	
	AC30TB	For 3m (9.84ft.) sink module	
	AC50TB	For 5m (16.40ft.) sink module	
	AC80TB	For 8m (314.96inch) sink module (Common current: 0.5A or less)	
	AC100TB	For 10m (393.7inch) sink module (Common current: 0.5A or less)	
	AC05TB-E	For 0.5m (1.64ft.) source module	A6TBX36-E A6TBY36-E A6TBX54-E A6TBY54-E A6TBX70-E
	AC10TB-E	For 1m (3.28ft.) source module	
	AC20TB-E	For 2m (6.56ft.) source module	
	AC30TB-E	For 3m (9.84ft.) source module	
	AC50TB-E	For 5m (16.40ft.) source module	
Relay terminal module	A6TE2-16SRN	For sink-type output module	AY42, AY42-S1, AY42-S3, AY42-S4, AH42
Cable for connecting relay terminal module	AC06TE	0.6 m (1.97ft.) long	A6TE2-16SRN
	AC10TE	1m (3.28ft.) long	
	AC30TE	3m (9.84ft.) long	
	AC50TE	5m (16.40ft.) long	
	AC100TE	10m (32.80ft.) long	

REMARK

Toa Electric Industrial CO., LTD. provides I/O cables with connectors, which can connect to 40-pin connector (AX42, AY42, etc.) or 37-pin D-sub connector (AX82, AY82) of I/O modules.

Contact:

TOA ELECTRIC INDUSTRIAL CO., LTD.

(2) Peripheral device

Product Name	Model Name	Remark
Programming unit	Q6PU	Connected to the CPU module by an RS-422 cable (AC30R4-PUS, AC20R4-A8PU); for program writing and reading. (5VDC 0.4A)
RS-422 cable	AC30R4-PUS	Cable for connection between CPU module and Q6PU 3m (9.84ft.) long
	AC20R4-A8PU	Cable for connection between CPU module and Q6PU 2m (6.56ft.) long

3.3.2 Precautions when configuring the system

The following shows the hardware and software packages which can be used for QnACPU.

(1) Hardware

- (a) The number of modules that can be mounted is restricted depending on the module type.

Applicable Module	Dedicated to QnACPU	For ACPU	Remark
I/O module	–	No restrictions	–
Special function module	No restrictions	No restrictions	–
Intelligent special function module	No restrictions	Total 6 modules	Including GOT-A900 Series (Only when the bus connection is used.), and GOT1000 Series (Only when the bus connection is used.)
Interrupt module	–	Only 1 module	–
Link module · Ethernet module	Total 4 for network, Ethernet use	Total 2 for data link use	Total 4 for network, Ethernet and data link use

REMARK

The modules described above are categorized as follows.

- 1) I/O module..... Standard input modules and output modules
- 2) Special function module..... Special function modules that perform processing in accordance with FROM/TO instructions from the QnACPU (for example: A68AD, A62DA, etc.)
- 3) Intelligent special function..... Special function modules that can process not only by executing FROM/TO instruction of QnACPU but also by accessing QnACPU from special function module (Example: AJ71UC24, AJ71QC24N, etc.)
module
- 4) Interrupt module..... Modules that issue interrupts to the QnACPU (AI61)
- 5) Link module..... Special function modules for MELSECNET II, /B data links and MELSECNET/10 networks. (Example: AJ71AP21, AJ71QLP21, etc.)
- 6) Ethernet module..... Dedicated Ethernet interface modules for QnACPU (AJ71QE71, AJ71QE71-B5)

(b) The following shows special function modules that cannot be used with QnACPU:

- AJ71C23 (Host controller high-speed link module)
- AD57-S2 (A6MD controller module)
- AJ71C24 (Computer link module): Manufactured through February 1987.

Products manufactured in March 1987 or later,
 and products marked "H" (corresponding to A3H)
 can be used.
- AD51 (Intelligent communication module): Manufactured through March 1987.

Products manufactured in April 1987 or later,
 and products marked "H"(corresponding to A3H)
 can be used.
- A7GT-BUS (Bus connection interface module for A77GOT and A870GOT):
 Manufactured through January 1996.

Products manufactured in February 1996 or
 later, and products marked "C" (corresponding to
 A3H) can be used.
- AJ71LP21(G), AJ71BR11, AJ71LR21 (MELSECNET/10 network modules)

(c) When using a special function module with QnACPU, the device range to be used is depending on models of special function modules.

Device	Model				
	AD51(S3), AJ71C24-S3, AJ71P41 *1	AD51H(S3), AD51FD-S3, AJ71C23-S3, AJ71C24-S6/S8, AJ71UC24, AJ71ME81 *2	AJ71E71 *2		
			Q2A	Q2A-S1	Q3A, Q4A
I/O device (X/Y)	X/Y0 to X/Y7FF	X/Y0 to X/Y7FF	X/Y0 to X/Y1FF	X/Y0 to X/Y3FF	X/Y0 to X/Y7FF
Internal relays (M, L, S) *3	M0 to M2047	M0 to M8191	M0 to M8191		
Link relay (B)	B0 to B3FF	B0 to BFFF	B0 to BFFF		
Timer (T)	T0 to T255	T0 to T2047	T0 to T2047		
Counter (C)	C0 to C255	C0 to C1023	C0 to C1023		
Data register (D)	D0 to D1023	D0 to D6143	D0 to D6143		
Link register (W)	W0 to W3FF	W0 to WFFF	W0 to WFFF		
Annunciator (F)	F0 to F255	F0 to F2047	F0 to F2047		

*1 Only the device range equivalent to that of A3HCPU can be accessed.
 Reading/Writing of file registers, programs, etc. are not possible.

*2 Only the device range equivalent to that of AnACPU can be accessed. Reading/Writing of file registers, programs, etc. are not possible.

*3 Even when L or S is specified, the device becomes M.
 (Example: Even when L10 is specified, the device becomes M10.)

- (d) When a QnACPU is mounted on a main base unit for A38HB/A38HBEU high-speed access, the QnACPU can access special function modules, intelligent special function modules and link modules to write/read at greater speeds. QnACPU cannot input/output to the I/O module at greater speed.
- (e) The following shows how to connect graphic operation terminal units to a QnACPU.

Model	Connection Method	Accessible Device Range
GOT1000 series	Direct connection to CPU Computer link connection CC-Link connection MELSECNET/10 connection Bus connection	Access is available for all device ranges of QnACPU. (Refer to the GT Works2/GT Designer2 Reference Manual for details.)
GOT-A900 series	Direct connection to CPU Computer link connection CC-Link connection MELSECNET(II), /B, /10 connection Bus connection	Access is available for all device ranges of QnACPU. (Refer to the GT Works2/GT Designer2 Reference Manual for details.)

- (f) The accessible range for an AJ71UC24 computer link module comprises the CPU to which the AJ71UC24CPU is mounted (the host station) and the other stations in the network to which the host station is connected. It is not possible to access other stations in other networks by using the MELSECNET/10 network system routing function.

The access range for an AJ71QC24N serial communication module is the host station, other stations in the network connected to the host station, and other stations in other networks accessed through up to 7 relay stations by using the routing function.

- (g) When accessing from intelligent communication module AD51H-S3 to other station QnACPU on the network, only Format 1 control table can be used. Format 2 control table cannot be used. Access to other network is not allowed on Format 1 control table.
- (h) In QnACPU, I/O assignment set with the parameter cannot be valid for MELSECNET (II) and MELSECNET/B. When setting the I/O assignment for a remote I/O station, build the remote I/O network with MELSECNET/10.

(2) Software package

The following shows the system start-up software packages to create programs for QnACPU.

Peripheral Device Capable of GPP Functions	Software Package for System Start-up
Personal computer	GX Developer, SW□IVD-GPPQ

Apart from the above, the following software packages can be used.

- CAD interface package SW□IVD-CADQ
- Data conversion package SW□IVD-CNVQ
- Macro/library package SW□IVD-MSDQ
- SW□IVD-MSPQ
- Ladder sequence linking package SW□IVD-LNKQ

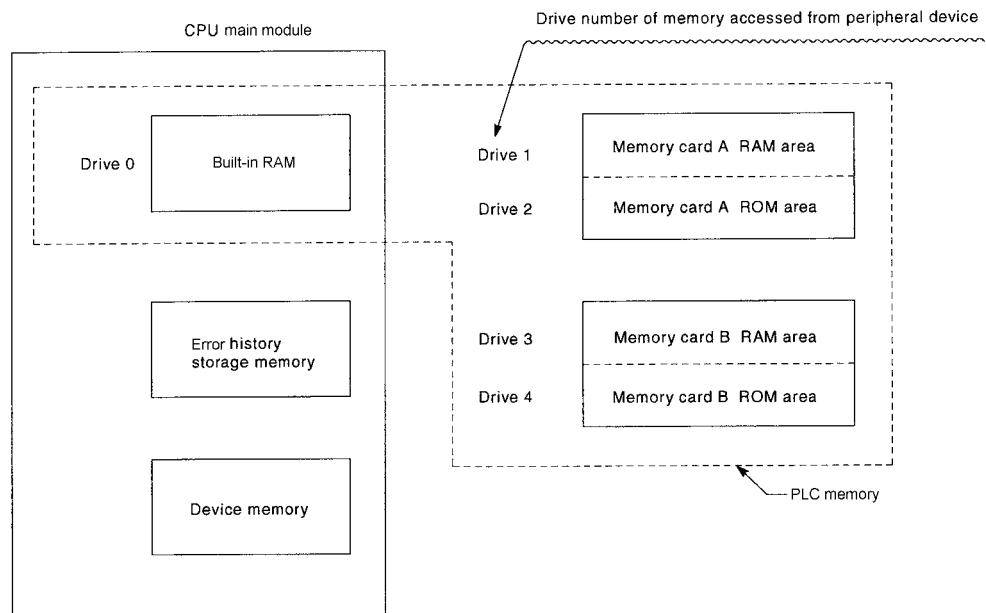
REMARK

The following shows the peripheral devices and software packages that cannot be used with QnACPU:

- A□PU (Programming unit)
- A6WU (ROM writer unit)
- A6DU-B (Data access unit)
- A6TEL (Modem interface unit)
- A6GPP (Intelligent GPP)
- A6HGP (Hand-held graphic programmer)
- A6PHP (Plasma hand-held graphic programmer)
- System start-up software package for ACPU
SW□□□-GPPA, SW□□□-SAP2
- Utility software package for ACPU
SW□□□-GPPATEL, SW□□□-CADIF, SW□□□-DRWA,
SW□□□-FUNP, SW□□□-TSAP2

3.3.3 QnACPU memory block diagram

The following block diagram shows the QnACPU memory configuration.



- Built-in RAM : Memory that stores parameters, sequence programs, etc.
- Error history storage memory : Memory that stores error history data
- Device memory : Memory that stores device data
- Memory card (RAM, ROM area) : Memory that stores the files, comments, etc., for parameters, sequence programs, sampling traces, etc.
- PLC memory : Indicates all the memories of drives 0 through 4.

For file types stored in each memory, refer to "File Types & Storage Destinations of Files Managed by QnACPU" in the QnACPU Programming Manual (Fundamentals).

4 PERFORMANCE SPECIFICATIONS

This section shows the performance specifications of the QnACPU.

Item		Model Name				Remark
		Q2ACPU	Q2ACPU-S1	Q3ACPU	Q4ACPU	
Control method		Sequence program control method				
I/O control mode		Refresh mode				Direct input/output is allowed by specifying direct input/output (DX□, DY□).
Programming language		Language dedicated to sequence control				
		Relay symbol language, logic symbolic language, MELSAP-3 (SFC)				
Processing speed (Sequence instruction)	LD	0.2 μs/steps		0.15 μs/steps	0.075 μs/steps	
	MOV	0.6 μs/steps		0.45 μs/steps	0.225 μs/steps	
Constant scan (Function that makes the scan time constant)		5ms to 2000ms (Possible to set in 5ms units)				Possible to set in the parameters
Memory capacity		Capacity of the installed memory card (Max. 2036k bytes)				
Program capacity	Number of steps	Max. 28k steps	Max. 60k steps	Max. 92k steps	Max. 124k steps	
	Number of files	28 files	60 files	92 files	124 files	
Number of I/O device points		8192 points (X/Y0 to X/Y1FFF)				The number of points usable in the program
Number of I/O points		512 points (X/Y0 to X/Y1FF)	1024 points (X/Y0 to X/Y3FF)	2048 points (X/Y0 to X/Y7FF)	4096 points (X/Y0 to X/YFFF)	The number of accessible points to actual I/O module

4. PERFORMANCE SPECIFICATIONS

MELSEC-QnA

Item		Model Name				Remark	
		Q2ACPU	Q2ACPU-S1	Q3ACPU	Q4ACPU		
Device points	Internal relay [M]	Default: 8192 points (M0 to M8191)				Possible to set the number of points to be used by the parameter	
	Latch relay [L]	Default: 8192 points (L0 to L8191)					
	Link relay [B]	Default: 8192 points (B0 to B1FFF)					
	Timer [T]	Default: 2048 points (T0 to T2047) (Low-speed timers and high-speed timers sharing) Set low-speed timers/high-speed timers switching with instructions. Set low-speed/high-speed measurement units by parameter. (Low-speed timers: 10ms to 1000ms, 10ms units, Default: 100ms) (High-speed timers: 1ms to 100ms, 1ms units, Default: 10ms)					
	Retentive timer [ST]	Default: 0 point (ST0 to ST2047) (Low-speed timers and high-speed timers sharing) Set Low-speed timers/high-speed timers switching with instructions. Set low-speed/high-speed measurement units by parameter. (Low-speed timers: 10ms to 1000ms, 10ms units, Default: 100ms) (High-speed timers: 1ms to 100 ms, 1ms units, default: 10 ms)					
	Counter [C]	• Normal counters Default: 1024 points (C0 to C1023) • Interrupt counters Max. 48 points (Default: 0 point, Can be set by the parameter.)					
	Data register [D]	Default: 12288 points (D0 to D12287)					
	Link register [W]	Default: 8192 points (W0 to W1FFF)					
	Annunciator [F]	Default: 2048 points (F0 to F2047)					
	Edge relay [V]	Default: 2048 points (V0 to V2047)					
	File register [R]	32768 points (R0 to R32767) Up to 1042432 points can be used by block switching.					
		1042432 points (ZR0 to ZR1042431) Block switching is not necessary.					
	Special link relay [SB]	Default: 2048 points (SB0 to SB7FF)				The number of device points is fixed.	
	Special link register [SW]	Default: 2048 points (SW0 to SW7FF)					
	Step relay [S]	8192 points (S0 to S8191)					
	Index register [Z]	16 points (Z0 to Z15)					
	Pointer [P]	4096 points (P0 to P4095), Possible to set Ranges for pointers in files and common pointers by the parameter.					
	Interrupt pointer [I]	48 points (I0 to I47) The fixed-cycle interval for system interrupt pointers I28 to I31 is set by the parameter. (5ms to 1000ms, in 5ms units)					
	Special relay [SM]	2048 points (SM0 to SM2047)					
	Special register [SD]	2048 points (SD0 to SD2047)					
	Function input [FX]	16 points (FX0 to FXF)					
	Function output [FY]	16 points (FY0 to FYF)					
	Function register [FD]	5 points (FD0 to FD4)					
Link direct device		Devices that access link devices directly. Dedicated to MELSECNET/10 Designation format: J □ □ \ □ □ □					

4. PERFORMANCE SPECIFICATIONS

MELSEC-QnA

Item	Model Name				Remark
	Q2ACPU	Q2ACPU-S1	Q3ACPU	Q4ACPU	
Special function module direct device	Devices that directly access the buffer memories of special function modules. Designation format: U□ □\G□ □				
Latch (power failure compensation) range	L0 to L8191 (Default) (Latch ranges can be set for B, F, V, T, ST, C, D, W devices.)				Possible to set in the parameters
Remote RUN/PAUSE contact	Possible to setup one contact point for each of RUN/PAUSE from X0 to X1FFF.				
Clock function	Year, month, day, hour, minute, second, day of the week (automatic detection of the leap year) Accuracy -2.3 to +4.4s (TYP. +1.8s)/d at 0℃ Accuracy -1.1 to +4.4s (TYP. +2.2s)/d at 25℃ Accuracy -9.6 to +2.7s (TYP. +2.4s)/d at 55℃				
Allowable momentary power failure period	Depends on the power supply modules				Refer to Section 16.1.
5VDC internal current consumption*	0.4A	0.4A	0.4A	0.9A	
Weight	0.8kg	0.8kg	0.8kg	0.8kg	
External dimensions	250mm (9.84inch) × 79.5mm (3.13inch) × 121mm (4.76inch)				

REMARK

- * Indicates current consumption of the QnACPU with function version "B" (9707B).
 The following shows the current consumption values of the QnACPU without the function version:
- Q2ACPU, Q2ACPU-S1, Q3ACPU : 0.3A
 - Q4ACPU : 0.6A

5 I/O NUMBER ASSIGNMENT

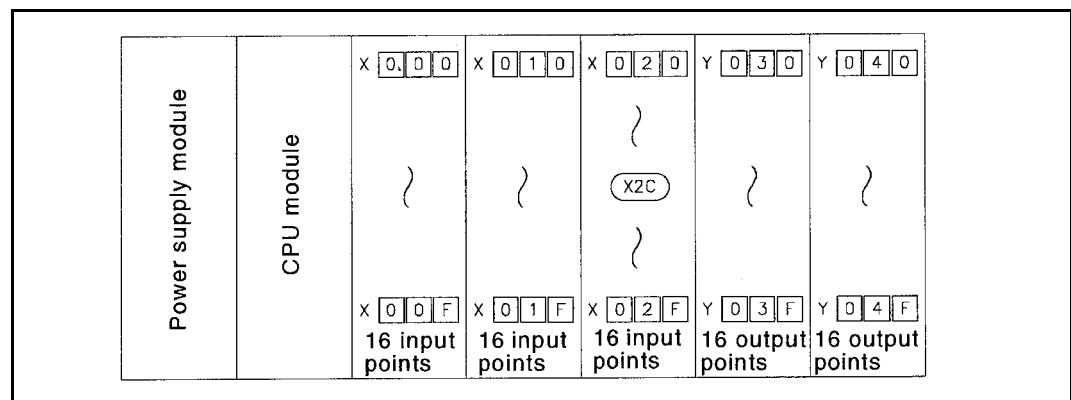
This section explains the method for I/O number assignment using the QnACPU to enable data communications with a I/O modules and a special function module.

5.1 I/O Numbers

The I/O number is used in the sequence program to input data from a input module and to output data to an output module.

The I/O number is expressed as three-digit hexadecimal numbers.

The I/O numbers when all the I/O modules are occupied in 16 points are indicated below.



Concept of I/O numbers

REMARK

When programming with a peripheral device for GPP function, I/O numbers can be input in 2 digits.

I/O numbers Input with a peripheral device

X010 → X10

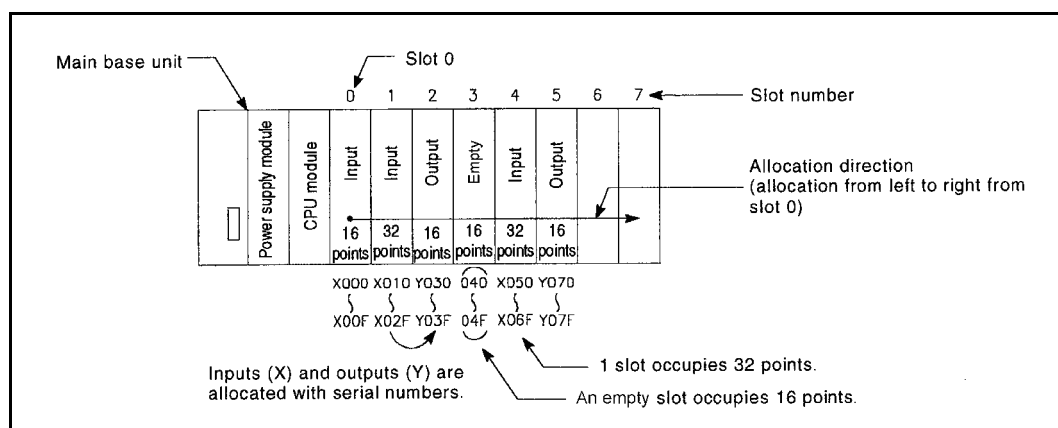
Y020 → Y20

5.2 I/O Number Assignment Concept

When the PLC power is ON or the CPU module is reset, the I/O assignment described below is performed.

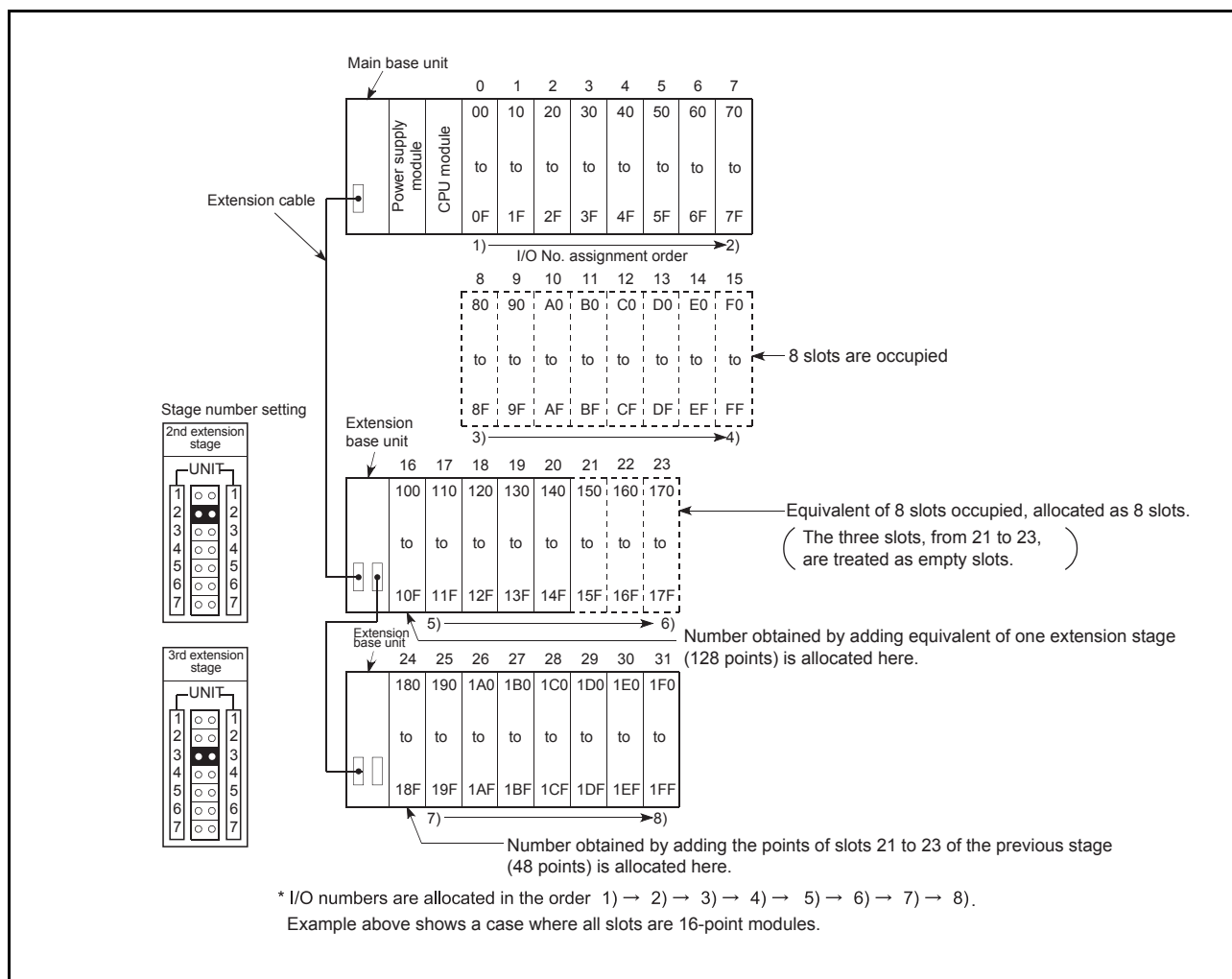
In the sequence program, designate the I/O numbers assigned in accordance with the following.

- (1) I/O numbers are sequentially assigned from left to right, taking slot 0 (The slot to the right of the CPU module) of the main base unit to be "0".
- (2) The I/O modules and special function modules mounted to the main base unit occupy the I/O numbers corresponding to the number of I/O points for each module.
- (3) 16 points are assigned to the empty slots where no I/O module or special function module is mounted.



- (4) If an extension base unit is connected, its assignment starts from the number immediately after the number assigned to a main base unit. The order of assignment for extension base units is not the order in which the extension base units are connected, but the order of the stage numbers set for the extension base units. It is possible to connect extension base units as follows: main base unit → 2nd extension base stage → 1st extension stage.
- (5) If any extension stage number is skipped, I/O points are assigned with assuming that "all the skipped stage × 8 slots" occupy 16 points.

- (6) I/O numbers are assigned assuming that every base unit has 8 slots.
 If a 5-slot type base unit is used, an I/O number obtained by adding points equivalent to 3 slots (48 points) to the final I/O number of the 5-slot base unit is assigned to the next extension base unit.



I/O number assignment example without no extension base on the 1st extension stage

5.3 I/O Assignment with GPP Function

When using the QnACPU, I/O modules and a special function module can be controlled even if I/O assignment with GPP function is not performed.

I/O assignment with GPP function are valid in the following cases.

- (1) The purpose of I/O assignment with GPP function
 - (a) When using a base unit for 5 slots, set 0 point for 3 slots for efficient use of number of I/O points.
 - (b) Reserve the points when changing a module to other than a 16-point module for future system extension.
 - (c) The I/O assignment prevents the I/O numbers from changing if an I/O module or special function module that occupies other than 16 points has to be removed due to failure.
 - (d) The I/O assignment reduces the I/O number modification in a program since it enables to match with the I/O numbers of the designed program and to change the I/O numbers assigned to each module on the base unit per slot.

- (2) The concept of I/O assignment with GPP function

The following two methods are available for I/O assignment with GPP function.

- 1) Set the number of points for the empty slots on a main base and extension base. (Points occupied by empty slot)
- 2) Set the I/O assignment per slot of main base unit or extension base unit to each module type. (I/O assignment)

Parameter settings are used for both of these methods. If both 1) and 2) are set, the setting of 2) takes priority.

- (a) Setting points occupied by empty slot

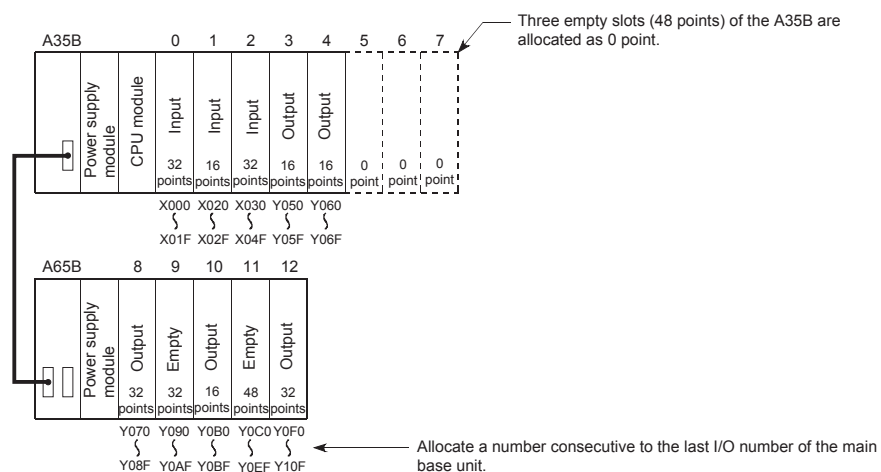
Set the number of points for all slots that are empty on the base unit.

In the systems in which this setting is not made in the parameters, 16 points are set for empty slots.

Make this setting in "7. # of empty slots" on the "PC system" screen in the parameter mode.

[PC System Setting]		Label :
1. Timer Interval	1. Slow [100]ms 2. Fast [10]ms	5. Common Pointer # from [1]
2. RUN-PAUSE Contact	RUN X[] PAUSE X[]	6. General Data Process[1]Unit/try
3. Allow Remote Reset	1.<*) Yes 2.<) No	7. # of Free Slots < 16 >
		8. System Interrupt

The setting is made in units of 16 point within the range of 0 to 64. The default is 16 points.
 Example: When the points occupied by empty slot is set to 0 points



(b) I/O assignment settings

Set the I/O assignment per slot of main base unit or extension base unit to each module type.

Make this setting in the "I/O Allocation" screen in the parameter mode.

[[I/O Allocation]]					Label :
Slot	Type	Items	1stXY	Type Name	
0<0-0>	<Inp>	<32Pt>	[0]	[AX41]	Basic
1<0-1>	<Inp>	<16Pt>	[20]	[AX40]	[A35B]
2<0-2>	<Inp>	<32Pt>	[30]	[AX41]	Power Supply
3<0-3>	<Out>	<16Pt>	[50]	[AY40]	[A61P]
4<0-4>	<Out>	<16Pt>	[60]	[AY40]	Extension Cable
5<0-5>	<Free>	< 0Pt>	[]	[]	[AC12B]
6<0-6>	<Free>	< 0Pt>	[]	[]	
7<0-7>	<Free>	< 0Pt>	[]	[]	
8<1-0>	<Out>	<32Pt>	[70]	[AY41]	Extension 1
9<1-1>	<Free>	<32Pt>	[90]	[]	[A65B]
10<1-2>	<Out>	<16Pt>	[B0]	[AY40]	Power Supply
11<1-3>	<Out>	<48Pt>	[C0]	[]	[A61P]
12<1-4>	<Out>	<32Pt>	[F0]	[AY41]	Extension Cable
13<1-5>	< >	< >	[]	[]	[]
14<1-6>	< >	< >	[]	[]	[]
15<1-7>	< >	< >	[]	[]	[]
PgUp:Prev PgDn:Next					Esc:Close

The setting details are as follows:

Item	Setting	Setting range	Default value
Slot setting	Set data for each slot. (Not necessary to set all data).	Free/input/output/special	No setting
	Type		
	Points	0 to 64 points (in 16 point units)	
	Start XY	0 to 1FFF (in 16 point units)	
	Model name	Up to 16 characters	
Base specification	Set data for each base unit.	Up to 16 characters	No setting
	Power model name		
	Extension cable	Up to 16 characters	

The items without settings are handled as follows:

- Type and Points : In accordance with the loaded module.
- Start XY : The number following the total points obtained by adding the number of points of the modules already set.
If there is any duplication, an error (SP.UNIT LAY ERROR) is detected.

POINT	The power supply module names set in the base specification is only used for the current capacity check in the PLC diagnostics mode and not used for a CPU module. Therefore, even if they are not set, any problem does not occur.

The CPU module performs the following processing when I/O assignment is set.

- 1) Any of the following assignment can be performed per slot of each base unit.

Assigned number of points			
Empty slot	Input module	Output module	Special function module
0	—	—	—
16	16	16	16
32	32	32	32
48	48	48	48
64	64	64	64

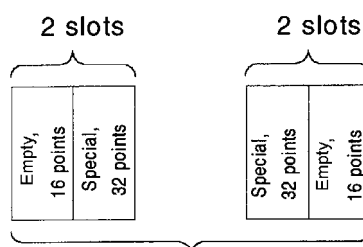
- 2) The slots for which I/O assignment has been performed with GPP function, the I/O assignment setting takes priority regardless of the loaded module.
- If a number of points fewer than the that of the loaded I/O module is set, the actual number of points of the loaded I/O module is reduced.
For example, if the loaded module is a 32-point input module but I/O assignment is set for a 16-point input module using GPP function, the latter 16 points for the input module cannot be used.
 - If a number of points is greater than the that of the loaded I/O module is set, the number of points in excess of the actual number of points is occupied with dummy points.
 - If the slot where an I/O module is loaded is set as a empty slot, the I/O module will be unusable.
- 3) The slots for which I/O assignment is not performed using GPP function are assigned with the number of points of the loaded module.
- 4) The slots for which I/O assignment is not performed using GPP function are assigned I/O numbers that are consecutive to those of modules for which I/O assignment has been performed.

(3) Precautions

- (a) If there is a disparity between the I/O assignment made in the parameter settings and the actually loaded I/O modules, the input and output is not normally performed.

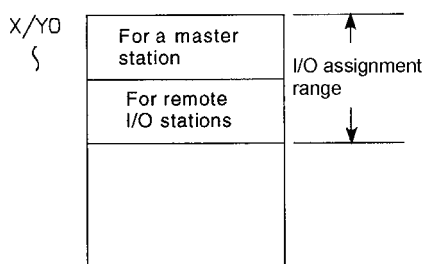
Loaded module	I/O assignment	Result
Input	Output	No input
Output	Input	No output
Input/Output	Special	CPU module error
Special	Input/Output	CPU module error

- (b) The I/O assignment of a slot to which a special function module is loaded has to be the same setting with the module. Not doing so may cause an error.
- 1) A11VC..... Special: 16 points
 - 2) AI61 Special: 32 points
 - 3) AG62..... Input: Set number of points
 - 4) Modules that occupy 2 slots..... Set "Empty, 16 points" and "Special, 32 points".



Refer to the User's Manual for the special function module to use.

- (c) When operating MELSECNET data link, perform I/O assignment as follows.
- 1) As for a master station, I/O assignment has to be performed for the master station and all remote I/O stations.
I/O assignment of MELSECNET (II)/B to the remote I/O station is invalid.



- 2) As for a local station, perform I/O assignment only for the local station.
 - 3) Assign the I/O for the I/O hybrid module (e.g. A42XY) as an output module.
- (d) When the MELSECNET/10 network is established, assign the I/O only for the host station (master station).
Since the I/O assignment of MELSECNET/10 to the remote I/O station is irrelevant, the I/O assignment is not allowed.
For I/O assignment of MELSECNET/10 to the remote I/O station, use the I/O assignment settings in the "Network parameter".

REMARK

As for the remote I/O station of MELSECNET (II)/B, I/O assignment settings in the "Network parameter" is irrelevant, therefore, the I/O assignment is not allowed.

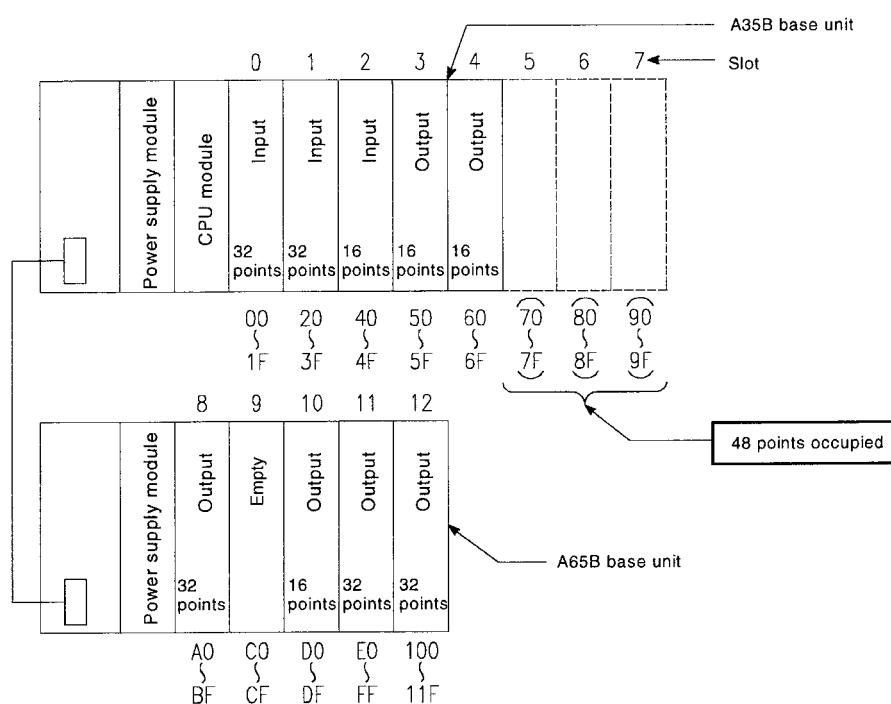
5.4 Example of I/O Number Assignment

The following shows the example of I/O number assignment when I/O assignment is performed using GPP function.

- (1) When changing the assignment for an empty slot from 16 points to 0 or 32 points
When the A35B is used, there are three empty slots. When setting the assignment for these to 0 points in order to increase the number of I/O points that can be used by the CPU module.

When reserving 32 I/O points for a current empty slot to which a 32-point input module is loaded later, in order to prevent the I/O number assignment change.
To achieve these operations, perform I/O assignment as follows.

- (a) Loading status and I/O numbers



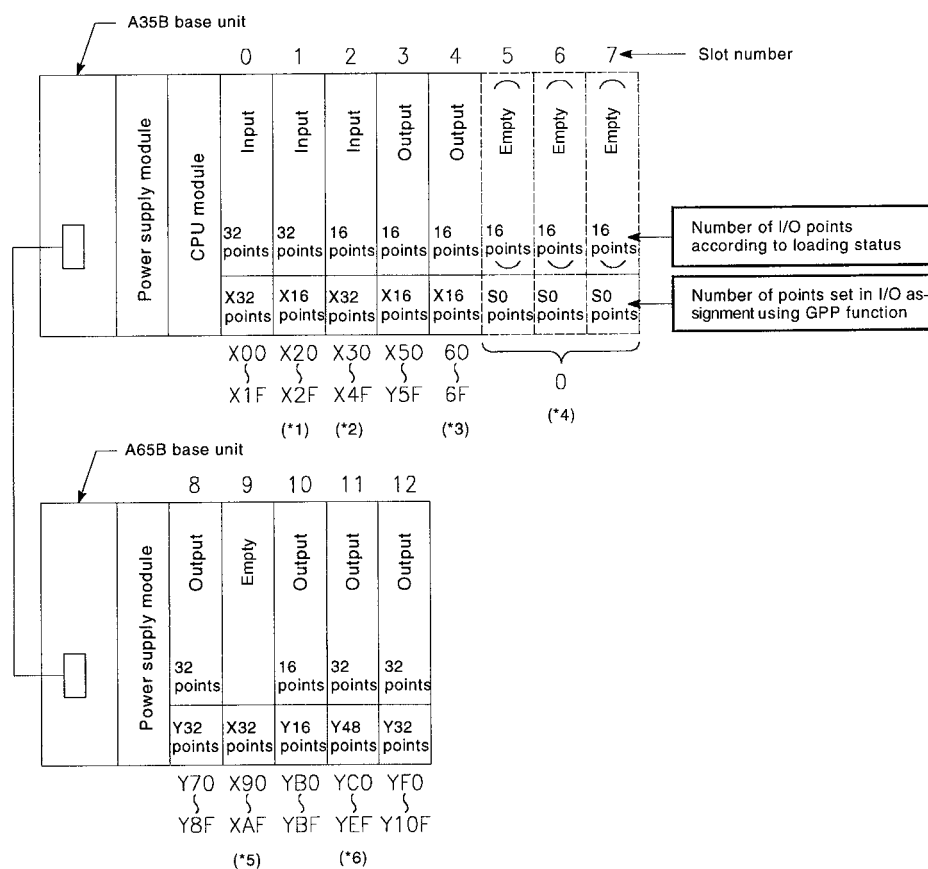
(b) I/O numbers when I/O assignment is performed using GPP function

1) I/O Allocation example

[I/O Allocation]					Label :
Slot	Type	Items	1stXY	Type Name	
0<0-0>	<Inp >	<32Pt>	[01	[AX41	] Basic
1<0-1>	<Inp >	<16Pt>	[201	[AX40	] IA35B]
2<0-2>	<Inp >	<32Pt>	[301	[AX41	] Power Supply
3<0-3>	<Out >	<16Pt>	[501	[AY40	] IA61P]
4<0-4>	<Free>	<16Pt>	[601	[	] Extension Cable
5<0-5>	<Free>	< 0Pt>	[]	[	] IA612B]
6<0-6>	<Free>	< 0Pt>	[]	[	]
7<0-7>	<Free>	< 0Pt>	[]	[	]
8<1-0>	<Out >	<32Pt>	[701	[AY41	] Extension 1
9<1-1>	<Out >	<32Pt>	[901	[AY41	] IA65B]
10<1-2>	<Out >	<16Pt>	[B01	[AY40	] Power Supply
11<1-3>	<Out >	<48Pt>	[C01	[	] IA61P]
12<1-4>	<Out >	<32Pt>	[F01	[AY41	] Extension Cable
13<1-5>	< >	< >	[]	[	] []
14<1-6>	< >	< >	[]	[	]
15<1-7>	< >	< >	[]	[	]
PgUp:Prev PgDn:Next					Esc:Close

The example of I/O assignment with GPP function

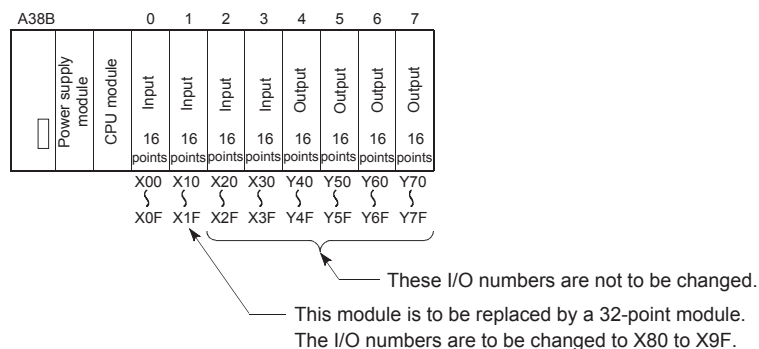
2) I/O numbers after performing I/O assignment using GPP function



(2) Replacing a 16-point input module with a 32-point input module

When replacing the 16-point input module with a 32-point input module without changing the all I/O number assignment in a system to which a 16-point input module is designed. To achieve this operation, perform I/O assignment as follows.

(a) Loading status and I/O numbers before the replacement



(b) I/O numbers when I/O Allocation is performed using GPP function

1) I/O Allocation example

[I/O Allocation]					Label :
Slot	Type	Items	1stXY	Type Name	
0<0-0>	<Inp>	<16Pt>	[01]	[AX40]	Basic
1<0-1>	<Inp>	<32Pt>	[80]	[AX41]	[A38B]
2<0-2>	<Inp>	<16Pt>	[20]	[AX40]	Power Supply
3<0-3>	<Inp>	<16Pt>	[01]	[AX40]	[A61P]
4<0-4>	<Inp>	<16Pt>	[01]	[AX40]	Extension Cable
5<0-5>	<Inp>	<16Pt>	[01]	[AX40]	[
6<0-6>	<Inp>	<16Pt>	[01]	[AX40]	[
7<0-7>	<Inp>	<16Pt>	[01]	[AX40]	[
8<1-0>	<Inp>	<16Pt>	[01]	[AX40]	Extension 1
9<1-1>	<Inp>	<16Pt>	[01]	[AX40]	[
10<1-2>	<Inp>	<16Pt>	[01]	[AX40]	Power Supply
11<1-3>	<Inp>	<16Pt>	[01]	[AX40]	[
12<1-4>	<Inp>	<16Pt>	[01]	[AX40]	Extension Cable
13<1-5>	<Inp>	<16Pt>	[01]	[AX40]	[
14<1-6>	<Inp>	<16Pt>	[01]	[AX40]	[
15<1-7>	<Inp>	<16Pt>	[01]	[AX40]	[
PgUp:Prev PgDn:Next					Esc:Close

The example of I/O assignment with GPP function

2) I/O numbers after performing I/O assignment using GPP function and replacing the module

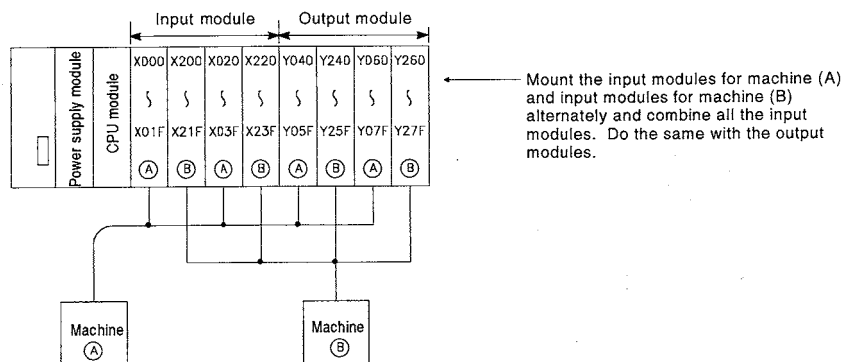
A38B		0	1	2	3	4	5	6	7
	Power supply module								
	CPU module								
		Input	Input	Input	Input	Output	Output	Output	Output
		16 points	32 points	16 points	16 points	16 points	16 points	16 points	16 points
		X00	X80	X20	X30	Y40	Y50	Y60	Y70
		X0F	X9F	X2F	X3F	Y4F	Y5F	Y6F	Y7F

POINT	
When the I/O number set for "Start XY" in the "I/O Assign" is changed, also set the "Start XY" for the next module to avoid changing the I/O numbers of the module for which the change was made and the subsequent modules. In the example above, since "20" is set for the "Start XY" for the second slot, consecutive I/O numbers starting from X30 are set for slot 3 and later.	

- (3) When combining an input module and output module having non-consecutive I/O numbers on a base unit

When controlling the machine ① (I/O numbers X0 to X3F, Y40 to Y7F) and machine ② (I/O numbers X200 to X23F and Y240 to Y27F) with a single PLC, it is desired to combine input modules and output modules on the base unit. To achieve this operation, perform I/O assignment as follows.

(a) Loading status and I/O numbers to be set



(b) The example of I/O Allocation with GPP function

[I/O Allocation]					Label :
Slot	Type	Items	1stXY	Type Name	
0<0-0>	<Inp>	<32Pt>	[0]	[AX41	Basic
1<0-1>	<Inp>	<32Pt>	[200]	[AX41	[A38B
2<0-2>	<Inp>	<32Pt>	[201	[AX41	Power Supply
3<0-3>	<Inp>	<32Pt>	[220]	[AX41	[A61P
4<0-4>	<Out>	<32Pt>	[40]	[AY41	Extension Cable
5<0-5>	<Out>	<32Pt>	[240]	[AY41	[
6<0-6>	<Out>	<32Pt>	[60]	[AY41	
7<0-7>	<Out>	<32Pt>	[260]	[AY41	
8<1-0>	<Inp>	<32Pt>	[1]	[	Extension 1
9<1-1>	<Inp>	<32Pt>	[1]	[	[
10<1-2>	<Inp>	<32Pt>	[1]	[	Power Supply
11<1-3>	<Inp>	<32Pt>	[1]	[	[
12<1-4>	<Inp>	<32Pt>	[1]	[	Extension Cable
13<1-5>	<Inp>	<32Pt>	[1]	[	[
14<1-6>	<Inp>	<32Pt>	[1]	[	
15<1-7>	<Inp>	<32Pt>	[1]	[	

PgUp:Prev PgDn:Next

Esc:Close

6 DATA COMMUNICATIONS WITH SPECIAL FUNCTION MODULES

This chapter explains the methods for reading data from a special function module, and writing data to a special function module with the QnACPU.

The special function module is a module that allows analog quantity, high-speed pulse, etc., which cannot be processed with I/O module alone, to be handled by the QnACPU.

For example, analog quantity is converted to a digital value by an analog/digital converter module (which is a special function module) so that they can be used by the QnACPU.

The special function module has buffer memory in which data input from external sources and data to be output to external destinations are stored.

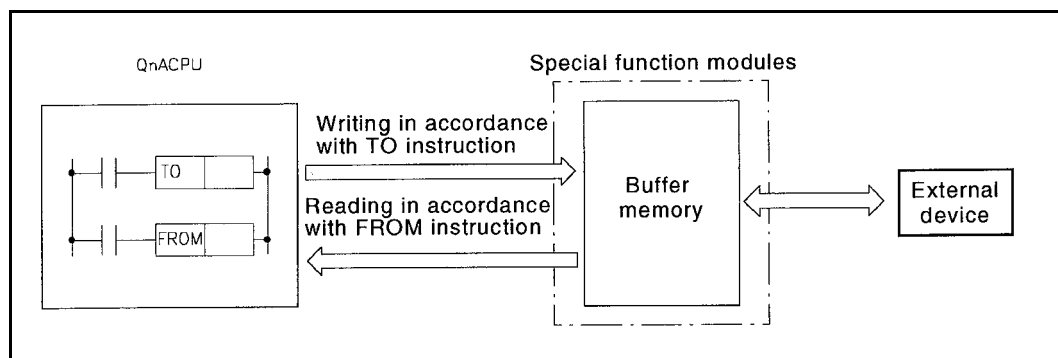
The following two methods are available for reading data from a special function module, and writing data to a special function module with the QnACPU.

- 1) Using the FROM/TO instruction
- 2) Using special direct devices

These methods are explained in the following sections.

6.1 Reading/Writing Data from/to the QnACPU Using the FROM/TO Instruction

When the FROM/TO instruction is performed, data stored in the buffer memory of a special function module is read, or data is written to the buffer memory of a special function module.



Data communications with a special function module

When the FROM instruction is performed, the data read from the buffer memory is stored in the specified device. When the TO instruction is performed, the data in the specified device is written to the buffer memory.

REMARK

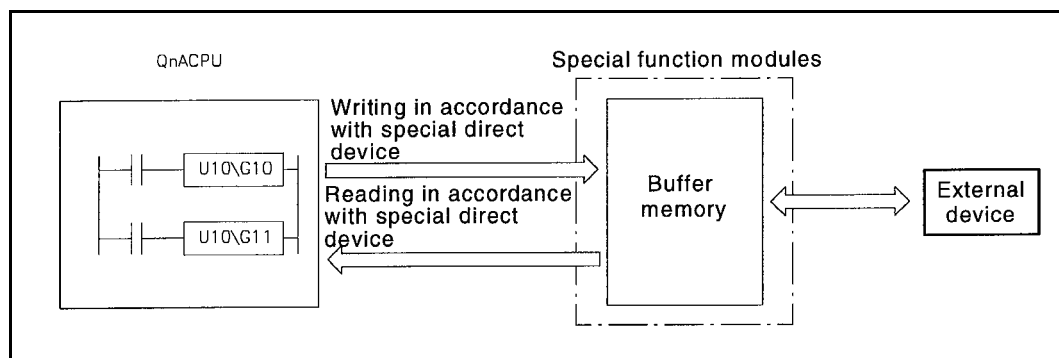
- 1) For details on the FROM/TO instructions, refer to the QCPU (Q mode)/ QnACPU Programming Manual (Common Instructions).
- 2) For details on the buffer memory of a special function module, refer to the manual of the special function module in use.

POINT

When executing the FROM/TO instruction for the special function module frequently in short scan time, it may cause the target special function module operation error.
When executing the FROM/TO instruction, match the processing time and conversion time of the special function module using timer or constant scanning.

6.2 Reading/Writing Data from/to the QnACPU Using Special Direct Devices

As the FROM/TO instruction, the special direct device reads data stored in the buffer memory of a special function module or writes data to the buffer memory of a special function module.



The special direct device represents the buffer memory in a special function module as the QnACPU device.

Example: U10\G10: U10 → Indicates the head I/O No.100 of the special function module. (Hexadecimal)
G10 → Indicates the buffer memory address 10. (Decimal)

REMARK

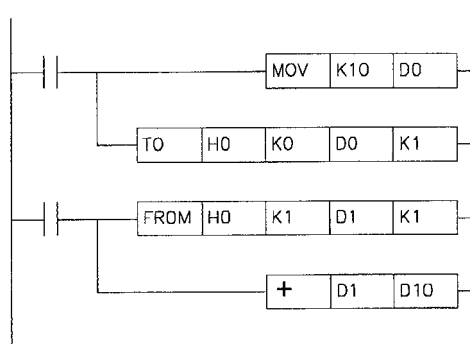
For details on a special direct device, refer to the QnACPU Programming Manual (Fundamentals).

The special direct device differs from the FROM/TO instruction in that the CPU module can handle the buffer memory of a special function module as a direct device.

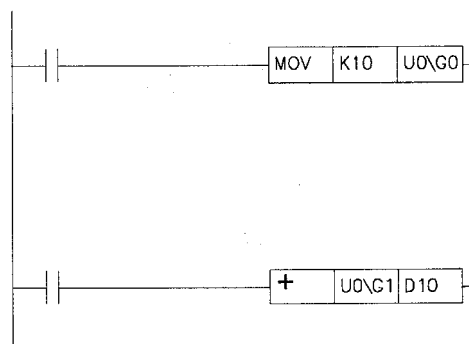
This can reduce the total number of steps in the program. However, the instruction processing speed is the same with the FROM/TO instruction.

Example: Writing data to address 0 of the buffer memory in the special function module loaded at X/Y0, and reading the data of address 1.

(a) Using the FROM/TO instruction



(b) Using special direct device



POINT	
1.	When reading data from the special function module frequently during the programming, store the special direct device to a data register after reading in an area of the program by using the FROM instruction rather than by using them at each instruction. This is because programming scan interval is added due to an access processing to the special function module for each instruction.
2.	When executing the instruction using a special direct device for the special function module frequently in short scan time, it may cause the target special function module operation error. When performing the instruction using a special direct device, match the processing time and conversion time of the special function module using timer or constant scanning.

6.3 Processing for Data Communication Requests from a Special Function Module

When a data communication request is received from a special function module such as a serial communication module, the QnACPU performs the processing for the data communication request at the END processing.

The QnACPU can process all the data communication requests received in one scan with one END processing, according to the parameter settings. In this case, the data lag to each module is eliminated, but the END processing is extended by the data communications request processing.

Data communications request batch processing is set in the "6. General Data Processing" on the "PC system" screen in the GPP function parameter mode.

The setting range is 1 to 6 modules, and the processing can be set per module.

[PC System Setting]		Label :
1. Timer Interval	1. Slow [100]ms 2. Fast [10]ms	5. Common Pointer # from []
2. RUN-PAUSE Contact	RUN X[] PAUSE X[]	6. General Data Process[1]Unit/try
3. Allow Remote Reset	1.<*> Yes 2.< > No	7. # of Free Slots < 16 >
4. Output at STOP→RUN	1.<*> Prior to Calc 2.< > After one Scan	8. System Interrupt
		1. 1st Interrupt Counter C[]
		2. I28 Const Interval[100]ms
		3. I29 Const Interval[40]ms
		4. I30 Const Interval[20]ms
		5. I31 Const Interval[10]ms
Execute<Y> Cancel<N>		
		Space:Select Esc:Close

7 AUTO REFRESH FUNCTION

7.1 For MELSECNET/MINI-S3

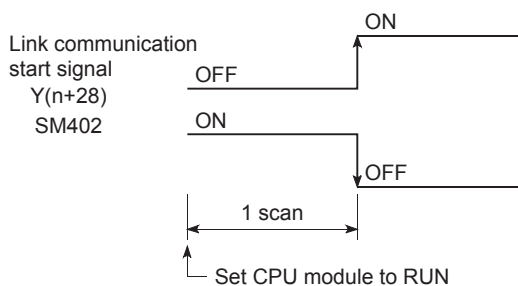
By setting link information, I/O storage device, etc. of the MELSECNET/MINI-S3 to the parameters, the module automatically communicates with the buffer memory area for the batch refresh send/received data of the type AJ71PT32-S3 MELSECNET/MINI-S3 master module (abbreviated as the MINI master module hereafter).

The settings are made on the MELSECNET/MINI setting in the parameter mode of GPP function.

Sequence programs can be created using the I/O devices allocated to send/received by the MELSECNET/MINI-S3 setting. (The FROM/TO instructions are not required.)

POINT

- (1) Since up to 8 master modules can be set for auto refresh by the parameter, auto refresh is possible for up to 8 modules.
When 9 or more modules are desired, use the FROM/TO instruction in the sequence program from the 9th module.
- (2) Since auto refresh is not possible with send/received data for the separate refresh I/O modules and for the remote terminal units No.1 to No.14, use them by the FROM/TO instructions.
However, the remote terminal units shown below are subject of auto refresh in the limited area:
 - AJ35PTF-R2 RS-232C interface module
 - AJ35PT-OPB-M1-S3 mount-type tool box
 - AJ35PT-OPB-P1-S3 portable type tool box
- (3) For the master modules set up for auto refresh, since the QnACPU automatically turns ON the link communication start signal Y(n+18) or Y(n+28), it is not necessary to turn it on from the sequence program.
- (4) Auto refresh of I/O data is performed by the batch after the QnACPU performs the END instruction.
(Auto refresh processing is performed when the CPU module is in the RUN/PAUSE/STEP-RUN status.)
- (5) The master module may perform the processing while the link communication start signal Y(n+18) or Y(n+28) is OFF depending on the remote terminal units connected.
For instance, if the AJ35PTF-R2 RS-232C interface unit is used without protocol, it is necessary to write parameters to the parameter area (buffer memory address 860 to 929) while the link communication start signal is OFF. Since the link communication start signal becomes ON after the CPU module enters the RUN status and one scan is performed, write the parameters during the first 1 scan.



- (6) If the hardware error signal X(n+0) or X(n+20) or ROM error signal X(n+8) or X(n+28) of a master module for which auto refresh has been set comes ON, the QnACPU does not perform auto refresh processing.
- (7) When making the settings, ensure that there is no duplication between receive data refresh devices and send data refresh devices.

- (1) Parameter setting items, setting ranges and contents of auto refresh, as well as the buffer memory address of the master module which is used for exchanging data with the QnACPU are shown below.

Set the parameters for the number of the master modules used.

I/O signal from a master module	Buffer memory address of a master module	Item	Setting range	Description	Default value
—	—	Number of master modules	0, 1 to 8 module(s)	Sets the total number of the master modules used. Set "0" if auto refresh is not to be used.	Follow the settings made in the "I/O Assign" in the parameter mode.*3
—	—	Start I/O No.	Number of I/O points of CPU module	Sets the head I/O number where the master module is installed.	
—	—	Model classification of MINI/MINI-S3	MINI or MINI-S3	- MINI In I/O mode (occupies 32 points) - MINI-S3 In expansion mode (occupies 48 points)	
—	0	Total number of remote I/O stations	0 to 64 stations	- Set only when MINI is set. - In MINI-S3, since the number of master module's initial ROMs becomes valid, the setting is not necessary. (When the setting is executed, ignore it).	
—	110 to 141	Storage device for received data *4	- X - M, L, B, T, ST, C, D, W, R, ZR, none (Bit device: multiples of 16)	- Sets the devices to store the received/send data for batch refresh. - Specify the head number of the device. - The total number of remote I/O stations, set starting from the first device number, is occupied as a auto refresh area. (8 points/station × 64 stations = 512 points...: Bit device)² - Use of X/Y remote I/O range is recommended for devices.	X1000 to X11FF
—	10 to 41	Send data storage device	- Y - M, L, B, T, ST, C, D, W, R, ZR, none (Bit device: multiples of 16)		Y1000 to Y11FF
—	1	Number of retries	0 to 32 times	- Sets the number of retries upon the communication errors occurrence. - Error is not output when the communication is restored within the number of the retries set.	5 times
Y(n+1A)*1	—	FROM/TO response specification	Link priority; CPU priority (Priority selection of access to the master module buffer memory)	1) Link priority - Link access by MINI-S3 has the priority. During the link access, FROM/TO is caused to wait. - Possible to read out the received data refreshed at the same timing. - The maximum wait time (0.3ms + 0.2ms × number of separate refresh stations) for the FROM/TO instruction may be generated. 2) CPU priority - The FROM/TO instructions from a CPU module are given access priority. Even during the link access, it interrupts and accesses. - Depending on the timing, received data in the midst of I/O refresh may be read. - No wait time for the FROM/TO instruction.	CPU priority
Y(n+1B)*1	—	Data clear specification for communication faulty station	Retention, clear (received data)	- Retention Retains the received data for batch and separate refresh. - Clear Sets all points to OFF	Clear

I/O signal from a master module	Buffer memory address of a master module	Item	Setting range	Description	Default value
—	100 to 103 195	Faulty station detection	M, L, B, T, ST, C, D, W, R, ZR, none (Bit device: multiples of 16)	- Sets the head device to store the faulty stations detected data. - MINI occupies 4 words; MINI-S3 occupies 5 words.	No setting
—	107 196 to 203	Error No.	T, ST, C, D, W, R, ZR	- Sets the head device to store the error code at the error occurrence. - MINI occupies 1 word; MINI-S3 occupies (1 + Number of remote terminal modules) words.	No setting
—	4	Line error check setting (Line error)	- Test message sending (Test) - OFF data sending (OFF) - Immediate data transmission before line errors (Retention)	Sets data sending method for verification of faulty area when the line errors occur.	Retention
—	—	Operation at CPU STOP	Stop/Continue	Sets the operating status when the CPU module is in the STOP state.	Stop

*1 "n" is determined by the installation location of the master modules.

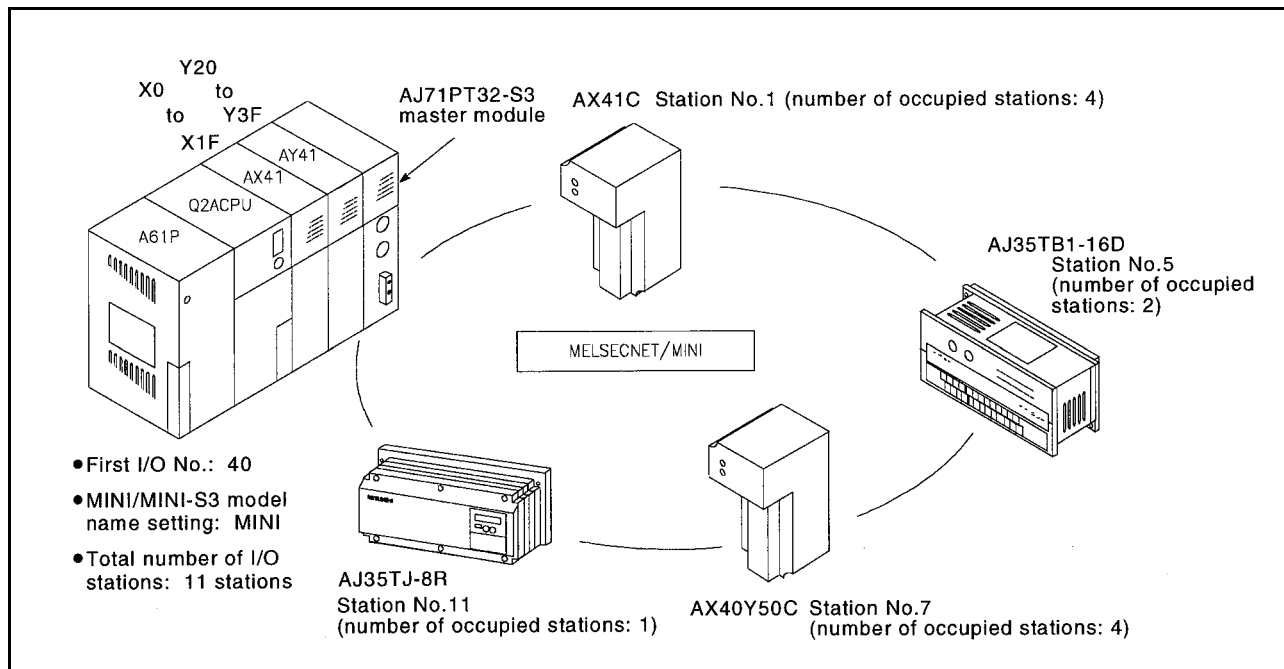
*2 When the total number of remote I/O station is odd, add 1 to the station number to obtain the occupied storage devices.

*3 When the master module number setting column is made blank in parameter setting, auto refresh can be used without this setting.
However, model name registration is required in the "I/O Assign". (MINI mode: AJ71PT32, MINI-S3 mode: AJ71PT32-S3)

*4 When the input (X) is specified in the received data storage device, use the I/O number later than the number used for the module loaded on the main base unit and the extension base unit. When the I/O number usage range for the module loaded on the main base and the extension base is used for input/output of the received data storage device, the CPU module imports both the input ON/OFF data from the input module and the ON/OFF data from auto refresh of MELSECNET/MINI-S3. Therefore, input (X) of the CPU module is not operated as desired.

- (2) Setting of the send/received data storage devices is explained using the system example shown below.

(Example) When the device X/Y400 and later are used as the remote I/O stations:



Sample parameter setting of the GPP function for the above system configuration is shown below:

[MELSECNET/MINI Setting]

1. Master Unit [1] Unit< >

Execute<Y> Cancel<N>

Esc:Close

➔

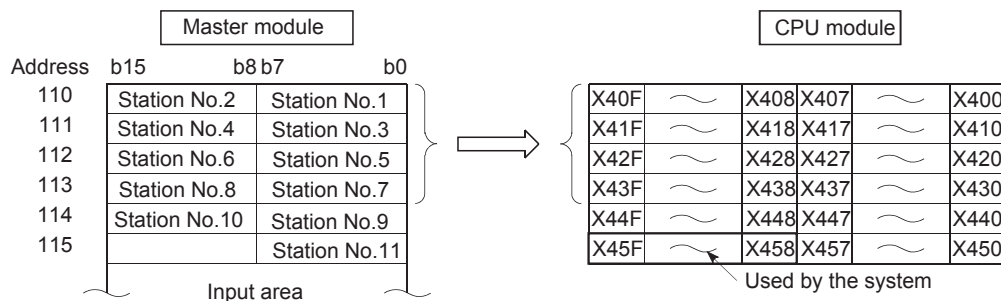
[MELSECNET/MINI Setting List]

Label :

Unit	1st I/O #	Type	Status	Batch Refresh RX Data	Batch Refresh TX Data	Reply	Reply	Clr Err Data	Fault Detection Bit Data	Sta Error / Remote Error #	Loop Error Chk	Act at Stop
1	40	S3	11	X400	Y400	5	CPU	Clr			Stor	Paus

The storage devices for the send/received data for the present system example are as follows:

(a) Storage device for received data

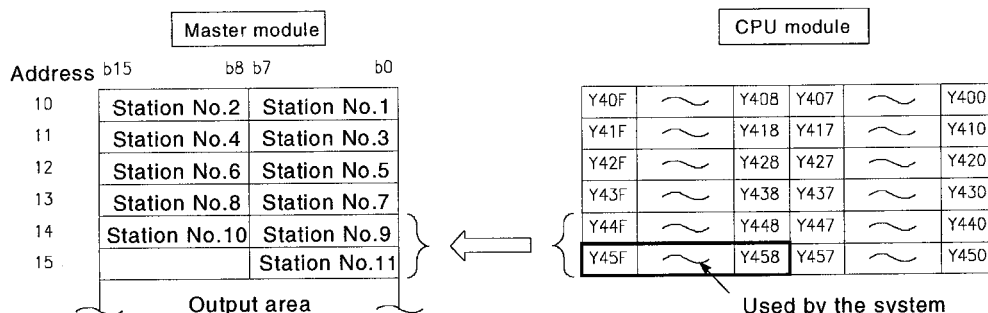


- 1) Set the device number (X400) for b0 of the station 1 as a received data storage device.
- 2) The received data storage device occupies from X400 to X45F.
For the present system example, since the total number of stations is odd, it is occupied for one extra station.
- 3) The device numbers of input modules connected are as follows:

Stations 1 to 4	AX41C	→	X400 to X41F
Stations 5 and 6	AJ35TB-16D	→	X420 to X42F
Stations 7 and 8	AX40Y50C	→	X430 to X43F

With respect to X440 to X45F, they are simultaneously refreshed, and set to OFF at any time.
Do not use X440 to X45F in the sequence program.

(b) Send data storage device



- 1) Set the device number (Y400) for b0 of the station 1 as a send data storage device.
- 2) The send data storage device occupies from Y400 to Y45F.
For the present system example, since the total number of stations is odd, it is occupied for one extra station.
- 3) The device numbers of output modules connected are as follows:
 Station 9 to 10 AX40Y50C → Y440 to Y44F
 Station 11 AJ35TJ-8R → Y450 to Y45F
 With respect to Y400 to Y43F and Y458 to Y45F, they are simultaneously refreshed, but are not output.

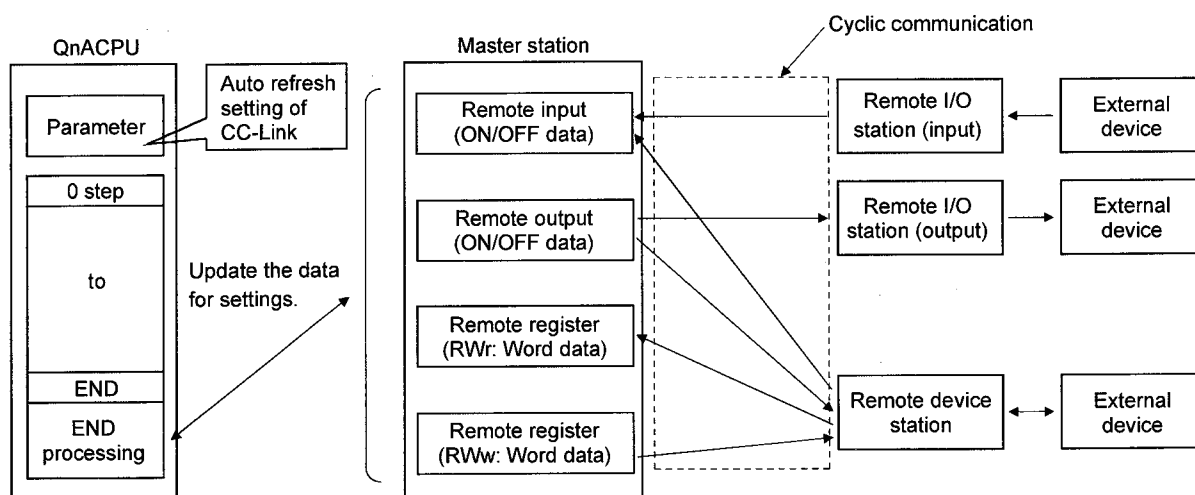
POINT												
(1) If the same device type is used for the send data storage devices and received data storage devices, make sure that there is no duplication of device numbers. When the received data storage device is set to B0 in the system configuration example, it occupies B0 to B5F as the device range. Set the send data storage device to B60 or later. When the send data storage device is set to B60, the device range will be B60 to BBF.												
(2) If a bit device is specified as the send/received data storage device, the device number set must be a multiple of 16. Example: <table><tr><td>(</td><td>X0, X10, ...</td><td>X100, ...</td><td>)</td></tr><tr><td>(</td><td>M0, M16, ...</td><td>M256, ...</td><td>)</td></tr><tr><td>(</td><td>B0, B10, ...</td><td>B100, ...</td><td>)</td></tr></table>	(	X0, X10, ...	X100, ...	)	(	M0, M16, ...	M256, ...	)	(	B0, B10, ...	B100, ...	)
(	X0, X10, ...	X100, ...	)									
(	M0, M16, ...	M256, ...	)									
(	B0, B10, ...	B100, ...	)									
(3) Device range used is (8 points) × (Number of stations). When the number of stations is an odd number, extra 8 points are necessary.												
(4) When specifying input (X) for the received data storage device, specify the device number out of the actual input (X) range.												

7.2 Auto Refresh Setting of CC-Link

Auto refresh of the CC-Link designates automatic communications between the QnACPU and the buffer memory for cyclic communication of CC-Link master stations/local stations. Data for communication varies depending on the remote station connected.

- Remote I/O station (Communication in ON/OFF data)
- Remote device station (Communication in ON/OFF data and Word data)
- Intelligent device station (Communication in ON/OFF data and Word data)
- Master station/local station (Communication in ON/OFF data and Word data)

The auto refresh setting of the CC-Link allows communication with other stations of CC-Link using the FROM/TO instruction without communicating with the master station of the CC-Link.



(1) Settings for auto refresh

The Table 7.1 shows the setting items for auto refresh parameters of the QnACPU.

Table 7.1 List of auto refresh settings

Item	Description	Setting range	Setting station		
			M	L	T
Number of modules	The number of CC-Link modules is set.	1 to 8	○	○	○
Module head I/O number	The head I/O number of a CC-Link module is set.	0000H to 0FE0H	○	○	○
Module type	The loaded CC-Link module type (Master station, local station, stand-by station) is set.	• M: Master station • L: Local station • T: Stand-by station	○	○	○
Receiving data batch refresh bit device (Input data)	• The device that stores the batch refresh received data from the remote station is set. • When the head device number is set, the points corresponding to the specified number of stations (Total number of stations) are obtained to refresh all areas. The output module area is also refreshed. • The settings are made in units of 16 points.	X, M, L, B, T, ST, C, D, W, R, ZR*	○	○	○
Transmission data batch refresh bit device (Output data)	• The device that stores the batch refresh send data to the remote station is set. • When the head device number is set, the points corresponding to the specified number of stations (Total number of stations) are obtained to refresh all areas. The input module area is also refreshed. • The settings are made in units of 16 points.	X, M, L, B, T, ST, C, D, W, R, ZR*	○	○	○
Receiving data batch refresh word device (Remote device: RWr)	• The device that stores the batch refresh received data from the remote station is set. • When the head device number is set, the points corresponding to the specified number of stations (Total number of stations) are obtained to refresh all areas. The I/O module area is also refreshed. • The settings are made per point.	M, L, B, T, ST, C, D, W, R, ZR*	○	○	○
Transmission data batch refresh device (Remote device: RWw)	• The device that stores the batch refresh send data to the remote station is set. • When the head device number is set, the points corresponding to the specified number of stations (Total number of stations) are obtained to refresh all areas. The I/O module area is also refreshed. • The settings are made per point.	M, L, B, T, ST, C, D, W, R, ZR*	○	○	○
Receiving buffer specification for transient station	• The receive buffer capacity for transient station is set.	80 to 4096	○	×	×
Transmission buffer specification for transient station	• The send buffer capacity for transient station is set.	80 to 4096	○	×	×
Batch refresh device for special relay	• The destination device for special relay is set.	M, L, B, T, ST, C, D, W, R, ZR*	○	○	○

* Only when the file register is set to "Use the designated file" with the "Parameter", R and ZR can be used as the auto refresh devices.

When "Use same file name as program" is set, R and ZR cannot be used.

REMARK

- 1) In "Setting station" in the table above, M refers to the master station, L to the local station, and T to the stand-by station.
- 2) In the table above, ○ means that the setting can be made and × means that the setting is not required.

Table 7.1 List of auto refresh settings (Continued)

Item	Description	Setting range	Setting station		
			M	L	T
Batch refresh device for special register	• The destination device for special register is set.	T, ST, C, D, W, R, ZR*	○	○	○
Auto update buffer specification	• The buffer capacity for automatic update is set.	128 to 4096	○	×	×
Total number of slave stations	• The last station number of the remote station connected to the master station is set.	1 to 64	○	×	×
Delay timer	• The delay time of link scan is set.	1 to 100 (0 is invalid.)	○	×	×
Standby station specification	• The use status of the stand-by master function is set.	• Not used • Used	○	×	×
Number of retries	• The number of retries at the occurrence of a transient transmission error is set.	1 to 7	○	×	×
Number of automatic return stations	• The number of automatic return stations is set to one link scan.	1 to 10	○	×	×
Operation specification for CPU stop	• When the CPU module has stopped, continuation/stop of the data link is set.	• Stop • Continue	○	×	×
Scan mode setting	• Synchronization/Non-synchronization is set to the CPU module scan.	• Non-synchronization • Synchronization	○	×	×
Station type	• The model for each remote station is set.	• Remote I/O station • Remote device station • Intelligent device station	○	×	×
Number of occupied stations	• The number of occupied stations for each remote station is set.	• 1 station • 2 stations • 3 stations • 4 stations	○	×	×
Specification of reserved station	• Reservation for remote station is set.	• Not reserved • Reserved	○	×	×
Specification of invalid station	• Validity/Invalidity for error detection of the remote station is set.	• Invalid • Valid	○	×	×

* Only when the file register is set to "Use the designated file" with the "Parameter", R and ZR can be used as the auto refresh devices. When "Use same file name as program" is set, R and ZR cannot be used.

REMARK

- 1) In "Setting station" in the table above, M refers to the master station, L to the local station, and T to the stand-by station.
- 2) In the table above, ○ means that the setting can be made and × means that the setting is not required.

(2) Precautions

- (a) Auto refresh of the CC-Link is available when the QnACPU and the CC-Link module with function version "B" are used.
When either of the QnACPU or the CC-Link module does not indicate function version "B," auto refresh of the CC-Link is not available.
- (b) Auto refresh can be set to up to 8 CC-Link modules.
When 9 or more CC-Link modules are used, handle with the FROM/TO instruction of the sequence program for the 9th module or later.
- (c) When both the CC-Link module and the master station module for MELSECNET/MINI-S3 are loaded and auto refresh is not set, the default parameter is set to the master station module for MELSECNET/MINI-S3.
- (d) The COM instruction or the G(P).ZCOM instruction allows auto refresh to the CC-Link module while performing the sequence program.
However, auto refresh to the CC-Link module cannot be performed with the J(P).ZCOM instruction. Error code "4102" (The network number designated with the dedicated network instruction does not exist) appears.
- (e) Refresh operation for the mixture of MELSECNET (/10, /II) and MELSECNET/MINI-S3.
- Refresh is performed in the order of MELSECNET (/10, /II), CC-Link and MELSECNET/MINI-S3.
Therefore, the input data specifying the same range is afterward overwritten with the executed data.
 - The output data is output to the MELSECNET (/10, /II), CC-Link, and MELSECNET/MINI-S3.
- (f) The operation of the QnACPU when the CC-Link module is in the online/offline mode is shown in the table below:

Parameter settings for auto refresh	CC-Link module status	Operation of the QnACPU
Set	Online	The communications with the remote station is performed with the specified parameter for auto refresh.
	Offline	The QnACPU does not generate an error, but does not communicate with the remote station.
Not set	Online	The communications with the remote station is performed by the FROM/TO instruction.
	Offline	The QnACPU does not generate an error, but does not communicate with the remote station.

- (g) Auto refresh setting to the CC-Link is performed using the following peripheral devices.
- Personal computer:
GX Developer, SW2IVD-GPPQ type GPP function software package

(3) Setting method

Auto refresh setting to the CC-Link is set with the following procedures.

- (a) When the "CC-Link" is selected in the "Parameter", the "CC-Link setting" screen appears.

[CC-Link setting]

1. Number of modules []

Execute(Y) Cancel(N)

Esc: Close

Set the number of the CC-Link modules (1 to 8).

- (b) Set the number of the CC-Link modules loaded on the main base unit and extension base unit for the QnACPU and select "Execute", then the screen of CC-Link setting list appears.

Module number setting for refresh setting

[CC-Link setting]

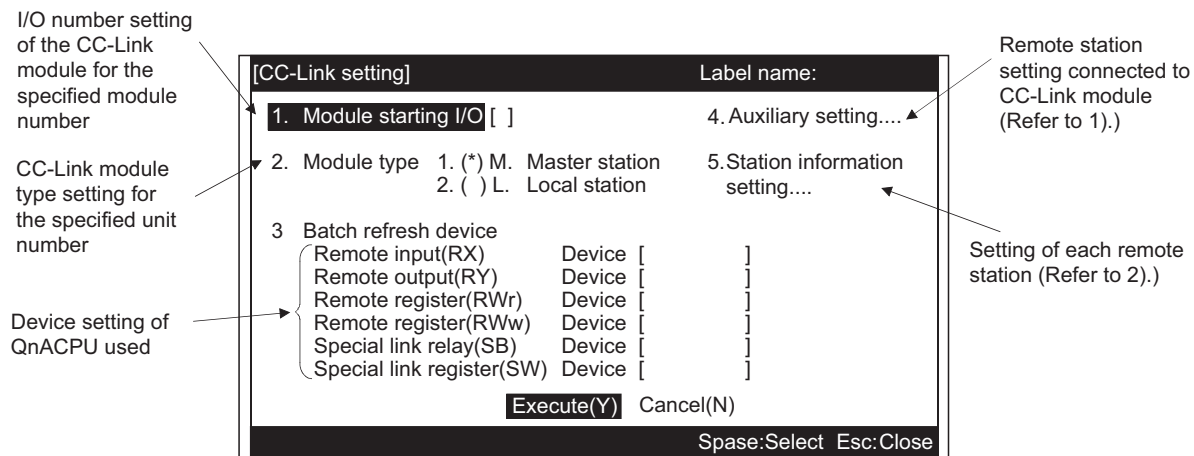
Module	Starting I/O No.	Type	Batch refresh device					
			Remote input (RX)	Remote output (RY)	Remote register (RWw)	Remote register (RWw)	Special relay (SB)	Special register (SW)
1		M						

Esc: Finished

Confirmation of settings (Press **F3** key for setting.)

Pressing the **Esc** key registers the set data.

- (c) Move the cursor to the module number position for auto refresh setting and press the **F3** key (Detail). The "CC-Link setting" screen appears. Select "4. Auxiliary setting...." and "5. Station information setting...." to set detailed data.



When pressing the Execute (Y) or the **Esc** key , the screen returns to the screen of CC-Link setting list.

- 1) When selecting the "4. Auxiliary setting....", the "Auxiliary setting" screen appears.

When pressing the Esc key, the screen returns to the CC-Link setting screen of (c).

Set the number of remote stations connected to the CC-Link module.

[Auxiliary setting]		Label name:
1. Total number of connected stations [64]	5. Number of automatic return stations [1]	
2. Delay timer [0] X0.05ms	6. Operation specified for CPU fault	
3. Standby station specification [0]	1. () Continue	
	2. (*) Stop	
	7. Scan mode specification	
	1. () Synchronous	
	2. (*) Asynchronous	
4. Number of retries [3]		
Spase: Select Esc: Close		

- 2) When selecting the "5. Station information setting...", the "Station information setting" screen appears.

When pressing the Esc key, the screen returns to the CC-Link setting screen of (c).

Set the number of stations specified in 2).

[Station information setting]				Label name:		
Station No.	Station type	Number of occupied stations	Reserved/invalid station	Intelligent buffer specification (word)		
				Send	Receive	Auto
1	< I/O >	< 1 >	< >	[---]	[---]	[---]
2	< I/O >	< 1 >	< >	[---]	[---]	[---]
3	< I/O >	< 1 >	< >	[---]	[---]	[---]
4	< I/O >	< 1 >	< >	[---]	[---]	[---]
5	< I/O >	< 1 >	< >	[---]	[---]	[---]
6	< I/O >	< 1 >	< >	[---]	[---]	[---]
7	< I/O >	< 1 >	< >	[---]	[---]	[---]
8	< I/O >	< 1 >	< >	[---]	[---]	[---]
9	< I/O >	< 1 >	< >	[---]	[---]	[---]
10	< I/O >	< 1 >	< >	[---]	[---]	[---]
11	< I/O >	< 1 >	< >	[---]	[---]	[---]
12	< I/O >	< 1 >	< >	[---]	[---]	[---]
Spase:Select Esc:Close						

8 DEBUGGING FUNCTION

8.1 Function List

QnACPU has a variety of convenient functions when debugging.
The following shows the debugging functions.

Item	Description	Reference
Monitor function	Function that reads CPU programs, device statuses from a peripheral device capable of GPP functions	Section 8.2
Write during RUN	Function that writes a program while the CPU module is running	Section 8.3
Execution time measurement	Functions that displays the processing time of a program being execute	Section 8.4
Program monitor list	Functions that displays the processing time of a program being executed	Section 8.4.1
Interrupt program monitor list	Function that displays the number of executions of an interrupt program	Section 8.4.2
Scan time measurement	Function that measures the execution time of section of a program	Section 8.4.3
Sampling trace function* ¹	Function that continually collects the data of devices in accordance with a timing set at the CPU module	Section 8.5
Status latch function* ¹	Function that collects the device data at the moment to designate	Section 8.6
Step operation	Functions that runs one step or one part of a program, runs a program with a part skipped	Section 8.7
Step execution	Function that runs a program step by step	Section 8.7.1
Partial execution	Function that executes a designated part of a program	Section 8.7.2
Skip execution	Function that executes a program with a designated part skipped	Section 8.7.3
Program trace function* ¹	Function that collects the program execution status	Section 8.8
Simulation function* ²	Function that simulats execution in isolation from the I/O modules and special function modules	Section 8.9
Debugging by several people	Function that simultaneously debuggs from several peripheral devices capable of GPP functions	Section 8.10
Monitoring trace function	Function that collects device data at a peripheral device capable of GPP functions in accordance with the designated timing	—

For details on the operation for each function, refer to the GPP function Operating Manual.

*1 When executing this function, a memory card is required.

*2 When executing part of this function, a memory card is required.

8.2 Monitor Function

This function reads CPU module programs and device statuses to a peripheral device capable of GPP functions.

Application

This function is used to set monitoring conditions for monitoring the operating statuses of the PLC in accordance with a precise timing.

There are three "Monitoring Condition" as follows.

- Executing a monitoring at END processing.
- Setting the step number to be monitored and the step conducting status.
- Setting the device status.

This function is used to retain the monitoring screen by setting "Monitor stop condition setup" in accordance with a precise timing.

When monitoring the CPU module marked Function version B using a peripheral device capable of GPP function, local device monitor test is executed by setting "local device monitor".

8.2.1 Monitoring condition setting

Function Description

- (1) This function allows setting of the monitoring condition.
All operations are performed using Monitor/test menu in the ladder mode.
The following shows an example of setting a monitor condition.

The screenshot displays the [Monitoring Condition] screen with the following content:

```

[Monitoring Condition]
1.< > Monitor Always.
2.<*> Condition
  1.[*] Device      1.< > Word Device [      ]   Device      Current Value
                   2.<*> Bit Device  [Y70]      1= [      ]
                   2.[*] Step #    [ 100]= < ↑ >  1= < ↑ >
                                     Execute<Y>   Cancel<N>
                                     Space:Select Esc:Close
  
```

The following shows an explanation of the screen above:

The monitoring condition can be select either "1. () Monitor Always." or "2. () Condition".

- (a) When "1. () Monitor Always." is set

The collection timing for monitor data is every scan after END processing at the CPU module.

(b) When "2. () Condition" is set

"1. [] Device" and "2. [] Step #" can be set.

1) When only "2. [] Step #" is set

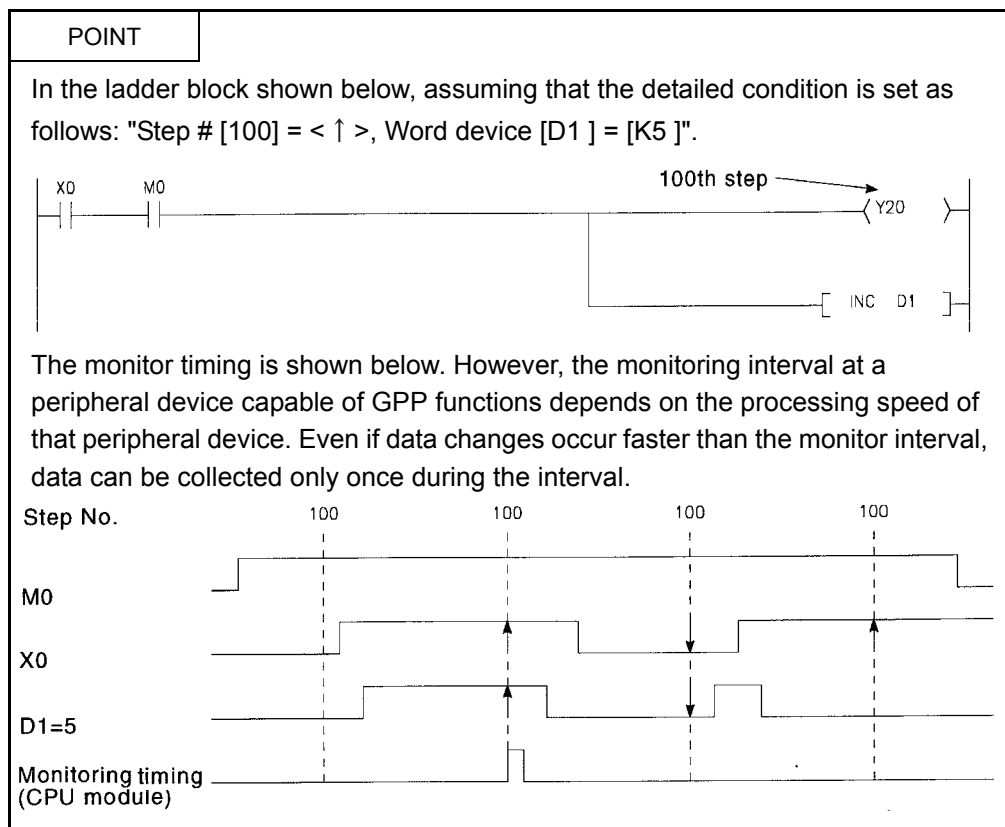
The monitor data collection timing is the moment when a QnACPU shows designated status immediately before executing the designated step.

The following shows the possible designations to execute.

- When switching from OFF to ON: :< ↑ >
- When switching from ON to OFF: :< ↓ >
- All the time only during ON :< ON >
- All the time only during OFF :< OFF >
- All the time in any statuses :< Always >

REMARK

- 1) When Step # [0] is designated, the execution condition must be set as Always.
- 2) When "1. [] Device" only is specified (when "2. [] Step #" is not specified), the monitor data collection timing is every scan after END processing of the PLC CPU. When the data is changed in the same scan, it cannot be detected. (Including the low-speed program)
- 3) When only "1. [] Device" is set, either
"1. () Word Device" or "2. () Bit Device" can be designated.
 - ① When "1. () Word Device" is designated
The collection timing of the monitor data is the scan END processing when the current value of the specified word device becomes the specified value.
The following shows the method for designating the current value.
 - Decimal designation: [K Decimal number]
 - Hexadecimal designation: [H Hexadecimal number]
 - ② When "2. () Bit Device" is designated
The collection timing of the monitor data is the scan END processing when the execution status of the specified bit device becomes the specified status.
The following shows the possible designations for execution status.
 - At leading edge :< ↑ >
 - At trailing edge :< ↓ >
- 4) When "2. [] Step #" and "1. [] Device" are designated
The monitor data collection timing is such that data is collected when the status immediately before execution of the designated step or the execution status (current value) of the designated bit device (word device) attains the designated status.



POINT

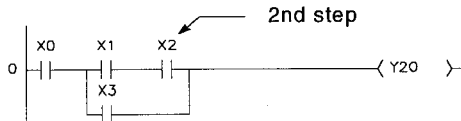
(1) Assume that "Step # [2] = <ON>" is designated as the detailed condition in the case of the ladders shown below; In this case the monitor execution differs for the two ladders. For (a) it is "X0 and X1 both ON" and for (b) it is "X1 ON (regardless of ON/OFF status of X0)".

If a step part way through an AND/OR block is designated for a monitor condition, the monitor data collection timing is such that data is collected when the status immediately before execution of the step designated from the LD instruction in the block becomes the designated status.

Ladder mode

List mode

(a) 

(b) 

0	LD	X0
1	AND	X1
2	AND	X2
3	OUT	Y20

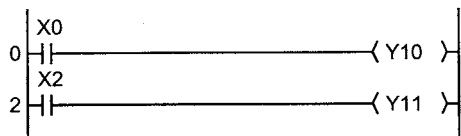
0	LD	X0
1	LD	X1
2	AND	X2
3	OR	X3
4	ANB	
5	OUT	Y20

(2) If the ladder block head other than 0 step is specified to the step number as detailed conditions, the monitor data is collected when the instruction execution status immediately before execution is the specified status.

When "Step # [2] = <ON>" is specified in the ladder below, the monitor data is collected for OUT Y10 ON.

Ladder mode

List mode



0	LD	X0
1	OUT	Y10
2	LD	X1
3	OUT	Y11

- (2) A monitor stop condition can be set.
 All operations are performed on the monitor/test screen window in the ladder mode.
 The following shows an example of the setting for a monitor stop condition.

[Monitor Stop Condition]			
1. < > Without Monitor Stop			
2. <*> Condition	Device	Current Value	
1. [*] Device	1. < > Word Device [	]= [	]
	2. <*> Bit Device [Y71	]= < ↑ >	
2. [] Calculation State < Always>			
Execute <Y>		Cancel <N>	
Space:Select Esc:Close			

The following shows an explanation of the screen above:

Either "1. () Without Monitor Stop" or "2. () Condition" can be set for the monitor stop condition.

- (a) When "1. () Without Monitor Stop" is set

Monitoring is stopped when Esc key is pressed.

- (b) When "2. () Condition" is set

"1. [] Device" and "2. [] Calculation State" can be set.

- 1) When "2. [] Calculation State" is set

The monitor stop timing is such that monitoring stops when the execution condition of the step designated for the monitor condition attains the designated status.

The following shows the possible designations for execution status.

- When switching from OFF to ON : < ↑ >
- When switching from ON to OFF : < ↓ >
- All the time only during ON : < ON >
- All the time only during OFF : < OFF >
- All the time in any statuses : < Always >

If "2. [] Calculation State" isn't set, the timing for monitor stop is such that monitoring is stopped after CPU module END processing.

- 2) When "1. [] Device" is set Either
 "1. () Word Device" or "2. () Bit Device" can be set.

① When "1. () Word Device" is set

The monitor stop timing is such that monitoring stops when the present value of the designated word device attains the designated value.
 The following shows the method for designating the current value.

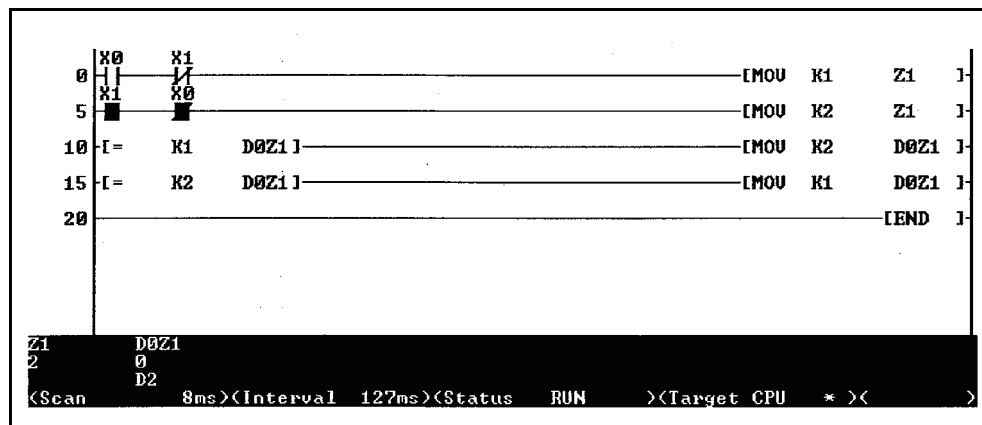
- For decimal (word) designation : [K]
- For hexadecimal (word) designation : [H]
- For decimal (double word) designation: [K L]
- For hexadecimal (double word) designation : [H L]
- For real number designation : [E]

② When "2. () Bit Device" is designated

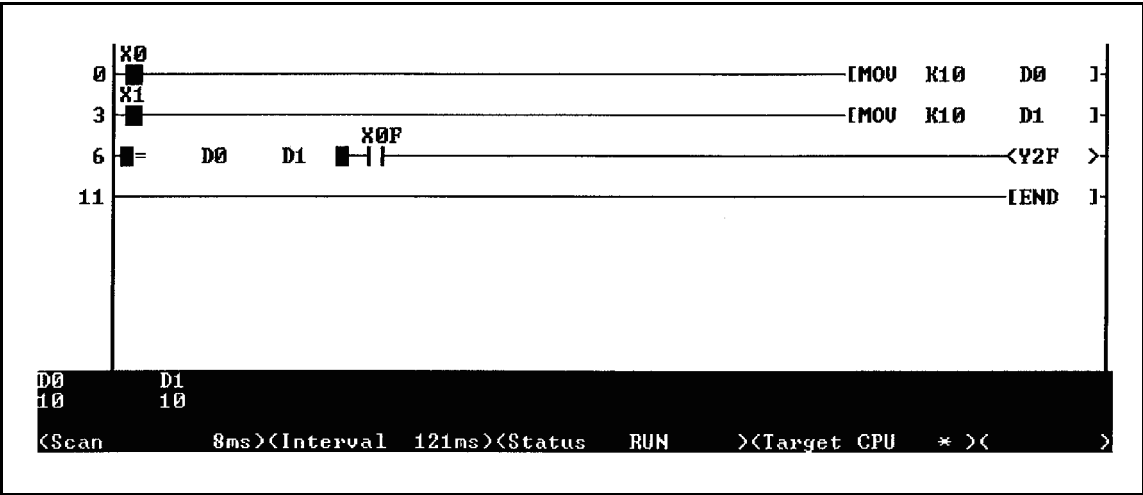
The monitor stop timing is such that monitoring stops when the execution status of the designated bit device becomes the designated status.
 The following shows the possible designations for execution status.

- At leading edge : < ↑ >
- At trailing edge : < ↓ >

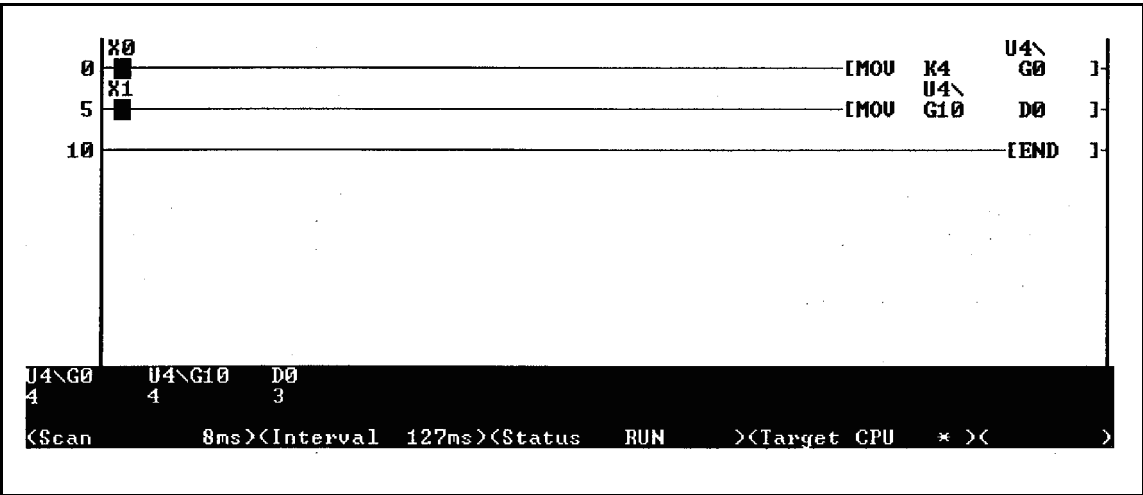
- (3) In the case of devices for which index qualifications have been made, the index qualified value is monitored.
 The following shows an example of this type of monitoring.



- (4) The ON status of comparison instructions can be monitored.
The following shows an example of this type of monitoring.



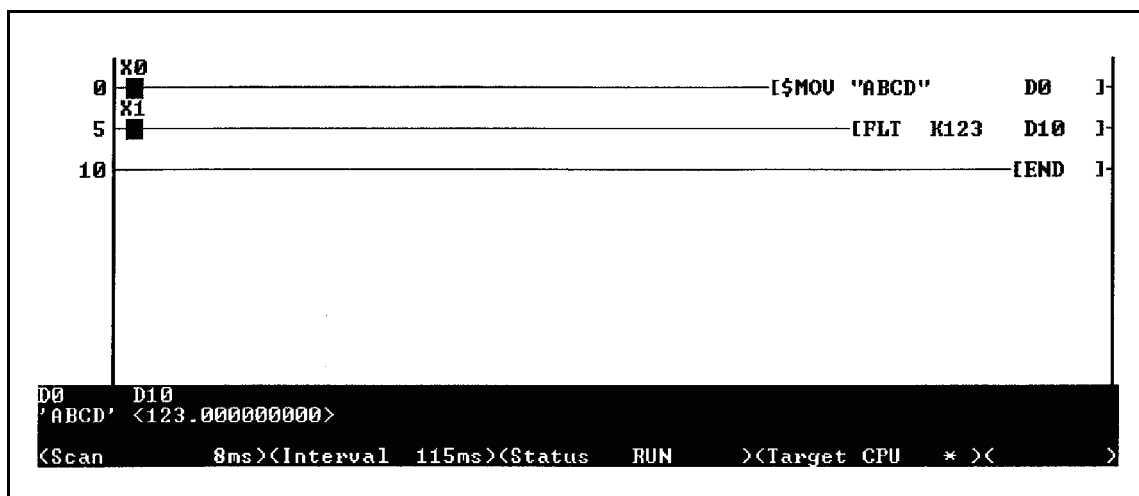
- (5) The devices of special function modules can be monitored.
The following shows an example of this type of monitoring.



REMARK

To monitor devices of special function modules, set "2. Buffer Memory 1. Monitor" for "5/Monitor Target Setting" under the ladder mode "Option" menu.

- (6) Real numbers and character strings can be monitored.
The following shows an example of this type of monitoring.



- (7) The following shows the devices that can be monitored.
- (a) Bit devices : X, FX, DX, Y, FY, DY, M, L, F, SM, V, B, SB, T(Contact), T(Coil), ST(Contact), ST(Coil), C(Contact), C(Coil), J□\X, J□\Y, J□\B, J□\SB, BL□\S
- (b) Word device : T(Current value), ST(Current value), C(Current value), D, SD, FD, W, SW, R, Z, ZR, U□\G, J□\W, J□\SW
- (8) The following shows the setting device under the detailed condition.
- (a) Bit device : X, FX, Y, FY, M, L, F, SM, V, B, SB, T(Contact), ST(Contact), C(Contact), J□\X, J□\Y, J□\B, J□\SB, BL□\S
- (b) Word device : T(Current value), ST(Current value), C(Current value), D, SD, FD, W, SW, R, Z, ZR, U□\G, J□\W, J□\SW

The following qualifications are possible with respect to the devices listed above.

- Digit designation for bit devices
- Bit number designation for word devices

NOTE

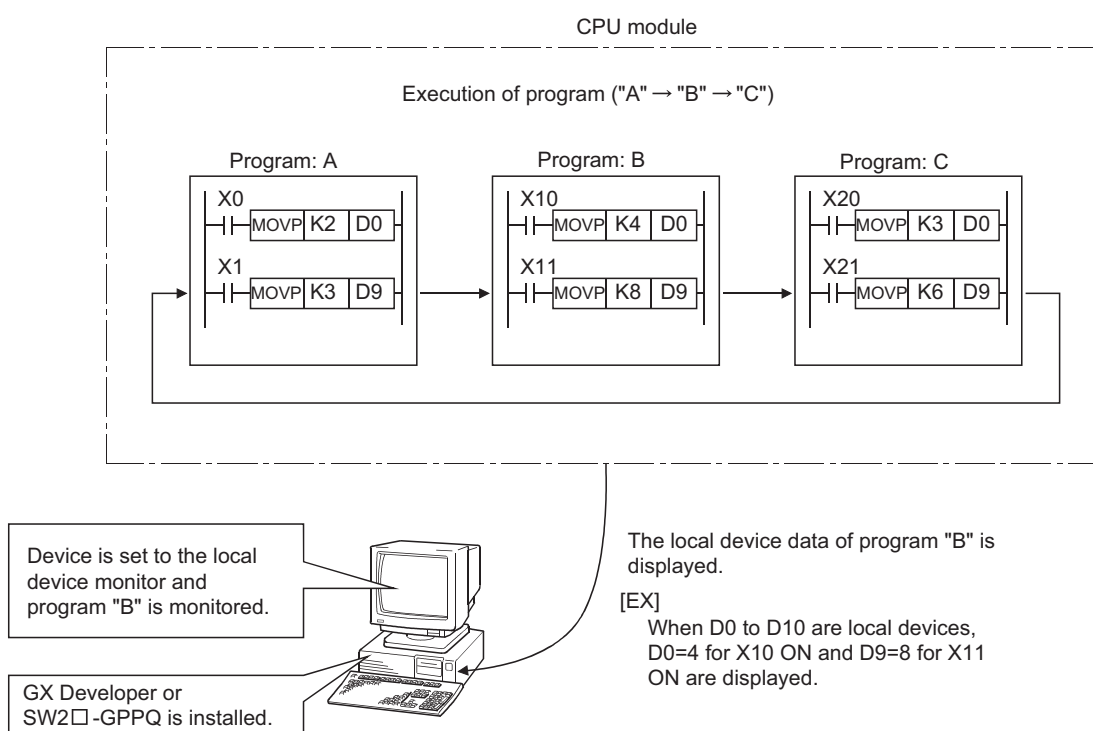
- 1) When a monitoring is performed with a monitor condition set, the file displayed at the device running GPP function is monitored.
Make sure that the file name used with GPP function is the same as the file name when monitoring is performed by executing "Newly from PLC".
- 2) When the buffer memory of a peripheral device is read by designating a direct device, FFFFH is monitored if the peripheral device is faulty or not connected.
- 3) When monitoring file registers, FFFFH is monitored if no file register designation is made.
- 4) Before monitoring, make sure that the device assignment of the CPU and GPP function agree.
- 5) For the local device monitor in each program file, the monitor operation varies depending on presence of the CPU module function version B and the GPP function model.
[Without function version B]
 - Detailed conditions (step number and device condition) are set for each program file to perform monitoring.
[With function version B]
 - When the GX Developer and the SW2IVD-GPPQ are used, the local device can be monitored in each program file by setting compatibility with local device.(Refer to Section 8.2.2.)
 - When SW0IVD-GPPQ and SW1IVD-GPPQ are used, the local device can be monitored with the same operation as the operation without function version B.
- 6) When monitoring the buffer memory of a special function module, the scan time is prolonged in the same way as it is when a FROM/TO instruction is executed.
- 7) Several people can perform monitoring at the same time.
The following considerations apply when executing this:
 - High-speed monitoring can be made possible by increasing the system area by 1k steps for each monitor for other station use when formatting the built-in RAM.
In the monitor for other stations, 15k steps maximum can be set in the system area and the corresponding file space for the user is reduced.
 - Only one person can set the detailed conditions for monitoring.
- 8) The detailed conditions for monitoring can only be set in ladder monitoring.
- 9) If the same device is designated for both a monitor condition and monitor stop condition, also designate the "ON" or "OFF" status.
- 10) When the step number is specified for the monitor condition, monitor conditions are not satisfied for no execution of the applicable step instruction as shown below:
 - Applicable step instructions are skipped by CJ, SCJ and JMP instructions.
 - The applicable instruction is the END instruction and the FEND instruction exists in the program.
- 11) Do not reset the CPU module while the monitor condition is registered.

8.2.2 Monitor test of local device (function version B or later)

With the "parameter device setting," the device set in the local device can be monitored and tested in the peripheral device.

This function allows debugging while checking details of the local device by peripheral devices.

To monitor the local device, set the peripheral device to "local device monitor". The following fig. is an example that monitoring the local device of program B with the CPU module, which is executing programs A, B and C.



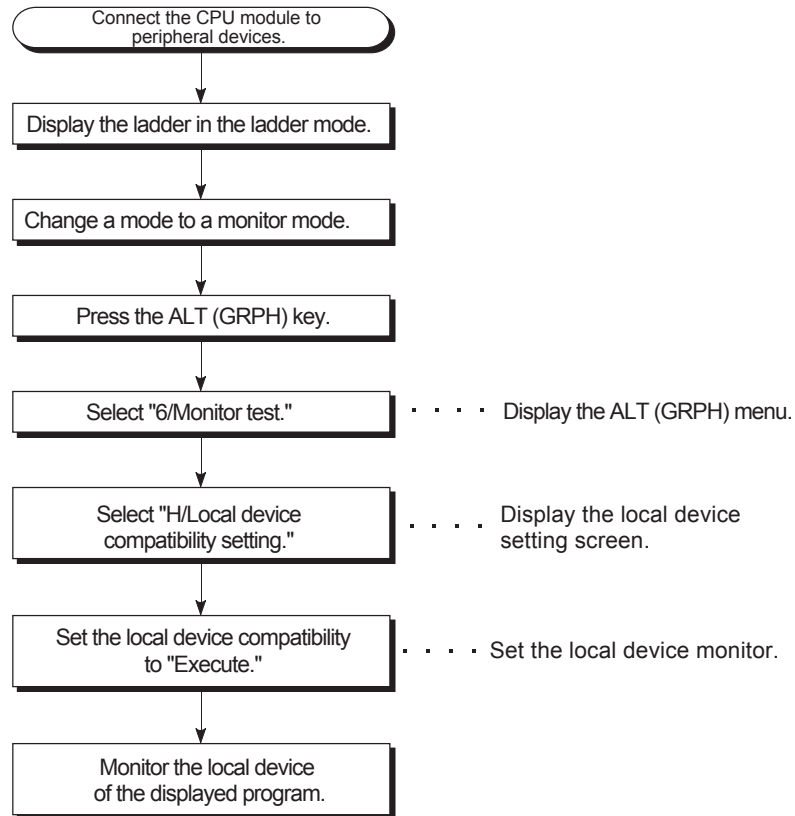
(1) Peripheral device

To perform monitor test of the local devices, the following GPP function software packages are required:

- Personal computer
GX Developer, SW2IVD-GPPQ type GPP function software package

(2) Monitoring procedures of local device

The following shows the procedures to be monitored local devices:



(3) Operation for CPU module and GPP function versions

Table 8.1 shows the operation when the local devices are set to D0 to D99 and when 3 programs with the program names of "A", "B" and "C" are performed in the CPU module.

(The order of the programs is A, B, C, (END processing), A, B...)

Table 8.1 Operation for CPU module and GPPQ function versions

GPPQ Model Name		Monitor Device			
		With Function Version "B"		Without Function Version "B"	
		D0	D100	D0	D100
SW0□-GPPQ SW1□-GPPQ		D0 of program "C" is monitored.	D100 after execution of program "C" is monitored.	D0 of program "C" is monitored.	D100 after execution of program "C" is monitored.
SW2□-GPPQ	When local device is not set	D0 of program "C" is monitored.	D100 after execution of program "C" is monitored.	D0 of program "C" is monitored.	D100 after execution of program "C" is monitored.
	When local device is set	D0 of the displayed program is set.	D100 after execution of the displayed program is set.	An error (error code: 4001) occurs.	

REMARK

GX Developer supports functions of function version B.

(4) Precautions

- (a) The local device that can perform the monitor test in one peripheral device is only one program.

Monitor test for multiple program local devices from one peripheral device is not allowed.

- (b) The number of programs that allows simultaneous monitor test from multiple peripheral devices is up to 16.

When the local device of the stand-by type program is monitored, the local device data is read/escape. The scan time is extended as follows:

- Q2ACPU(S1) : $560 + 1.3 \times (\text{Number of words in the local device}) [\mu\text{s}]$
- Q3ACPU : $425 + 1.0 \times (\text{Number of words in the local device}) [\mu\text{s}]$
- Q4ACPU : $220 + 0.8 \times (\text{Number of words in the local device}) [\mu\text{s}]$

8.3 Write During RUN

This is a function that writes a program to the CPU while the CPU module is in the RUN.

**CAUTION**

- Read the manual carefully and confirm safety before changing the program during operation.
An operation error of write during run may result in damage to the machine or accident.

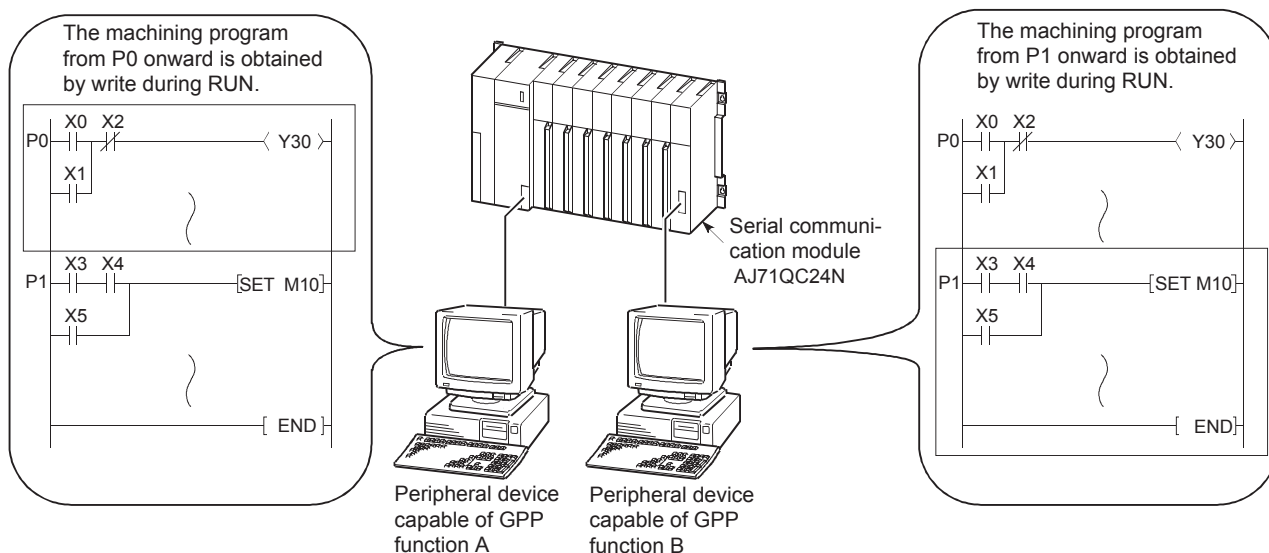
Application

This function is used to change a program without stopping program execution.

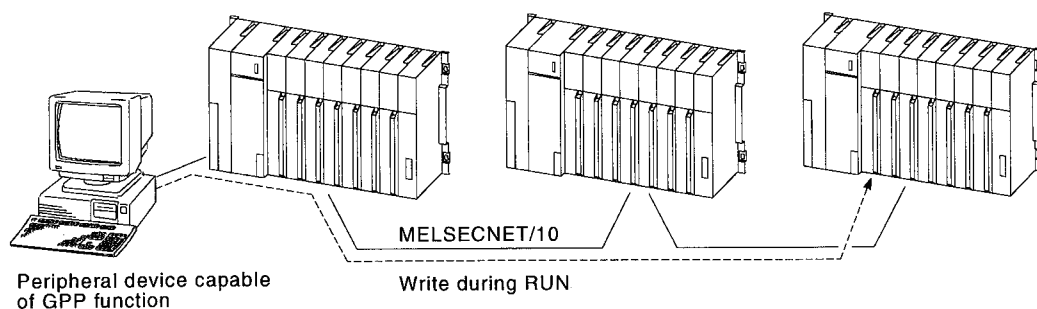
Function Description

- (1) Write during RUN is possible from multiple peripheral devices capable of GPP functions with respect to one file.
In order for this, designate the pointer for the programs to be written from the peripheral devices capable of GPP functions in advance. This enables write safely during RUN using peripheral devices capable of GPP functions.

The example below shows a case where peripheral device capable of GPP functions A performs write during RUN from P0, and peripheral device capable of GPP functions B performs write during RUN from P1. The program enclosed in the frame  is the program subject to write during RUN.



- (2) It is possible to write programs from peripheral devices capable of GPP functions that are connected to other stations in the network during the RUN.



Operation Procedures

To write from the GPP function peripheral devices during RUN, the following two methods are available:

- (1) After a ladder is created in the ladder mode, write during RUN is performed by pressing + keys for conversion of the ladder.
- (2) With "4. Write/conversion setting" in "8/ Option" menu of the ladder mode, "4. Write setting during RUN" and "7. Write method during RUN" are set.

When the key is pressed for conversion of the ladder after the ladder is created, write during RUN is performed.

The following shows the setting examples:

[Write and conversion setting]	
4. Write setting during RUN	1. (*) After conversion, PC is written during RUN. 2. () After conversion, PC is written if PC is STOP. 3. () After conversion, PC is not written.
7. Write method during RUN	1. (*) Write during normal RUN 2. () Write during relative RUN with pointer

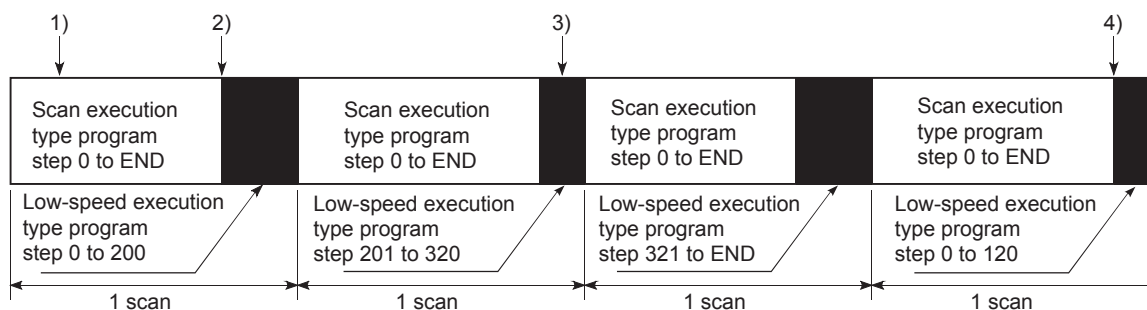
- (a) In "4. Write setting during RUN," "1. () After conversion, PLC is written during RUN" is set.
- (b) In "7. Write method during RUN," "1. () Write during normal RUN" or "2. () Write during relative RUN with pointer" is selected.

NOTE

The following shows the precautions relating to write during RUN.

- (1) The only memory that can be used for write during RUN is the built-in RAM. If write during RUN is performed during a boot operation, also write the program to the memory card at STOP.
When the boot operation is started again without write on the memory card, the program before write during RUN is transferred from the memory card to the built-in RAM for execution.
- (2) The maximum number of steps that can be handled in one write during RUN operation is 512.
The number can be changed according to how many steps of write during RUN saved using a peripheral device capable of GPP function. The saved steps of write during RUN can be set during the CPU module OFF. Note that the saved steps of write during RUN decrease every time write during RUN is performed.

- (3) During low-speed program execution, write during RUN is started when execution of all low-speed programs is completed. Also, execution of low-speed programs is suspended during write during RUN.



- 1): Write during RUN command of scan execution type program
 2): Write during RUN execution of scan type program
 3): Write during RUN command of low-speed execution type program
 4): Write during RUN execution of low-speed execution type program

POINT	
Write during RUN cannot be performed on the program in step operation.	

8.4 Execution Time Measurement

This is a function that displays the processing time of the program being executed.

Application

This function is used to determine the influence of the processing time of each program on the total scan time when making system adjustments.

Function Description

Execution time measurement provides the following three functions. For explanations of each function, refer to Section 8.4.1 through Section 8.4.3.

- Program monitor list
- Interrupt program monitor list
- Scan time measurement

8.4.1 Program monitor list

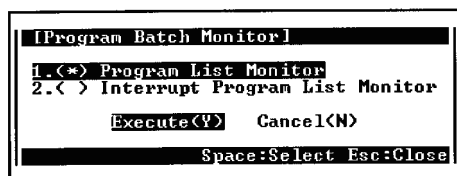
This is a function that displays the processing time of the program being executed.

Function Description

The scan time, execution count, and processing time for each item can be displayed for each program.

All operations are performed using Monitor/test menu in the ladder mode.

- (1) Select "Program Batch Monitor".



- (2) Select "Program List Monitor".

The following shows an example of execution of the program list monitor when a constant scan time of 120ms is set.

(c)

(a)

[Program List Monitor]

<Total Scan Time>

<Program Status>

	Mon Time	Max Scan
Scan	200ms	120.000ms
Init	ms	120.000ms
Slow	ms	0.200ms

#	Program	Exec	Scan Time	Ex Times
1	INITIAL	Init	0.100ms	1 x
2	MACHINE	Scan	0.100ms	1400 x
3	ASSEMBLY	Scan	0.100ms	1400 x
4	TRANSFER	Scan	0.100ms	1400 x
5	TEST	Wait	0.000ms	0 x
6	MONITOR	Slow	0.300ms	57221 x
7		Wait	0.000ms	0 x
8		Wait	0.000ms	0 x
9		Wait	0.000ms	0 x
10		Wait	0.000ms	0 x
11		Wait	0.000ms	0 x

(b)

<Time Details / Scan>

Program	0.300ms
END Proc Time	119.700ms
Slow Prog	110.600ms
Wait for Con	112.200ms

PgUp:Prev PgDn:Next

Esc:Close

The following shows an explanation of the screen above:

- (a) "Total Scan Time"

The times set in "5.() PC RAS Setting" for monitor time and scan time total are displayed here for each program type.

- 1) "Mon Time"

The monitor times for scan execution type programs, initial execution type programs, and low-speed execution type programs are displayed here.

If the scan time exceeds the time displayed here, a watchdog timer error occurs at the CPU module.

- 2) "Max Scan"

The total time for the items listed under "Time Details / Scan" is displayed here.

- (b) "Time Details / Scan"

The scan time details are displayed here.

- 1) "Program"

The total execution time of scan execution type programs is displayed here.

- 2) "END Proc Time"

The END processing time is displayed here.

- 3) "Slow Prog"

When an execution time for low-speed execution type programs is set, the total execution time for low-speed execution type programs is displayed here.

- 4) "Wait for Con"

When constant scan is set, the constant scan waiting time is displayed here. However, if an execution time for low-speed execution type programs is also set, 0.000 ms is displayed.

(c) "Program Status"

The times set in "9. () Auxilliary Setting" in the parameter mode are displayed here.

1) "Program"

The program names are displayed here in the order that the parameters are set.

2) "Exec"

The types of the programs set in the parameters are displayed here.

3) "Scan Time"

The actual scan times (current values) are displayed here. In the program stop (stand-by) status, 0.000ms is displayed as the scan time.

4) "Ex Times"

The number of execution times is displayed here, taking the point at which measurement was started to be 0 in the count (When reaching the maximum times of 65536, the count returns to 0). The number of execution times is retained even when program execution is stopped.

When the subroutine program/interrupt program of the stand-by program is performed in the subroutine call/interrupt request, the number of the stand-by program is not counted.

- (3) Both start () and stop () of the program can be performed on Program monitor list screen.

(a) Start of program ()

Either "Scan execution" or "Low-speed execution" can be set for the stand-by program.

When the key is pressed, the window below is displayed.

[Program start]	
1. Program name [	]
2. Start mode	1. (*) Scan execution
	2. () Low-speed execution
	Execution (Y) Cancel (N)

Enter the program name for start with keys.

Select either scan execution or low-speed execution.

(b) Stop of program ()

[Program stop]	
1. Program name [	]
2. Stop mode	1. (*) Output stop after stop
	2. () Output retention after stop
	Execution (Y) Cancel (N)

Enter the program name for stop with keys.

Select either output stop after stop or output retention after stop.

- 1) When the stop mode is set to "Output stop after stop" and stop is executed, the program stops after execution of 1 scan-off. (The operation is the same as the POFF instruction execution.)

When the above stop operation is made in the stand-by program, the program stops after 1 scan-off execution.

Therefore, the "execution count" is added by one.

- 2) If an error occurs with the RET/IRET instruction during 1 scan OFF execution in the stand-by program, the "execution count" is added by one.

In this case, the execution type becomes "Scan execution".

8.4.2 Interrupt program monitor list

This function displays the number of executions of interrupt programs.

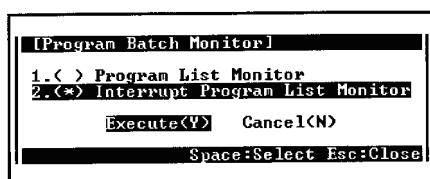
Application

This is used to check the execution status of interrupt programs.

Function Description

This function allows display of the execution counts of interrupt programs.
All operations are performed using the monitor/test menu in the ladder mode.

- (1) Select "Program Batch Monitor".



- (2) Select "Interrupt Program List Monitor".

The following shows an example of the display when the interrupt program monitor list function is run.

Int Prog List Moni				
	Ex	Times	Comment	
I 0	1	x	IAI61 X0	I
I 1	100	x	IAI61 X1	I
I 2	100	x	IAI61 X2	I
I 3	100	x	IAI61 X3	I
I 4	20	x	IAI61 X4	I
I 5	0	x	I	I
I 6	0	x	I	I
I 7	0	x	I	I
I 8	0	x	I	I
I 9	0	x	I	I
I10	0	x	I	I
I11	0	x	I	I
I12	0	x	I	I
I13	0	x	I	I
I14	0	x	I	I
PgUp:Prev PgDn:Next				Esc:Close

The following shows an explanation of the screen above:

- (a) "Ex Times"

The number of times the program has been executed, taking the point when monitoring started as 0 in the count, is displayed here.

(When reaching the maximum times of 65536, the count returns to 0.)

The count is cleared to zero when switching to RUN.

- (b) "Comment"

The comments set in the documentation mode are displayed here.

8.4.3 Scan time measurement

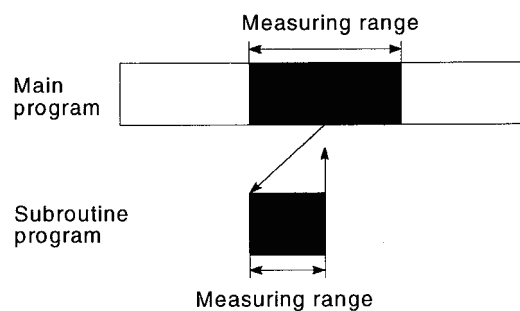
This function displays the processing time for section of a program.

Function Description

This function allows measurement of the execution time of section of the program in a program file.

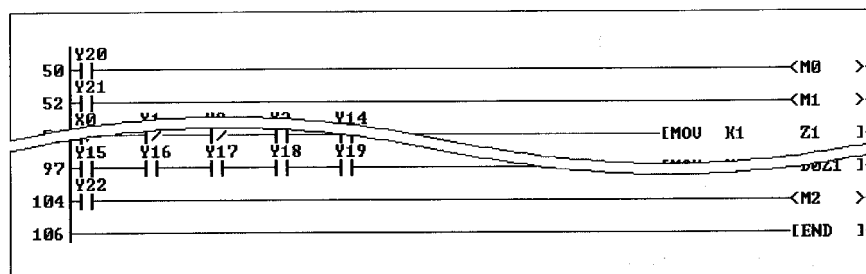
The function can also be used to measure times within subroutine programs and interrupt programs.

If there is an interrupt program in the monitored section, the processing is added to the total measurement time.

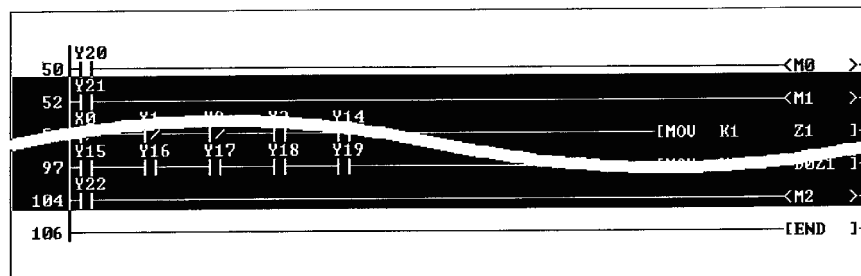


All operations are performed using "Monitor/test" menu in the ladder mode.

- (1) Select "Measure Scan".



- (2) Designate the scan time measurement range (The designated part is highlighted).



- (3) The scan time measurement results are displayed.

[Measur Scan]			
Start Stp	52	First	1.100ms
Last Step	105	Cur	1.100ms
		Max.	1.200ms
		Min.	1.000ms
Esc:Close			

NOTE

- 1) Make sure that the start step is lower than the end step in the setting.
- 2) Times that span different program files cannot be measured.
- 3) If the measured time is less than 0.100ms, 0.000ms is displayed.
- 4) END processing time is not included in the measuring time, being included in the measurement range.

8.5 Sampling Trace Function

The function that collects devices continuously on the CPU module with the specified timing.

POINT	
When executing the sampling trace function, a memory card is required.	

Application

This allows checking the changes in the contents of the devices used in a program in accordance with a designated timing during debugging.

This enables debugging time to be shortened.

Function Description

(1) Function

(a) The sampling trace function samples the contents of a designated device in a constant time interval (the sampling cycle) and stores the trace results in a sampling trace file in a memory card.

(b) The devices that can be traced are listed below.

- 1) Bit device: X, FX, DX, Y, FY, DY, M, L, F, SM, V, B, SB, T (Contact), T (Coil), ST (Contact), ST (Coil), C (Contact), C (Coil), J□\X, J□\Y, J□\B, J□\SB, BL□\S.....Max. 50 points
- 2) Word device: T (Current value), ST (Current value), C (Current value), D, SD, FD, W, SW, R, Z, ZR, U□\G, J□\W, J□\SW
.....Max. 50 points

- (c) The sampling trace file stores the trace condition data and trace execution data required to execute the sampling trace. Once a GPP function starts tracing, the number of set tracing times are executed.

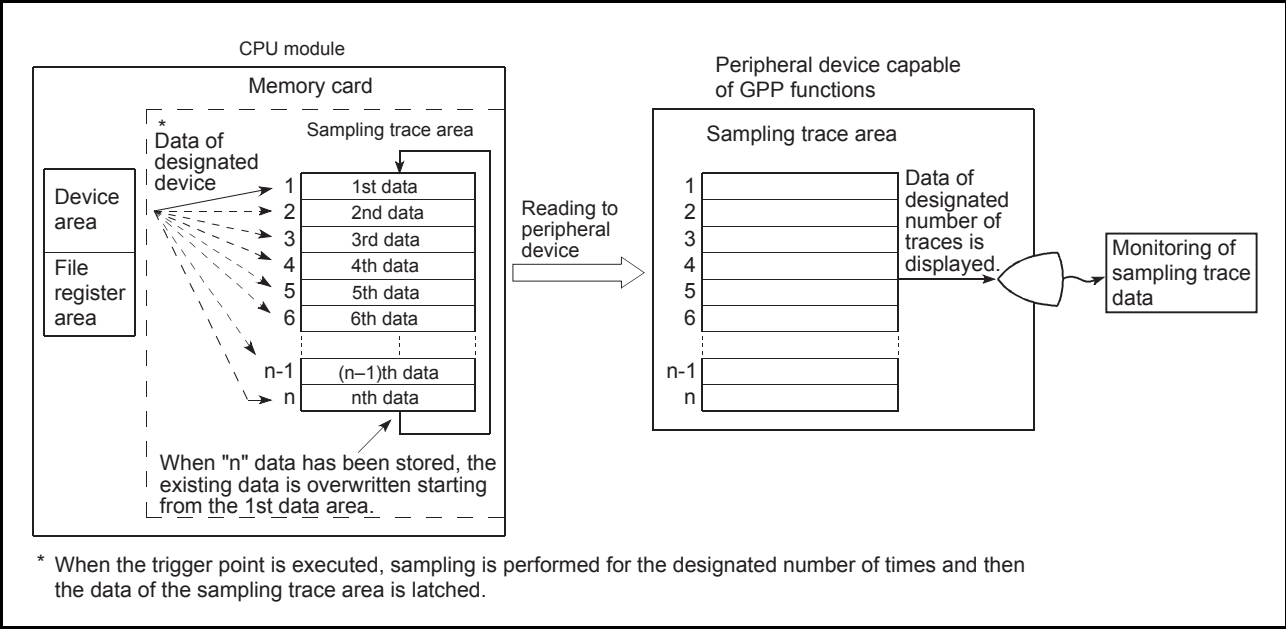
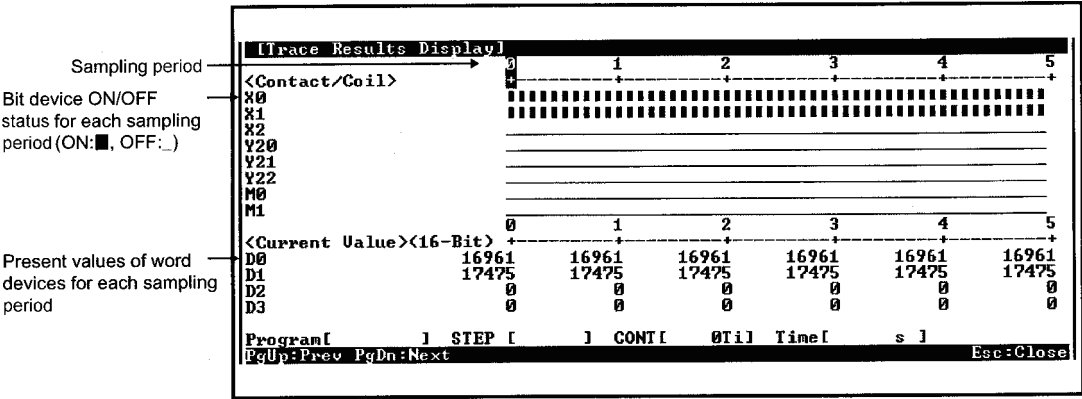


Fig. 8.1 Sampling trace operation

- (d) The trace results show the ON/OFF statuses of bit devices, and current values of word devices, for each sampling cycle.



NOTE

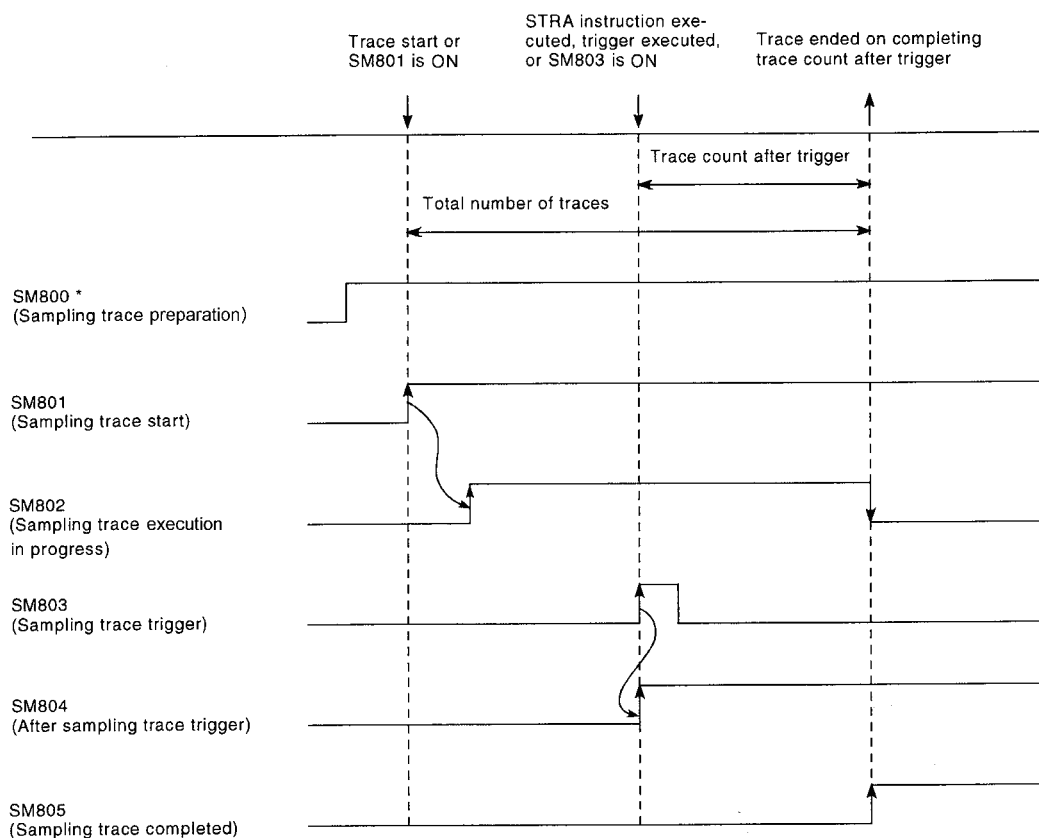
While the CPU module is STOP, trace is stopped. The trace result cannot be read.

(2) Basic operation

The basic operation for sampling trace is shown below.

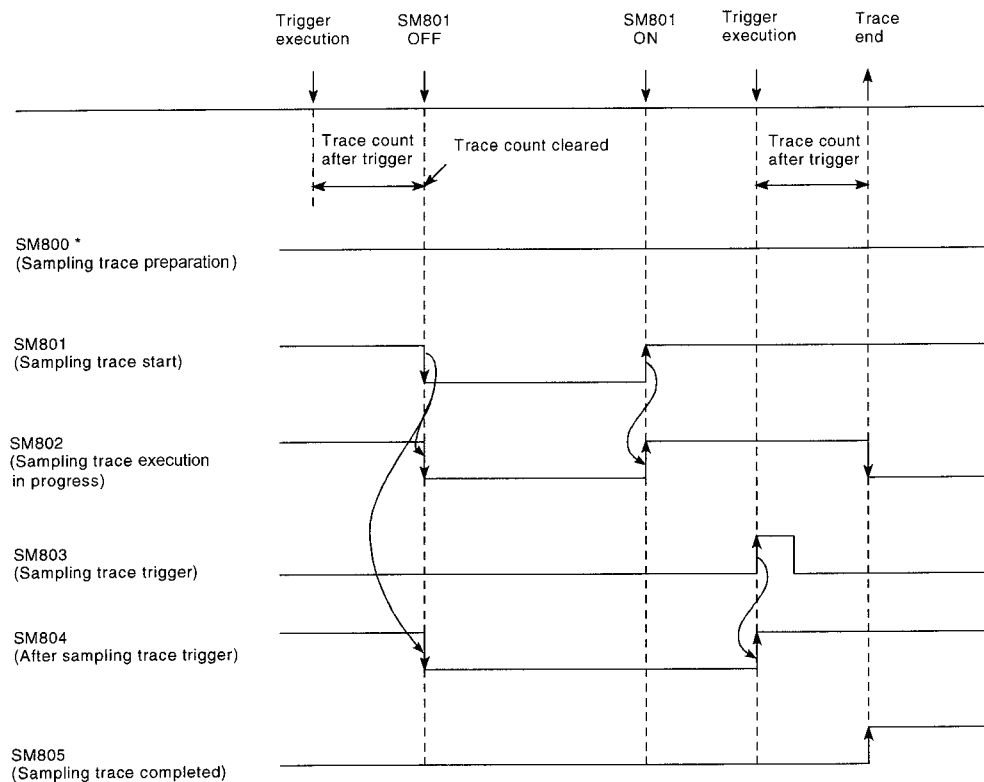
The statuses during execution of the sampling trace function can be confirmed by monitoring special relays SM800 to SM805 and SM826.

- Trace execution



* SM800 comes ON automatically when preparation for sampling trace is completed.

- Suspending the trace



* When the trace is suspended from a peripheral device capable of GPP functions, SM800 is turned OFF.

The following shows the operation at error occurrence.

When an error occurs during sampling trace, SM826 (sampling trace error) comes ON, and at the same time, SM801 (sampling trace start) goes OFF. Start the trace again for turning OFF SM826.

Operation Procedures

The following shows the procedures of sampling trace.

These operations are performed on the "Sampling Trace" screen of the trace menu in the online mode.

(1) Set the trace devices and trace conditions with GPP function.

(a) Setting the trace devices

Set the devices at "Trace Device Setting" on the "Sampling Trace" screen.

[Trace Device Setting]					
Bit Device		Selection	Word Device		Selection
[X0	]	< Do >	[D0	]	< Do >
[X1	]	< Do >	[D1	]	< Do >
[X2	]	< Do >	[D2	]	< Do >
[Y20	]	< Do >	[D3	]	< Do >
[Y21	]	< Do >	[	]	
[Y22	]	< Do >	[	]	
[M0	]	< Do >	[	]	
[M1	]	< Do >	[	]	
[M2	]	< Do Not >	[	]	
[	]		[	]	
[	]		[	]	
[	]		[	]	

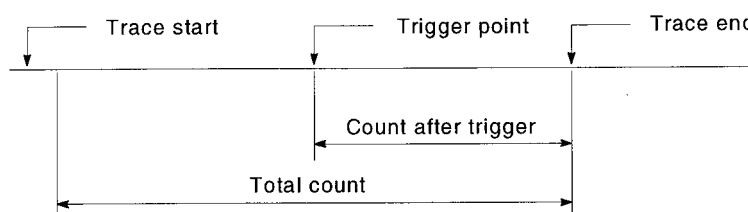
PgUp:Prev PgDn:Next Space:Select Esc:Close

(b) Setting the trace conditions

Set the trace conditions at "Trace Device Setting" on the "Sampling Trace" screen.

[Trace Condition Setting]	
1. Trace Counts	1. Total Counts [10] Times 2. Post-Trigger Counts [5] Times
2. Trace Point	1. < > Every END 2. < > Every Interval [] ms 3. < * > Specify Detail Condition
3. Trigger Point	1. < > At Instruction Execution 2. < > At Request of PDT 3. < * > Specify Detail Condition
4. Added Trace Information	1. [] Time 2. [] Step # 3. [] Program Name
Execute<Y> Cancel<N>	
Space:Select Esc:Close	

Sampling the designated number of times (count after trigger) leads completion after the trigger point execution.



The following shows an explanation of the screen above:

One of the following four settings can be made for the trace condition: "1. Trace Counts", "2. Trace Point", "3. Trigger Point", or "4. Added Trace Information".

1) "Trace Counts"

In the case of the total count, set the number of sampling traces executed from start to end of the trace.

In the case of the count after the trigger, set the number of sampling traces executed from the trigger execution to the trace end.

The following shows the formula that sets range for these counts:

$$\text{Count after trigger} \leq \text{total count} \leq 8192$$

2) "Trace Point"

Set the timing for collection of trace data. Select one of the following:

- Ⓐ Every END : Data collected at END instruction of every scan.
- Ⓑ Every Interval : Data collected with each designated time. Setting range is 5 to 5000ms in 5ms units.
- Ⓒ Specify Detail Condition : Set a device and step number.
The following shows setting examples: The details on how to make the settings and data collection timing are the same as described in Section 8.2.1 Monitor condition setup in Monitor Function.

The following shows the setting device under the detailed condition.

- Ⓐ Bit device : X, FX, Y, FY, M, L, F, SM, V, B, SB, T (Contact), ST (Contact), C (Contact), J□\X, J□\Y, J□\B, J□\SB, BL□\S
- Ⓑ Word device : T (Current value), ST (Current value), C (Current value), D, SD, FD, W, SW, R, Z, ZR, U□\G, J□\W, J□\SW

The following qualifications are possible with respect to the devices listed above.

- Digit designation for bit devices
- Bit number designation for word devices

[Trace Pt Setting]			
	Device	Current Value	
1.[*] Device	1.< > Word Device [	]= [	]
	2.< * > Bit Device [X0	]= < ↑ >	
2.[*] Step #	[	1]= <Always>	
Execute(Y) Cancel(N)			
Space:Select Esc:Close			

3) "Trigger Point"

The point at which the trigger is executed is set. Select one of the following:

- Ⓐ At Instruction Execution : When executing STRA instruction
- Ⓑ At Request of PDT : When operating trigger using GPP functions
- Ⓒ Specify Detail Condition : Set a device and step number.

The following shows setting examples: The details on how to make the settings and trigger execution timing are the same as described in Section 8.2 Monitor condition setup in Monitor Function.

[Trigger Pt Setting]			
		Device	Current Value
1.[*] Device	1.< > Word Device [		]= [
	2.<*> Bit Device [X2		]= < ↑ >
2.[*] Step #	[	]= <Always>	
		Execute<Y>	Cancel<N>
Space:Select Esc:Close			

4) "Added Trace Information"

Set information to be added at each trace. Select one or multiple item(s) of the following: (Making no selection is possible.)

- Ⓐ Time : The time at which the trace was executed is stored.
- Ⓑ Step No. : The step number at which the trace was executed is stored.
- Ⓒ Program Name : The program name for which the trace was executed is stored.

(2) Write the set trace device and trace condition to the memory card.

(a) Set the trace file and storage destination.

Set the drive number and file name at "1. () Execute Trace & Display Status" on the "Sampling Trace" screen.

[Execute Trace & Display Status]	
2. Sampling Trace Data	
File to Save	
1.< > Select From List	
2.<*> File Shown Right	Drive [1] File Name [SAMPLE5]

(b) Write the trace file to the memory card.

Write the trace file to the memory card by using "9. () Write to PC (Condition)" on the "Sampling Trace" screen.

Since file names are used when writing to the memory card, multiple trace files can be written.

- (3) Execute the sampling trace.
 Execute the sampling trace by using "1. () Execute Trace & Display Status" on "Sampling Trace" screen.
 The following shows a setting example for "1. () Execute Trace & Display Status".

[Execute Trace & Display Status]

1. Operation
 1.< > Register, Start
 2.< > Suspension
 3.<*> **Display Status**
 4.< > Trigger Execution

2. Sampling Trace Data
 File to Save
 1.< > Select From List
 2.<*> File Shown Right

3. Trace Condition
 1.< > Overwrite Conditions onto CPU's
 2.<*> Use Condition in CPU

<SmpTr state>
 Total Setg Curr
 0Ti 0Ti
 AftTrig 0Ti 0Ti
 Trace Not Execute

Execute<Y> Cancel<N>

Space:Select Esc:Close

Displayed only when "Display Status" is selected.

The following shows an explanation of the screen above:

The following settings can be made for "Execute Trace & Display Status" : "1. Operation", "2. Sampling Trace Data", and "3. Trace Condition".

(a) "Operation"

Select one of the following:

- 1) Register, Start : The trace is registered and started. The trace count is started.
- 2) Suspension : The trace is suspended. The trace count and the count are cleared after the trigger. (To restart the trace, select "Register, Start" again.)
- 3) Display Status : The trace statuses are displayed on the same screen.
- 4) Trigger Execution : The count is started after the trigger. The trace is ended on reaching the designated count after the trigger.

(b) "Sampling Trace Data"

Select one of the following:

- 1) Select From List : Data from among the sampling trace files in the memory card are selected.
- 2) File Shown Right : The drive number and sampling trace file name are set.

(c) "Trace Condition"

Select one of the following:

- 1) Overwrite Conditions onto CPU's : The trace condition in an existing trace file is overwritten.
 - 2) Use Condition in CPU : Sampling trace under the condition in the trace file designated in "2. Sampling Trace Data" is executed.
- (4) Retrieve the trace results from the CPU module and display them.
- 1) Read the trace results from the CPU module by using "4. () Read from PC (Results)" on the "Sampling Trace" screen.
 - 2) Display the trace results by using "4. () Trace Results Display" on the "Sampling Trace" screen.

POINT

Once the sampling trace has been executed, the second is not executed. To execute the trace again, execute the STRAR instruction to reset sampling trace.

NOTE

- 1) Set sampling trace files in the RAM area of the memory card.
- 2) It is possible to execute sampling trace from another station in the network, or from a serial communication module. However, sampling trace cannot be executed from more than one site at the same time. With the QnACPU, sampling trace can be executed from only one site at a time.
- 3) Since the trace condition registered in the CPU module is latched, the condition data is retained even when the PLC power is turned OFF. The data can be cleared by performing a latch clear operation using the RUN/STOP key switch on the QnACPU.
- 4) The QnACPU must be connected to the peripheral device capable of GPP functions in order to execute sampling trace.

8.6 Status Latch Function

This function collects the data of devices at designated moment.

POINT	
When executing status latch function, a memory card is required.	

Application

This function is used to retain the statuses of devices used in a program at designated moment during debugging.

Function Description

- (1) Function
 - (a) Status latch stores the device statuses at designated moment in a status latch file of a memory card.
 - (b) The status latch file stores the status latch condition and status latch execution data for status latch execution.

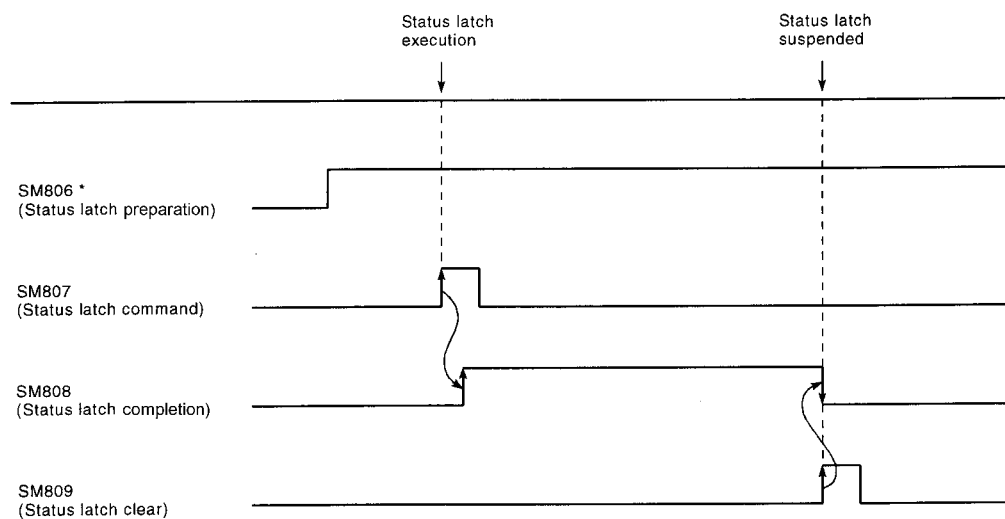
Saving the device statuses can be executed in the following case.

 - When executing SLT instruction in a program
 - When specifying a status latch start at GPP functions
 - When the conditions of the set devices and step Nos. are met
 - (c) The status latch results show the bit device ON/OFF statuses and word devices values at designated moment.

(2) Basic operation

The following shows the basic operation for status latch.

The statuses during execution of the status latch function can be checked by monitoring special relays SM806 to SM809 and SM827.



* SM806 comes ON automatically when preparation for status latch is completed.

(3) The following shows the operation at error occurrence.

When an error occurs during status latch, SM827 comes ON, and at the same time SM808 (completed) is turned ON.

To turn SM827 OFF, either turn SM809 ON or execute the SLTR instruction.

Operation Procedures

The following shows procedures for status latch.

All operations are performed on the "Status Latch" screen of the trace menu in the online mode.

(1) Setting the status latch condition

Set the status latch condition at "2. () Status Latch Condition Setting" on the "Status Latch" screen.

```

[Status Latch Condition Setting]

1. Status Latch Device Setting
   1.< > All Internal Dev <Yes>
   File R [ ] 1-[ ]
   2.<*> Specify Detail Range

2. Trigger Point
   1.< > At Instruction Execution
   2.< > At Request of PDT
   3.<*> Specify Detail Condition

Execute<Y>   Cancel<N>

Space:Select Esc:Close
  
```

The following shows an explanation of the screen above:

Either "1. Status Latch Device Setting" or "2. Trigger Point" can be set for the status latch condition setting.

(a) "Status Latch Device Setting"

Set the devices to execute the status latch. Select one of the following:

- 1) All Internal Dev : Whether or not QnACPU latches all built-in devices is set.
- 2) Specify Detail Range : The device types and numbers of points are set.

The following shows setting examples:

```

[Status Latch Device]

# of Pt   First Device   Last Device
[ 4]      [D0           1-[D3
[ 3]      [M0           1-[M2
[ ]       [             1-[
[ ]       [             1-[
[ ]       [             1-[
  
```

(Applicable devices)

- 1) Bit device : X, Y, M, L, F, SM, V, B, SB, T (Contact), T (Coil), C (Contact), C (Coil), ST (Contact), ST (Coil), J□\X, J□\Y, J□\B, J□\SB, BL□\S
- 2) Word device : T (Current value), ST (Current value), C (Current value), D, SD, W, SW, R, ZR, U□\G, J□\W, J□\SW

REMARK

Up to 1000 device ranges can be set including both bit devices and word devices.
The devices listed above cannot be qualified.

(b) "Trigger Point"

Set the condition to execute the status latch. Select one of the following:

- 1) At Instruction Execution : When executing SLT instruction
- 2) At Request of PDT : When operating trigger using the peripheral devices capable of GPP function.
- 3) Specify Detail Condition : Set a device and step number.

The following shows setting examples: The details on how to make the settings and trigger execution timing are the same as described in Section 8.2.1 Monitor condition setting in Monitor function.

Data collection timing

- In the case that only "Device" is specified, data are collected when the trigger condition is satisfied.
- In the case that "Step No." only is set, data is collected with the END processing when the trigger condition is satisfied.

[Trigger Pt Setting]			
1.[*] Device	1.< >	Word Device [	Device
	2.<*>	Bit Device [X0	Current Value]
2.[] Step #	[	]= < ↑ >	
		]= <Always>	
Execute<Y> Cancel<N>			
Space:Select Esc:Close			

(2) Write the created status latch condition to the memory card.

(a) Set the status latch file and storage destination.

Set the status latch condition at "1. () Exec Status Latch & Disp Status" on the "Status Latch" screen.

[Exec Status Latch & Disp Status]	
2. Sampling Trace Data	
File to Save	
1.< >	Select From List
2.<*>	File Shown Right
Drive [1]	File Name [SAMPLE5]

(b) Write the status latch file to the memory card.

Write the status latch file to the memory card using "7. () Write to PC (Condition)" on "Status Latch" screen.

Since file names are used when writing to the memory card, multiple status latch files can be written.

- (3) Execute the status latch.

Execute the status latch by using "1. () Exec Status Latch & Disp Status" on "Status Latch" screen.

The following shows a setting example for "1. () Execute Status Latch & Display Status".

[Exec Status Latch & Disp Status]

1. Operation
 1.< > Register, Start
 2.< > Suspension
 3.<*> **Display Status**
 4.< > Trigger execution

2. Status Latch
 File to Save
 1.< > Select from List
 2.<*> File Shown Right Drive [1]
 File Name [SAMPLE7B]

3. Trace Condition
 1.< > Overwrite Conditions onto CPU's
 2.<*> Use Condition in CPU

Execute<Y> Cancel<N>

Space:Select Esc:Close

<StsLtch State>
 StsLtch Not Register

Displayed only when "Display Status" is selected.

The following is an explanation of the screen above:

The following settings can be made for "Exec Status Latch & Disp Status": "1 Operation", "2 Status Latch", and "3 Trace Condition".

(a) "Operation"

Select one of the following:

1) Register, Start	: The status latch is registered and started. Device data collection is started.
2) Suspension	: The status latch statuses are cleared.
3) Display Status	: The status latch statuses are displayed on the same screen.
4) Trigger execution	: The trigger is executed. (Refer to Precaution 6.)

(b) "Status Latch"

Select one of the following:

1) Select From List	: Data from among the status latch files in the memory card are selected.
2) File Shown Right	: The drive number and status latch file name are set.

(c) "Trace Condition"

Select one of the following:

1) Overwrite Conditions onto CPU's	: The status latch condition in an existing status latch file is overwritten.
2) Use Condition in CPU	: Status latch under the condition in the status latch file designated in "2. Status Latch" is executed.

- (4) Retrieve the status latch results from the CPU module and display them.
 - (a) Read the status latch results from the CPU module by using "8. () Read from PC (Results)" on "Status Latch" screen.
 - (b) Display the read trace results by setting "1. () Monitor Target" on the "Monitor Target Setting" screen of "Option" menu in the ladder mode to "3. () Status Latch".

NOTE

- 1) Set status latch files in the RAM area of the memory card.
- 2) It is possible to execute status latch from another station in the network, or from a serial communication module. However, sampling trace cannot be executed from more than one site at the same time.
With QnACPU, sampling trace can be executed from only one site at a time.
- 3) Since the status latch conditions registered in the CPU module are latched, the status latch data is retained even when the power is turned OFF.
The data can be cleared by performing a latch clear operation using the RUN/STOP key switch on the QnACPU.
- 4) Status latch is performed by connecting the QnACPU with the peripheral devices capable of GPP function.
- 5) When the monitor destination is set to the "status latch", set values of the timer/counter are not displayed.
"0" is displayed for the column of the timer/counter set values.
- 6) When "device" is specified in the detailed condition for trigger point setting, "device" is specified. When the condition is satisfied before execution of the trigger, trigger cannot be executed.

REMARK

- 1) When the monitor destination is set to "device memory", the set values of the timer/counter are not displayed.
"0" is displayed in the set value column of the timer/counter.

8.7 Step Operation

This function runs one step or one part of a program, runs a program with a part skipped.

Application

This function is used to determine the causes of faults during debugging.

Function Description

This function can only be used when the CPU module is set to STEP-RUN.

The step operation function provides the following three functions. For explanations of each function, refer to Section 8.7.1 through Section 8.7.3.

- Step execution
- Partial execution
- Skip execution

8.7.1 Step execution

Step execution is a sequence program execution that performs by one step at a time, starting from the designated step.

It allows a sequence program execution while checking an execution status of the sequence program and the contents of each device during debugging.

There are two types of step execution as described below:

- (1) Step execution for one instruction
- Instructions are executed one for each step starting from the step where program operation is stopped. Program operation is stopped again after execution of each instruction.
- This method is used to confirm the status of each devices after execution of one instruction.

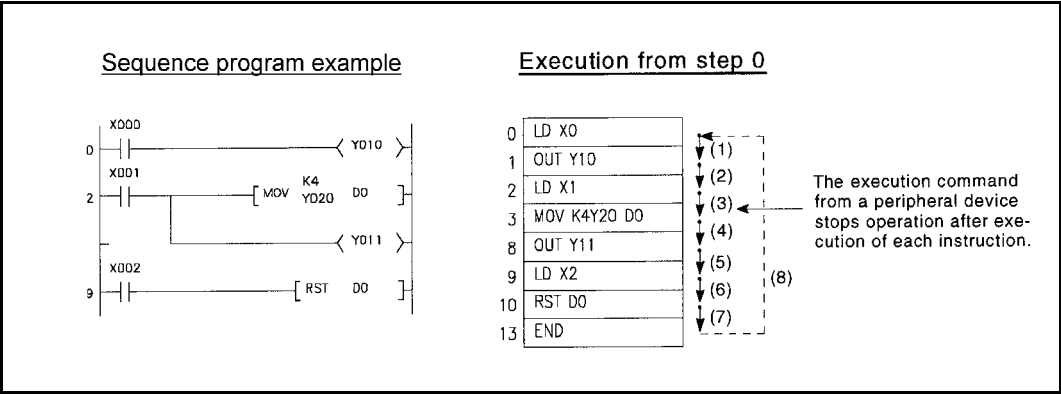


Fig. 8.2 Step execution for each instruction

- (2) Step execution with designated loop count
- Program execution is repeated for the designated loop count (range: 1 to 32767) beginning with step 0 or the step where program operation was last stopped, and is stopped at the designated step (break point).

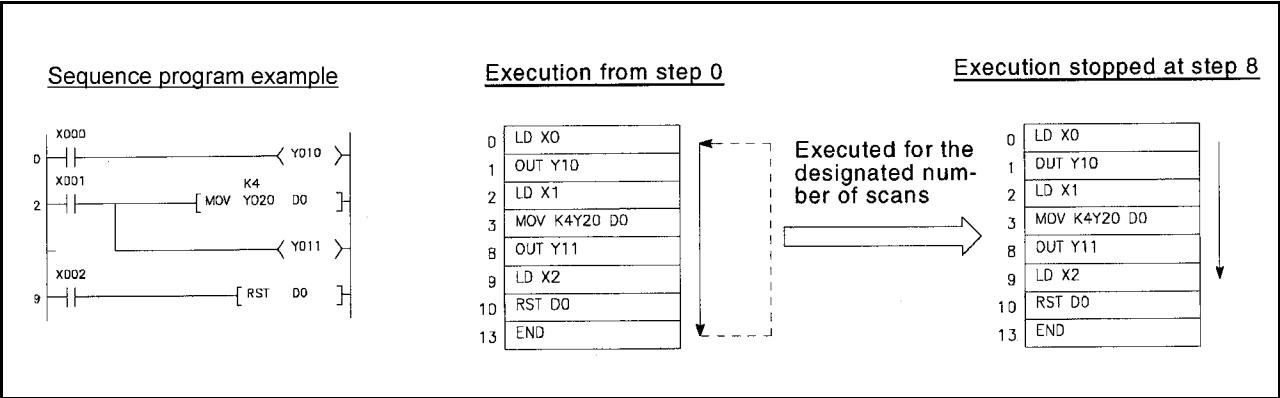


Fig. 8.3 Step execution with designated loop count

Operation Procedures

The following shows the procedures to perform step execution.

All operations are performed on Monitor/test screen in the ladder mode (debugging).

- (1) Select "B/Step Run".

[Step Run]			
1. Step Run	1.<*>	From Current Step	
	2.< >	Start Step/Pointer	[0]
2. Option	1.[]	# of Retries	[1]Times
	2.[]	Repeating Interval	[1000]
	3.[]	Break Point	1.[] Step/Pointer [0]
			2.[] Step/Pointer [0]
			3.[] Step/Pointer [0]
			4.[] Step/Pointer [0]
			5.[] Step/Pointer [0]
			6.[] Step/Pointer [0]
			7.[] Step/Pointer [0]
			8.[] Step/Pointer [0]
Execute<Y> Cancel<N>			
Space:Select Esc:Close			

8.7.2 Partial execution

The sequence program is executed from the start step or the step where operation is currently stopped to a designated step (break point).

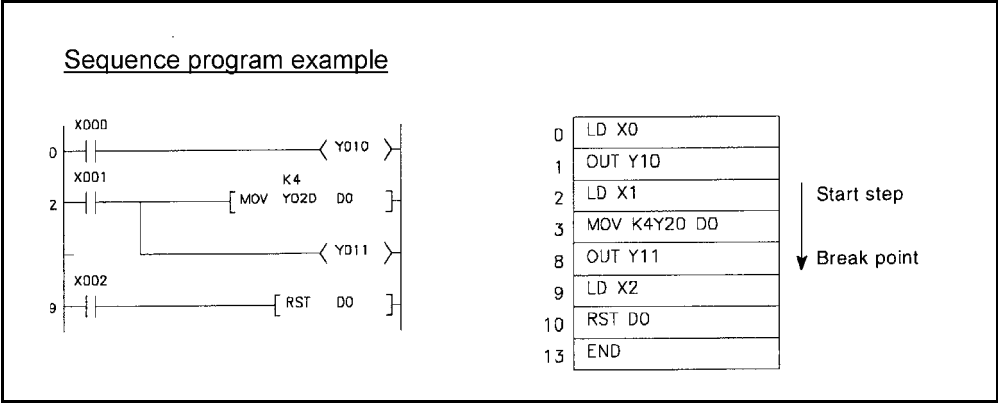
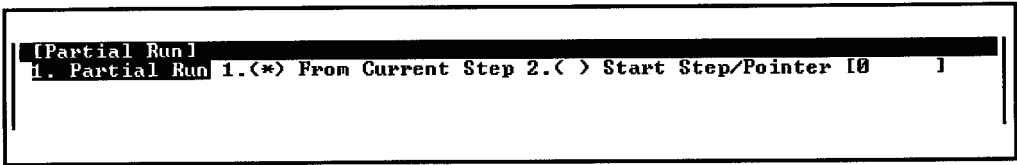


Fig. 8.4 Partial execution

Operation Procedures

The following shows the procedures to perform partial execution.
All operations are performed on Monitor/test screen in the ladder mode (debugging).

- (1) Designate the execution start step, break condition, and execution operation with GPP function.
 - (a) Setting the execution start step
Designate the step at which partial execution is started at "1. Partial Run" on the "Partial Run" screen.



(b) Setting the break condition

Set the device status and break point at "2. Break Cond" on the "Partial Run" screen.

[Partial Run]			
1. Partial Run	1.<*> From Current Step	2.< > Start Step/Pointer	[0] 1
2. Break Cond	1.[] Device	Device	Current Value
	1.<*> Word Device	[]	[K0]
	2.< > Bit Device	[]	[< ↑ >]
	2.[] Break Point		
	1.[] Step/Pointer	[0]	] = < Always> [1Times
	2.[] Step/Pointer	[0]	] = < Always> [1Times
	3.[] Step/Pointer	[0]	] = < Always> [1Times
	4.[] Step/Pointer	[0]	] = < Always> [1Times
	5.[] Step/Pointer	[0]	] = < Always> [1Times
	6.[] Step/Pointer	[0]	] = < Always> [1Times
	7.[] Step/Pointer	[0]	] = < Always> [1Times
	8.[] Step/Pointer	[0]	] = < Always> [1Times
3. Option	1.[] Scan Time	1.<*> Real-time	
		2.< > Specified Time	[10]ms
	2.[] Interrupt Status	< Inhibit >	
	3.[] Refresh	< Successively>	
		Execute<Y>	Cancel<N>
Space:Select Esc:Close			

The following shows the devices that can be set.

- 1) Bit device : X, FX, DX, Y, FY, DY, M, L, F, SM, V, B, SB, T (Contact), T (Coil), ST (Contact), ST (Coil), C (Contact), C (Coil), J□\X, J□\Y, J□\B, J□\SB, BL□\S
- 2) Word device : T (Current value), ST (Current value), C (Current value), D, SD, FD, W, SW, R, Z, ZR, U□\G, J□\W, J□\SW

8.7.3 Skip function

Skip execution or partial execution of a program whereby the program is executed with the designated step(s) skipped.

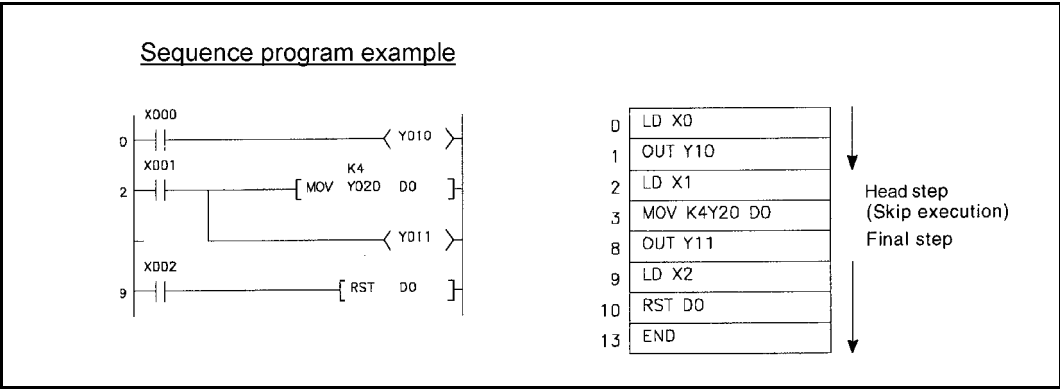
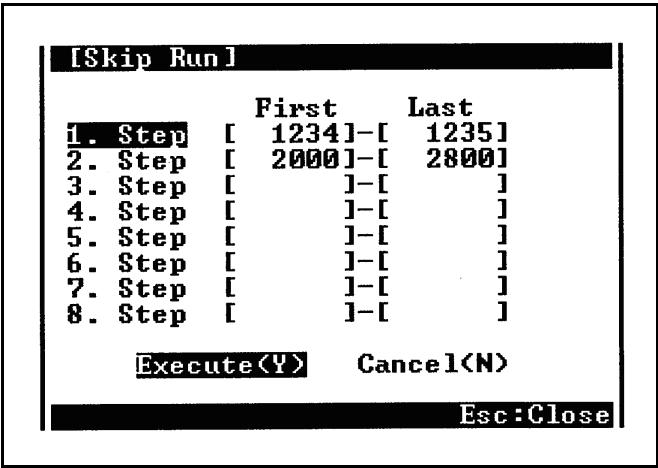


Fig. 8.5 Skip execution

Operation Procedures

The following shows the procedures to perform skip execution.
All operations are performed on Monitor/test screen in the ladder mode (debugging).

- (1) Set the program range to be skipped using GPP function.
Designate the step number(s) to be skipped on "D/Skip Run" screen.



8.8 Program Trace Function

This function collects program execution statuses.

POINT
When executing the program trace function, a memory card is required.

Application

This function is used to check the execution status of any step of any program during debugging.

This enables debugging time to shorten.

Function Description

(1) Function

(a) The program trace function collects the execution status of the designated step of the designated program and stores it in a program trace file in the memory card.

(b) The devices that can be traced are listed below.

- 1) Bit device : X, FX, DX, Y, FY, DY, M, L, F, SM, V, B, SB, T (Contact), T (Coil), ST (Contact), ST (Coil), C (Contact), C (Coil), J□\X, J□\Y, J□\B, J□\SB, BL□\S.....Max. 50 points
- 2) Word device : T (Current value), ST (Current value), C (Current value), D, SD, FD, W, SW, R, Z, ZR, U□\G, J□\W, J□\SW
.....Max. 50 points

(c) The program trace file stores the trace condition data and trace execution data to execute a program trace. After a trace is started in a peripheral device capable of GPP functions, it is continued until the set number of traces is completed.

(d) The trace results show the program name, step No. device status, etc., for each trace No.

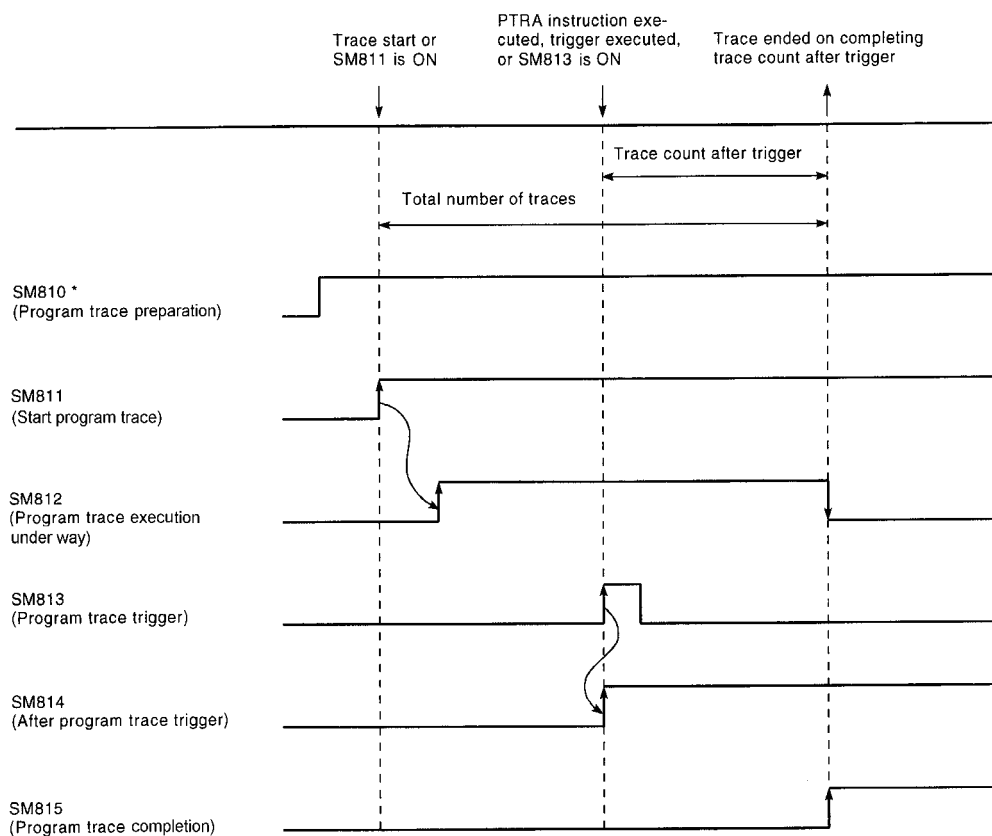
[Trace Results Display]							
Times	Program	Step	BranchIns	Time(ms)	D0	M0	M1
-5	MAIN	0	S 0 Step	1894.2	31339		
-4	MAIN	9	END(FEND)	1894.5	31340		
-3	MAIN	0	<Stat>	1894.9	31340		
-2	MAIN	0	S 0 Step	1900.4	31340		
-1	MAIN	9	END(FEND)	1900.6	31341		
0	MAIN	0	<Stat>	1901.1	31341		
1	MAIN	0	S 0 Step	1906.7	31341		
2	MAIN	9	END(FEND)	1906.9	31342		
3	MAIN	0	<Stat>	1907.5	31342		
4	MAIN	0	S 0 Step	1912.7	31342		
5	MAIN	9	END(FEND)	1912.9	31343		
6	MAIN	0	<Stat>	1913.4	31343		
7	MAIN	0	S 0 Step	1918.6	31343		
8	MAIN	9	END(FEND)	1918.8	31344		
9	MAIN	0	<Stat>	1919.3	31344		
PgUp:Prev PgDn:Next							Esc:Close

(2) Basic operation

The following shows the basic operation for program trace.

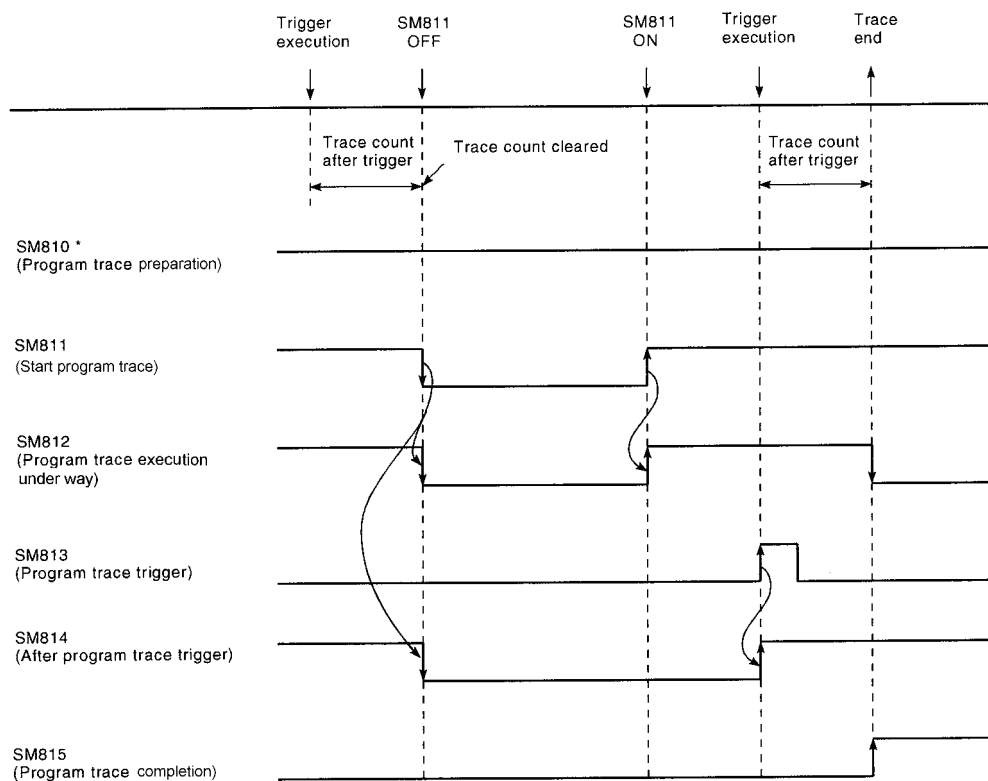
The statuses during execution of the program trace function can be confirmed by monitoring special relays SM810 to SM815 and SM828.

- Without suspension of the trace



* When ready for program trace, SM810 is automatically turns ON.

- With trace suspension



* When the trace is suspended from a peripheral device capable of GPP functions, SM810 is turned OFF.

The following shows an operation at error occurrence.

When an error occurs during program trace, SM828 (program trace error) comes ON, and at the same time, SM811 (program trace start) goes OFF.

To turn SM828 OFF, either turn SM811 ON, or execute the PTRR instruction.

Operation Procedures

The following shows the procedures to perform program trace.

These operations are performed on the "Program Trace" screen of the trace menu in the online mode.

Perform these operations with the CPU module setting to the STEP-RUN. (Refer to Section 8.7.)

(1) Set the trace devices and trace conditions with GPP function.

(a) Setting the trace devices

Set the devices at "Trace Device Setting" on the "Program Trace" screen.

[Trace Device Setting]					
Bit Device		Selection	Word Device		Selection
[X0	]	< Do >	[D0	]	<Do Not>
[X1072	]	<Do Not>	[K4X0	]	< Do >
[J2\B100	]	< Do >	[U1\G10	]	<Do Not>
[D0.0	]	<Do Not>	[W0Z3	]	< Do >
[M0	]	< Do >	[	]	
[Y100	]	<Do Not>	[	]	
[	]		[	]	
[	]		[	]	
[	]		[	]	
[	]		[	]	
[	]		[	]	
[	]		[	]	

PgUp:Prev PgDn:Next Space:Select Esc:Close

(b) Setting the trace conditions

Set the trace conditions at "Trace Condition Setting" on the "Program Trace" screen.

```

[Trace Condition Setting]

1. Trace Counts      1. Total Counts [ 1024]Times
                    2. Post-Trigger Counts [ 500]Times

2. Trace Point
                    1.[*] Branch Instruction
                    2.[*] Every Interruption
                    3.[*] At Instruction Execution

3. Trigger Point
                    1.< > At Instruction Execution
                    2.< > At Request of PDT
                    3.<*> Specify Detail Condition

Execute<Y>      Cancel<N>

Space:Select  Esc:Close

```

The following is an explanation of the screen above:

One of the following three settings can be made for the trace condition: "1. Trace Counts", "2. Trace Point", or "3. Trigger Point".

1) "Trace Counts"

For the total count, set the number of program traces executed from the trace start to the trace end.

For the count after the trigger, set the number of program traces executed from execution of the trigger to the trace end.

The following shows the formula that sets range for these counts:

$$\text{Count after trigger} \leq \text{total count} \leq 8192$$

2) "Trace Point"

Set the point at which the trace is to be executed. Select one or multiple item(s) of the following:

- Ⓐ Branch Instruction :Executed at each CALL, JMP, or other instructions.
- Ⓑ Every Interruption :Executed at each interrupt program.
- Ⓒ Upon execution of :Executed at each PTRAXE instruction.
each instruction

3) "Trigger Point"

Set the point at which the trigger is executed. Select one of the following:

- ① Upon execution of : When executing PTR instruction each instruction
- ② At Request of PDI : When operating trigger using the peripheral devices capable of GPP function.
- ③ Specify Detail Condition : Set a device and step number.
The following shows setting examples: The details on how to make the settings and trigger execution timing are the same as described in Section 8.2 Monitor condition setup in Monitor function.

[Trigger Pt Setting]			
		Device	Current Value
1.[*] Device	1.< > Word Device	[	] = []
	2.< * > Bit Device	[X2	] = < ↑ >
2.[] Block	1.1.< * > Step	[] Sequence Step #	[] < Always >
	2.< > TR	[] Sequence Step #	[] < Always >
Execute<Y> Cancel<N>			
Space:Select Esc:Close			

The following shows the setting device under the detailed condition.

- Bit device : X, FX, Y, FY, M, L, F, SM, V, B, SB, T (Contact), ST (Contact), C (Contact), J□\X, J□\Y, J□\B, J□\SB, BL□\S
- Word device : T (Current value), ST (Current value), C (Current value), D, SD, FD, W, SW, R, Z, ZR, U□\G, J□\W, J□\SW

The following qualifications are possible with respect to the devices listed above.

- Digit designation for bit devices
- Bit number designation for word devices

POINT
The trace execution time, program name, step and branch factor are automatically added to the trace results.

(2) Write the set trace device and trace condition to the memory card.

(a) Set the trace file and storage destination.

Set the drive number and file name at "1. () Execute Trace & Display Status" on "Program Trace" screen.

[Execute Trace & Display Status]

2. Program Trace Data

File to Save

1.< > Select From List

2.<*> File Shown Right

Drive [1]

File Name [SAMPLE5]

(b) Write the trace file to the memory card.

Write the trace file to the memory card by using "9. () Write to PC (Condition)" on "Program Trace" screen.

Since file names are used when writing to the memory card, multiple trace files can be written.

- (3) Execute the program trace.

Write the trace file to the memory card by using "9. () Write to PC (Condition)" on "Program Trace" screen.

The following shows a setting example for "1. () Execute Trace & Display Status".

[Execute Trace & Display Status]

1. Operation
 1.< > Register, Start
 2.< > Suspension
 3.<*> **Status Display**
 4.< > Trigger Execution

2. Program Trace Data
 File to Save
 1.< > Select from List
 2.<*> File Shown Right Drive [1] File Name [SAMPLE7B1]

3. Trace Condition
 1.< > Overwrite Conditions onto CPU's
 2.<*> Use Condition in CPU

Execute(Y) Cancel(N)

Space:Select Esc:Close

<ProIr state>

	Setg	Curr
Total	0Ti	0Ti
AftTrig	0Ti	0Ti
Trace	Not Register	

Displayed only when "Status Display" is selected.

The following is an explanation of the screen above:

The following settings can be made for "Execute Trace & Display Status": "1. Operation", "2. Program Trace Data", and "3. Trace Condition".

(a) "Operation"

Select one of the following:

- 1) Register, Start : The trace is started. The trace count is started.
- 2) Suspension : The trace is suspended. The trace count and the count are cleared after the trigger. (To restart the trace, select "Register, Start" again.)
- 3) Display Status : The trace statuses are displayed on the same screen.
- 4) Trigger Execution : The count is started after the trigger.
The trace is ended on reaching the designated count after the trigger.

(b) "Program Trace Data"

Select one of the following:

- 1) Select From List : Data from among the program trace files in the memory card are selected.
- 2) File Shown Right : The drive number and program trace file name are set.

(c) "Trace Condition"

Select one of the following:

- 1) Overwrite Conditions onto CPU's : The trace condition in an existing trace file is overwritten.
- 2) Use Condition in CPU : Program trace under the condition in the trace file designated in "2. Program Trace Data" is executed.

- (4) Retrieve the trace results from the CPU module and display them.
 - (a) Read the trace results from the CPU module by using "A. () Read from PC (Results)" on "Program Trace" screen.
 - (b) Display the read trace results by using "4. () Trace Results Display" on "Program Trace" screen.

POINT

Once the program trace has been executed, the second is not executed. To execute the trace again, execute the PTRAR instruction to reset program trace.

NOTE

- 1) The program trace can be performed only for STEP-RUN.
- 2) Set program trace files in the RAM area of the memory card.
- 3) It is possible to execute program trace from another station in the network, or from a serial communication module. However, sampling trace cannot be executed from more than one site at the same time. With the QnACPU, sampling trace can be executed from only one site at a time.
- 4) The program trace is performed by connecting the QnACPU with the peripheral device capable of GPP function.

8.9 Simulation Function

POINT	
	When the link memory and the buffer memory are simulated in the simulation data file, a memory card is required.

Application

This function simulates execution of a program in step execution or partial execution, with the input module, output module, or special function module isolated from the CPU module. This enables QnACPU to debug a program without any effects on other modules.

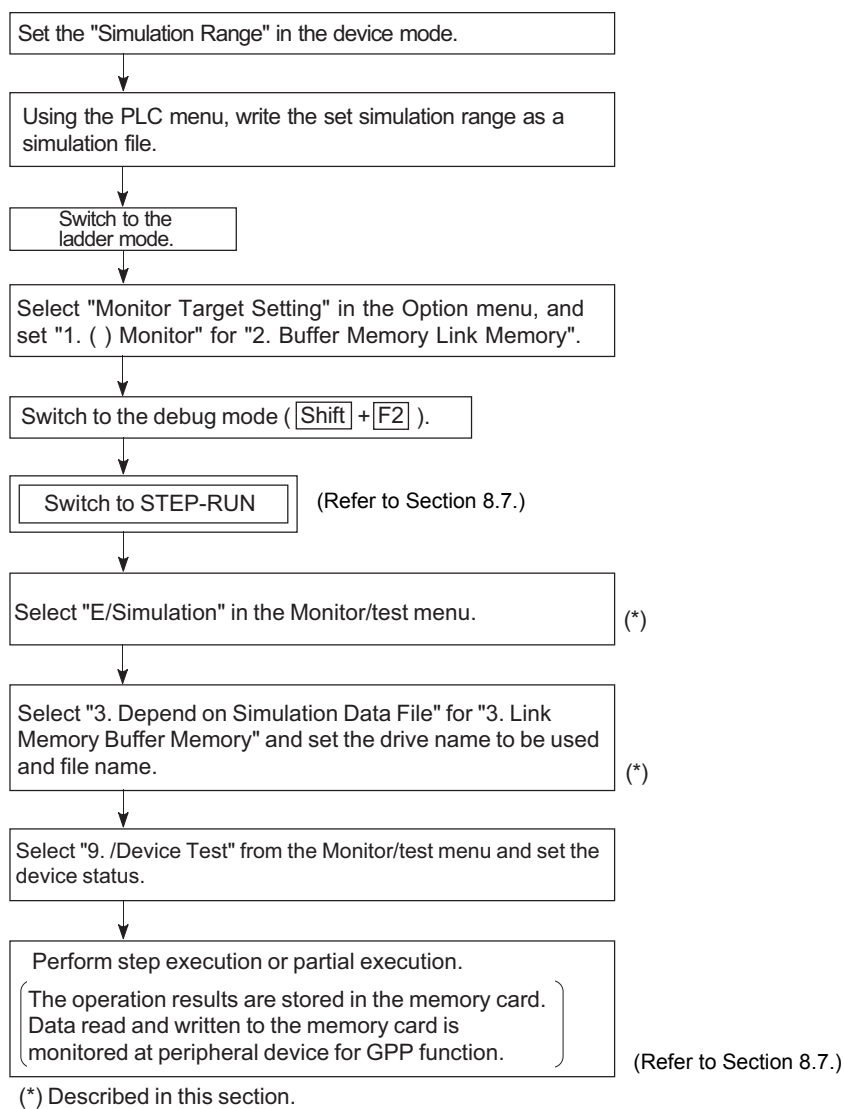
Function Description

- (1) When the program is executed, data changes from/to external sources are isolated by setting so that data refreshes for input/output modules are not executed.
- (2) Isolation from special function module operations is achieved by setting "Ignore" or "Depend on Simulation Data File" with respect to the buffer memory of the special function module.

Operation Procedures

The following shows the procedures to perform simulation.

□ indicates a GPP function operation and □ indicates an operation at the CPU module.



- (1) Make the settings on the simulation setting screen shown below.

```

[Simulation]
1.<*) Simulation Setting
  1. Input Refresh <Yes>
  2. Output Refresh <Yes>
  3. Link Memory  1.<*) Access Unit
     Buffer Memory 2.< > Ignore
                   3.< > Depend on Simulation Data File
                           Drive [0]
                           File [  ]
2.< > Simulation Range Confirmation
                        Execute<Y>   Cancel<N>
Space:Select Esc:Close

```

- The following shows details on the settings that can be made for each item:

Setting Item	Setting Option	Description
Input Refresh	Yes/No	Select whether inputs from external sources are input to the CPU module or not.
Output Refresh	Yes/No	Select whether the operation results in the CPU module are output to external destinations or not.
Link Memory/ Buffer Memory	Access Unit Ignore Depend on Simulation Data File	Select the method of accessing each module.

If "Depend on Simulation Data File" is selected for "Link Memory/Buffer Memory", the access range for each module can be checked by checking the simulation range settings.

[Simulation Range]				
#	# of Dev	First Device	Last Device	Comment
1	[0]	[	]->[	]
2	[0]	[	]->[	]
3	[0]	[	]->[	]
4	[0]	[	]->[	]
5	[0]	[	]->[	]
6	[0]	[	]->[	]
7	[0]	[	]->[	]
8	[0]	[	]->[	]
9	[0]	[	]->[	]
10	[0]	[	]->[	]
11	[0]	[	]->[	]
12	[0]	[	]->[	]
PgUp:Prev PgDn:Next Esc:Close				

NOTE

- Simulation can be performed only for STEP-RUN.
- A memory card is required to carry out link memory/buffer memory simulation using a simulation data file.
Set the simulation data file to the RAM area of the memory card.
- It is possible to carry out simulation from another station in the network, or from a serial communication module. However, simulation cannot be executed from several sites at the same time. With the QnACPU, sampling trace can only be executed from one site at a time.
- Simulation is performed by connecting the QnACPU and the peripheral devices capable of GPP function.
- Note the following points when executing simulation:
 - If direct inputs (DX) and direct outputs (DY) are used to handle inputs/outputs directly, the device memory is accessed rather than the actual inputs/outputs.
 - No processing is performed for any special function module instruction.
 - When a "SP.UNIT ERROR" occurs, FFFFH is displayed in the module number area of the common information.
 - If "Ignore" is set for the buffer memory access method, FFFFH is set for access by instruction and the monitor results.

8.10 Debugging by Several People

This function allows simultaneous debugging from several peripheral devices capable of GPP functions.

Application

This function is used to simultaneously debug different files from more than one peripheral device capable of GPP functions.

Function Description

The following shows the combinations of debugging functions that can be used simultaneously by different operators.

Debug function from host	Debug function from other stations						
	Monitor	Write during RUN	Execution Time Measurement	Sampling Trace /Program Trace	Status Latch	Step Operation	Simulation
Monitor	○	×	○	○	○	○	○
Write during RUN	×	○	×	×	×	×	×
Execution time measurement	○	×	×	○	○	○	○
Sampling trace	○	×	○	×	○	○	○
Program trace	○	×	○	×	○	○	○
Status latch	○	×	○	○	×	○	○
Step operation	○	×	○	○	○	×	○
Simulation	○	×	○	○	○	○	×

○: Simultaneous execution possible. (However, the detailed condition setting at only one peripheral device capable of GPP functions is valid; detailed conditions cannot be set at the other peripheral devices capable of GPP functions.)

×: Can only be executed from one peripheral device capable of GPP functions.

8.10.1 Simultaneous monitoring by several people

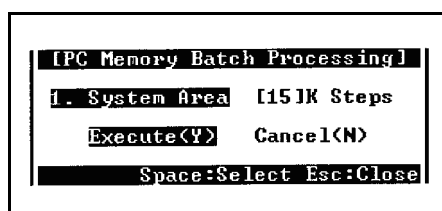
The QnACPU allows monitoring for several people. Setting of other station monitor file in the built-in RAM system area allows monitoring at a high-speed from other stations. (Monitor file setting for the host is not required.)

Operation Procedures

The operation for simultaneous monitoring by several people is described below.

- (1) Select "5. () Format (with Option)" for "B/PC Memory Batch Processing" in the "2/ PC" menu in the online mode, and set a monitor file for another station.

The following shows setting examples:



Up to 15k steps in 1k step units can be set as the system area. The area corresponding to one monitor file for another station is no more than 1k step. Accordingly, a maximum of 15 monitor files can be set.

Since the built-in RAM program file area is in the same area as the monitor file for other stations, the program file area is reduced for the area of the other station monitor file.

- (2) After setting, the built-in RAM is formatted.

NOTE

- 1) The detailed conditions for monitoring can be set from one site only.
- 2) Monitoring from other stations is possible without setting monitor files for other stations, but in this case, high-speed monitoring is not possible.
- 3) When simultaneous monitoring from multiple persons is desired, perform this operation before writing the parameter file or the program file in the built-in RAM.
If this operation is performed after writing the file in the built-in RAM, all files are erased.
- 4) The number of locations for simultaneous access to one CPU is up to 16.

8.10.2 Simultaneous execution of write during RUN by several people

The QnACPU allows simultaneous write during RUN to one file or another file by several people.

Operation Procedures

The following shows the procedures for simultaneous write during RUN executed by several people.

- (1) With "4/ Write & Conversion Setting" in "8/ Option" menu of the ladder mode, "4. Write During RUN Setting" and "7. Write Method at Write During RUN" are set.

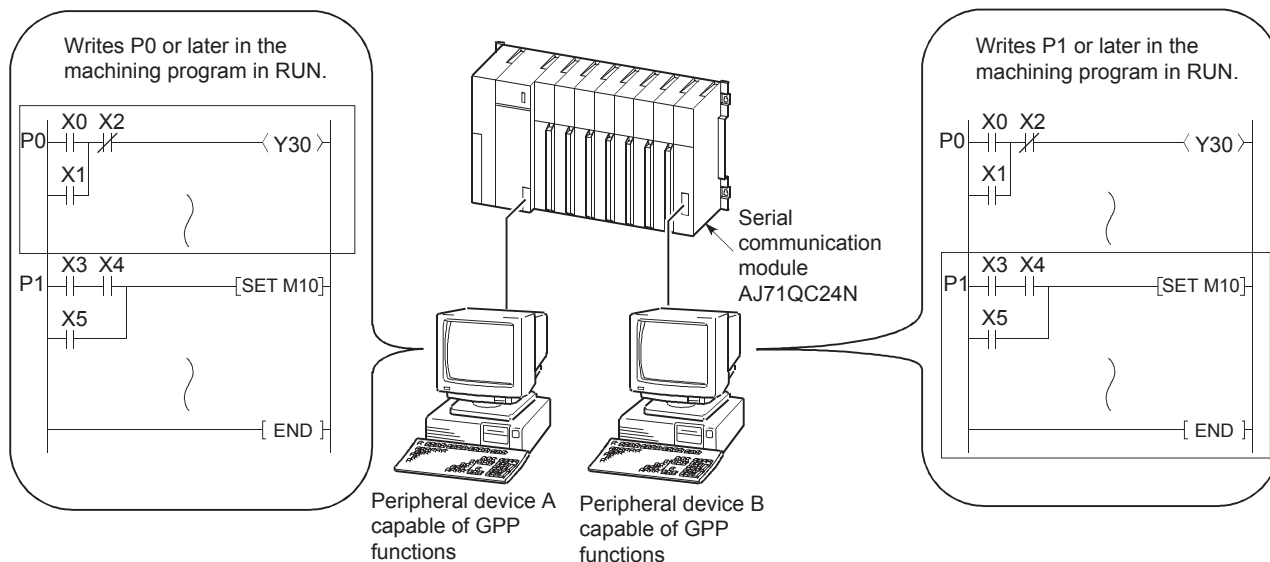
The following shows setting examples:

[Write & Conversion Setting]	
4. Write During Run Setting	1.<*) Write into PC during Run state. 2.<) Write into PC in Stop state. 3.<) Don't Write into PC.
7. Write Method at Write During Run	1.<*) Normal 2.<) Relatively using Pointer

- (a) Set "1. () Write into PC during Run state" for "4. Write During Run Setting".
- (b) Select "1. () Normal" or "2. () Relatively using Pointer" for "7. Write Method at Write During Run".

If more than one person is to perform a write during RUN operation with respect to the same file, set a write during RUN pointer in advance and select "2. () Relatively using Pointer".

The example below shows a case where peripheral device capable of GPP functions A performs write during RUN from P0, and peripheral device capable of GPP functions B performs write during RUN from P1. The program enclosed in the frame is the program subject to write during RUN.



NOTE

Refer to Section 8.3.

9 MAINTENANCE FUNCTION

9.1 Function List

The following shows the functions for maintenance.

Item	Description	Reference
Watchdog timer	Function that monitors watchdog errors due to CPU module hardware or program errors.	Section 9.2
Self-diagnostics function	Function whereby the QnACPU itself diagnoses whether or not there are any errors.	Section 9.3
Breakdown history	Function that stores the results of diagnosis in memory as a fault history.	Section 9.4
System protect	Function that sets whether reading/writing is enabled or disabled for QnACPU files.	Section 9.5
Keyword registration	Function that disables GPP function operations with respect to the CPU module.	Section 9.6
Online I/O module change	Function that allows replacement of I/O modules while the CPU module is in the RUN status.	Section 9.7
System display	Function that allows monitoring of the system configuration by connecting a peripheral device capable of GPP functions.	Section 9.8
LED indications	Function that indicates the operating state of the CPU module by means of LEDs or the LED indicator on the front face of the CPU module.	Section 9.9
	LED indication	Indicates whether CPU module operation is normal or abnormal. Section 9.9.1
	Priority setting	Priority for LED indication is set depending on the error. Section 9.9.2

For details on operations at GPP function, refer to the GX Developer Operating Manual or SW□IVD-GPPQ Operating Manual (Online).

9.2 Watchdog Timer

(1) Watchdog timer (WDT)

The watchdog timer is an internal timer of PLC that detects PLC CPU hardware errors and sequence program errors.

200ms is set as the default setting for this timer.

REMARK

The time set for the watchdog timer can be changed using "WDT" in PC RAS setting in the GPP function parameter mode.

The setting range is 10ms to 2000ms (in 10ms units).

(2) Resetting the watchdog timer

The QnACPU resets the watchdog timer during END processing.

When the QnACPU is normally operating and executing the END instruction within the setting value of the watchdog timer, the watchdog timer does not give time-out. WDT times out when the END instruction is not executed within the value set for the watchdog timer due to a QnACPU hardware error or an excessively long sequence program scan time.

REMARK

Scan time is the time taken for the execution of the sequence program, starting from step 0 and ending at step 0.

The scan time is not the same in every scan: it differs according to the execution or non-execution of the instructions used in the program. (Refer to Section 12.1.)

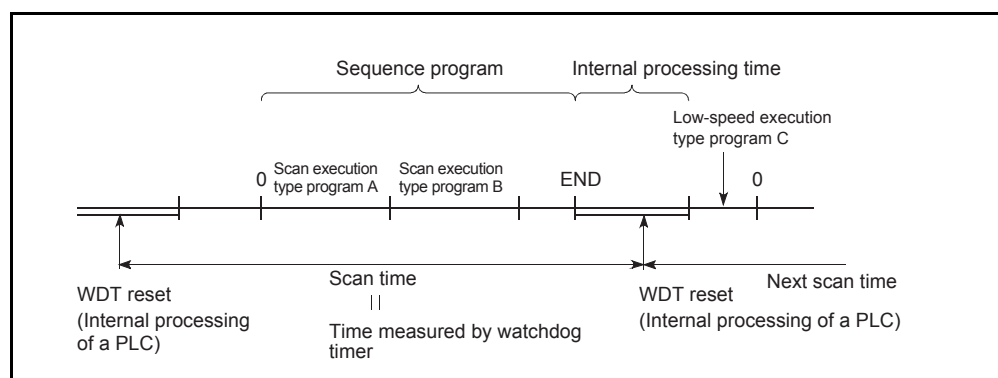


Fig. 9.1 Resetting the watchdog timer

- (3) Processing when the watchdog timer times out
When the scan time exceeds the set value of the watchdog timer, a watchdog timer error occurs and the PLC operates as follows.
- (a) All PLC outputs are turned OFF.
 - (b) The RUN LED on the front of the CPU module goes off and the ERROR LED flickers.
 - (c) SM1 turns ON and the error code is stored in SD0.

REMARK

The watchdog timer can be reset by a WDT instruction in the sequence program. However, the scan time value is not reset and scan time is measured up to the END instruction.

POINT

An error occurs within 0ms to 10ms in the measured time for watchdog timer.

9.3 Self-diagnostics Function

The self-diagnosis function is a function whereby the QnACPU diagnoses its own errors.

- (1) The self-diagnosis function serves to prevent malfunctions of the PLC, and to facilitate preventive maintenance. Self-diagnostics processing is executed if an error occurs at QnACPU power ON or while the PLC is in the RUN status, and it involves the display of the error detected by the self-diagnostics function, stopping of PLC operation, etc.
- (2) The QnACPU stores the error code corresponding to the error that has occurred in special register SD0, turns the ERROR LED on, and displays an error message on the LED indicator.
If several errors occur, the error code of the latest error is stored in SD0.
- (3) Even if the PLC power is turned OFF, the latest 16 errors are recorded with the battery backup. (Refer to Section 9.4.)
The PLC diagnostics mode of the GPP function can check error histories.
- (4) When an error is detected by self-diagnosis, CPU module operation complies with one of the following two modes:
 - Mode in which PLC operation is stopped
When an error is detected, operation is stopped immediately and all outputs (Y) are turned OFF.
 - Mode in which PLC operation is continued
When an error is detected, only the program part affected by the error is not executed; the rest of the program is executed.

In addition, settings can be made in PC RAS setting in the parameter mode to continue operation or stop operation when the following errors occur:

- 1) Calculation (including SFC programs)
- 2) Extended Ins
- 3) Fuse Blown
- 4) I/O Unit Compare
- 5) Sp Unit Access
- 6) IC Card Access
- 7) IC Card Operate

(The default for all of these in the parameters is "Pause".)

Example: If "Resume" is set for I/O module verify error, operation is continued using I/O address before error occurrence.

When an error is detected, a record of the error occurrence is stored in the special relays (SM0, SM1) and the error contents are stored in a special register (SD0). Use these special relays and this special register in the sequence program to establish PLC or mechanical system interlocks.

- (5) It is possible to select whether or not the following checks are performed by setting "Yes/No" for error check in PC RAS setting in the parameter mode.

- 1) Battery Check
- 2) Fuse Blown Check
- 3) I/O Unit Compare

(The default for all of these in the parameter settings is "Yes".)

If "No" is set for error check, error detection is not performed for these items, which shortens the processing time for the END instruction.

Even if "Yes" for error check is set in the parameter, 1) through 3), above error check, can be canceled by turning on the special relay SM1084.

However, if "No" is set in the parameter, turning off SM1084 is ineffective to execute the error check.

Self-diagnostics list

	Diagnosis Item	Diagnosis Timing	CPU Module Status	LED Status		LED Indicator Message (Q3A/Q4ACPU Only)
				RUN	ERROR	
Hardware error	CPU module error	Always	Stop	OFF	Flickers	MAIN CPU DOWN
	END instruction not executed	When executing END instruction	Stop	OFF	Flickers	END NOT EXECUTE
	RAM check	At power-ON or RESET	Stop	OFF	Flickers	RAM ERROR
	Operation circuit check	At power-ON or RESET	Stop	OFF	Flickers	OPE.CIRCUIT ERR.
	Fuse blown (Default ... stop)* ¹	When executing END instruction (Default ... check executed)* ²	Stop/Continue	OFF/ON	Flickering/ON	FUSE BREAK OFF
	I/O interrupt error	When interruption occurs	Stop	OFF	Flickers	I/O INT.ERROR
	Special function module error	• At power-ON or RESET • When executing FROM/TO instruction	Stop	OFF	Flickers	SP.UNIT DOWN
	Control bus error	• At power-ON or RESET • When executing FROM/TO instruction	Stop	OFF	Flickers	CONTROL-BUS ERR.
	Occurrence of momentary power interruption	Always	Continue	ON	OFF	AC DOWN
	Low battery	Always (Default ... check executed)* ³	Continue	ON	OFF	BATTERY ERROR
Handling error	I/O module verification (Default ... stop)* ¹	When executing END instruction (Default ... check executed)* ²	Stop/Continue	OFF/ON	Flickering/ON	UNIT VERIFY ERR.
	Special function module allocation error	• When power is ON or RESET • When switching from STOP to RUN	Stop	OFF	Flickers	SP.UNIT LAY.ERR.
	Special function module access error (Default ... stop)* ¹	When executing FROM/TO instruction	Stop/Continue	OFF/ON	Flickering/ON	SP.UNIT ERROR
	No parameters	When power is ON or RESET	Stop	OFF	Flickers	MISSING PARA.
	Boot error	When power is ON or RESET	Stop	OFF	Flickers	BOOT ERROR
	Memory card operation error (Default ... stop)* ¹	When memory card is inserted/removed	Stop/Continue	OFF/ON	Flickering/ON	ICM.OPE ERROR
	File setting error	When power is ON or RESET	Stop	OFF	Flickers	FILE SET ERROR
	File access error (Default ... stop)* ¹	When executing each instruction	Stop/Continue	OFF/ON	Flickering/ON	FILE OPE.ERROR
	Unable to execute instruction	When power is ON or RESET	Stop	OFF	Flickers	CAN'T EXE .PRG.
Parameter errors	Parameter setting check	• When power is ON or RESET • When switching from STOP to RUN	Stop	OFF	Flickers	PARAMETER ERROR
	Link parameter error	• When power is ON or RESET • When switching from STOP to RUN	Stop	OFF	Flickers	LINK PARA.ERROR
	SFC parameter error	When switching from STOP to RUN	Stop	OFF	Flickers	SFC PARA.ERROR

*1 Can be changed to operation continues by GPP function parameter setting.

*2 GPP function parameters can be set so that no check is performed, or so that no check is performed when SM251 is ON.

*3 GPP function parameters can be set so that no check is performed.

Self-diagnostics list(Continued)

Diagnosis Item		Diagnosis Timing	CPU Module Status	LED Status		LED Indicator Message (Q3A/Q4ACPU Only)
				RUN	ERROR	
Program error	Instruction code check	- When power is ON or RESET - When switching from STOP to RUN	Stop	OFF	Flickers	INSTRCT CODE ERR.
	No END instruction	- When power is ON or RESET - When switching from STOP to RUN	Stop	OFF	Flickers	MISSING END INS.
	Pointer setting error	- When power is ON or RESET - When switching from STOP to RUN	Stop	OFF	Flickers	CAN'T SET(P)
	Pointer setting error	- When power is ON or RESET - When switching from STOP to RUN	Stop	OFF	Flickers	CAN'T SET(I)
	Operation error (Default ... stop)*1	When executing each instruction	Stop/Continue	OFF/ON	Flickering/ON	OPERATION ERROR
	FOR-NEXT instruction configuration error	When executing each instruction	Stop	OFF	Flickers	FOR-NEXT ERROR
	CALL-RET instruction configuration error	When executing each instruction	Stop	OFF	Flickers	CAN'T EXECUTE(P)
	Interrupt program error	When executing each instruction	Stop	OFF	Flickers	CAN'T EXECUTE(I)
	Unable to execute instruction	When executing each instruction	Stop	OFF	Flickers	INST.FORMAT ERR.
	Extended instruction error (Default ... stop)*1	When executing each instruction	Stop/Continue	OFF/ON	Flickering/ON	EXTEND INST.ERR.
	SFC program configuration error	When switching from STOP to RUN	Stop	OFF	Flickers	SFCP.CODE ERROR
	SFC block configuration error	When switching from STOP to RUN	Stop	OFF	Flickers	CAN'T SET(BL)
	SFC step configuration error	When switching from STOP to RUN	Stop	OFF	Flickers	CAN'T SET(S)
	SFC syntax error	When switching from STOP to RUN	Stop	OFF	Flickers	SFCP.FORMAT ERR.
	SFC operation check error (Default ... stop)*1	When executing each instruction	Stop/Continue	OFF/ON	Flickering/ON	SFCP.OPE.ERROR
	SFC program execution error	When switching from STOP to RUN	Continue	ON	ON	SFCP.EXE.ERROR
	SFC block execution error	When executing each instruction	Stop	OFF	Flickers	BLOCK EXE.ERROR
	SFC step execution error	When executing each instruction	Stop	OFF	Flickers	STEP EXE.ERROR
CPU error	Watchdog error supervision	Always	Stop	OFF	Flickers	WDT ERROR
	Program timeout	Always	Continue	ON	ON	PRG.TIME OVER
Annunciator check		When executing each instruction	Continue	ON	OFF	F**** *4
CHK instruction check		When executing each instruction	Continue	ON	OFF	<CHK>ERR ***_*** -5

*1 Can be changed to operation continues by GPP function parameter setting.

*4 The detected annunciator number is displayed at ****.

*5 The detected contact and coil numbers are displayed at ***.

9.3.1 Interruption due to error detection

QnACPU can execute the interrupt program, which is interrupt pointer I32 to I39, at error occurrence.

In the case of errors for which operation can be set to continue or stop in PC RAS setting in the GPP function parameter mode, this function is only executed when "Resume" is set. If "Pause" is set for the error, a stop error interrupt program (I32) is executed.

The following shows the relevant errors.

Interrupt Pointer	Corresponding Error Message
I32	All stop errors
I33	Empty
I34	UNIT VERIFY ERR. FUSE BREAK OFF SP.UNIT ERROR
I35	OPERATION ERROR SFCP OPE.ERROR SFCP EXE.ERROR
I36	ICM.OPE.ERROR FILE OPE.ERROR
I37	EXTEND INS.ERR.
I38	PRG.TIME OVER
I39	CHK instruction Annunciator detect
I40 to I47	Empty

Errors for which the operation mode at the occurrence of the error is "Resume", or for which "Resume" is set if it is possible to select "Pause/Resume"

POINT
Interrupt pointers I32 to I39 are prohibited for execution when the PLC power is ON or when the CPU module is reset. To use I32 to I39, make the execution allowed with IMASK instruction.

REMARK

- 1) For details on interrupt pointers, refer to the QnACPU Programming Manual (Fundamentals).
- 2) For the IMASK instruction, refer to the QCPU (Q mode)/QnACPU Programming Manual (Common Instructions).

9.3.2 LED indication due to an error

In the case of an error occurrence, the LED/LED indicator on the front face of the CPU module gives a visual indication. For details on the operation of the LED, refer to Section 9.9.

9.3.3 Resetting error

The QnACPU can reset the errors only for the errors that continue operation of the CPU module.

The procedure for resetting an error is as follows.

- 1) Eliminate the cause of the error.
- 2) Store the error code to be reset in special register SD50.
- 3) Turn on special register SM50.
- 4) The error is reset.

If the CPU module is reset with the error reset, the special relay and special register relating to the error, and the LED/LED indicator, return to their status before error occurrence.

If the same error occurs again after the error reset, it is recorded in the error history again.

To reset multiple detected annunciators, only the first detected F number is reset.

POINT	
	When an error is reset by storing its error code in SD50, the last two digits of the error code are ignored. Example: If errors with error codes 2100 and 2111 have occurred, and error code 2100 is reset, error code 2111 is also reset.

9.4 Error History

QnACPU can record the results detected by the self-diagnostics function with the detection time in memory as an error history.

POINT
Since the internal clock of the QnACPU is used for setting the detection time, be sure to set the correct time before using the CPU module. (Refer to Section 10.5 for setting method of the clock.)

(1) Storage area

- (a) The latest 16 errors are stored in the error history storage memory of the CPU module, which is latched.
- (b) In the case of storing more than 16 errors, they can be stored to files in a memory card by making the appropriate setting in the PC RAS settings in the GPP function parameter mode.
- (c) If a discrepancy arises between the parameters and memory card error history when executing 1) or 2) below, the contents of the error history files are cleared first, and the 16-point data of the fault history storage memory of the CPU is transferred to the history file.
 - 1) The number of error records in the history file as set in the parameters is changed part way through.
 - 2) A memory card whose capacity does not match the number of error records set in the parameters is installed.
- (d) The following shows the storage area for the error history file:

Storage area	File in set memory card
Number of storable error records	Max. 100 (can be changed)*1

*1 When the number of errors that can be stored is exceeded, the oldest error record is cleared and the newest one stored in the same place.

POINT
Even if the error history file set in the parameters does not exist in the memory card, no CPU module error occurs. The CPU module performs only the processing that stores errors in the error history storage file.

(2) Clearing the error history

The error history is cleared by using the error history clear function in the PLC menu in the PLC diagnosis mode of GPP function.

The error history clear function erases all details in the error history storage memory of the CPU module and in the error history file of the memory card.

9.5 System Protect

QnACPU features a number of functions that protect against program changes ("system protect") by restricting general data processing (access processing from GPP functions, serial communication modules, etc.) by third parties other than designers.

The following system protect functions are available.

Target Protection	Valid File for Protection	Description	Method	Valid Timing	Remark
Whole of CPU module	All files	Batch prohibition of write/control to the CPU module.	Turn ON SW5 of system setting switch 1 on the main CPU module. (Refer to Section 15.2.)	Always	Valid for devices
Memory card units	All files	Establishes write protect for the memory card and prohibits writing.	Turn ON the memory card's write protect switch. (Refer to Section 18.5.)	Always	
Drive units	Parameter program	Registers entry codes for the following settings in relation to a specific drive (Example: Built-in RAM): 1) Prohibiting read/write display 2) Prohibiting writing	Register password. (Refer to Section 9.6.)	Always	
File units	All files	Changes attributes file for each file as follows: 1) Prohibiting read/write display 2) Prohibiting writing	Change file attributes by password registration. (Refer to Section 9.6.)	Always	

* "Control direction", "read/write display" and "writing" in the table above have the following meanings:

Item	Description
Control instruction	CPU module operation instruction by remote operation(Remote RUN, Remote STOP, etc.)
Read/write display	Operations of program read/write
Write	Operations that involve write processing, such as program write and test.

9.6 Password Registration

Passwords serve to prohibit reading and overwriting of data such as programs, comments, etc., in the QnACPU from a peripheral device.

In password registration, the parameter files and program files of a designated memory (built-in RAM, memory card) are made the target of the entry code. There are two types of registration as follows:

- File names are not displayed, and read/write are prohibited.
- File write is prohibited. (Read is possible).

When a password is registered, file operations from a peripheral device are not possible without inputting the entry code registered in the CPU module.

(1) Register Password

Entry codes are registered using the entry code registration function in the PLC menu of the online mode of GPP function.

```

[Register Password]
Current
1. Password [ ]
New
2. Operation 1.<*> Change [ ]
    1.<*> Read,Write and Display Protect
    2.<*> Write Protect
    2.<*> Cancel Password
    3.<*> None
    4.<*> Change Attribute
3. Memory 1.<*> Internal RAM
    2.[ ] IC Memory Card A(RAM)
    3.[ ] IC Memory Card A(ROM)
    4.[ ] IC Memory Card B(RAM)
    5.[ ] IC Memory Card B(ROM)
Execute<Y> Cancel<N>
Space:Select Esc:Close
  
```

The following shows an explanation of each item in the screen:

(a) Password.... When a password is registered in the CPU module, input the registered password so that file operations are executed.
When an incorrect password is input, file operations are not performed.

(b) Operation.... 1) Change : Register a new password in the CPU module.
Or, if the password matches, change the password.

① Read, Write and

Display Protect : File names in the designated memory cannot be displayed or written to.

② Write Protect

: Files in the designated memory cannot be written to. Read is possible.

2) Cancel

Password : If the password matches, the registered password is deleted from the CPU module.

3) None : The current password is recorded in the GPP function only and is not registered at the CPU module.

4) Change

Attribute : File read/write display or write can be prohibited in file units.

(Operation possible even if no entry code is registered.)

(c) Memory..... Designate the memory for which the password is to be registered.

POINT	
(1)	Password registration is valid for parameter files and program files only. Invalid for other file types. Other file types can be protected by changing attributes for each file.
(2)	The keyword registered in the CPU module cannot be read from the CPU module. If you forget the password, CPU module file operations will be impossible. Keep a record of the password, e.g. on paper, and store it in a safe place.
(3)	When a keyword is registered, memory for 1 file is occupied. (When a keyword is registered in the built-in RAM, 4k bytes are occupied.)

9.7 Online I/O Module Replacement

When an I/O module is installed or removed while the QnACPU power is ON, "UNIT VERIFY ERROR" appears, and PLC CPU operation stops or control is kept with I/O numbers that are different from the set numbers.

Replacing the I/O module during online is the replacement method that replaces the I/O module without "UNIT VERIFY ERROR" while the PLC CPU power is ON.

**CAUTION**

- Basically, replace I/O modules after turning off the power supply.

When replacing I/O modules during online using the function in this section, perform it according to the user system specification.

POINT

Replacing I/O modules during online is possible only for I/O module.
This is not applied to special function modules.

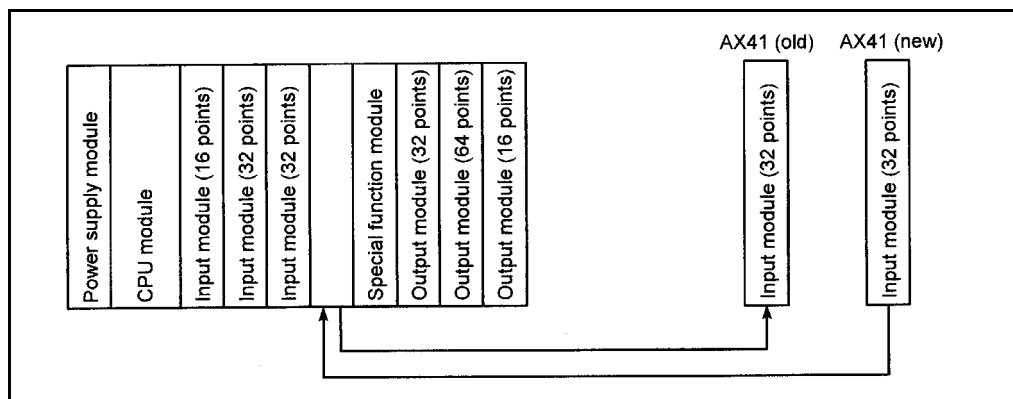


Fig. 9.2 Replacing input modules during online

- (1) Application
Replacing I/O modules during online is used to replace an I/O module at which an error has occurred while continuing control by the sequence program.
- (2) Replacement method
The following two methods can be used to replace an I/O module during online.
 - (a) Use "Connect Unit" in the PLC menu in the GPP function PLC diagnostics mode.
 - (b) Use special relays/special registers.
- (3) Procedure when using GPP function
 - (a) Designate the I/O module to be replaced with "Connect Unit" of the PLC menu in the PLC diagnostics mode.
 - (b) Replace the designated I/O module.

- (4) Procedure when using special relays/special registers
- (a) Use the following procedure when using special relays/special registers:
- 1) Set the first two digits of the three-digit expression for the head I/O number of the I/O module to be replaced in SD251 (replaced I/O module head I/O No. storage register).
Example: Head I/O No. = 070 → set number is H07
Head I/O No. = 170 → set number is H17
 - 2) Turn ON SM251 (I/O replacement flag).
 - 3) Confirm that SM252 (replacement enabled flag) comes ON first, and replace the designated I/O module.
 - 4) Turn OFF SM251. (SM252 is turned OFF automatically.)
- (b) Setting data in SD251 and turning ON/OFF SM251 can be done either by using the sequence program or a peripheral device.

(a) Method when Using a Sequence Program	(b) Method when Using GPP function
A sequence program of the type shown below can be used to replace a designated I/O module while the QnACPU is in the "RUN" status. * The sequence program shown above can be written from GPP function in the RUN status. Procedure (1) Turn ON the input condition, and set the number of the I/O module to be replaced in SD251 and turn ON SM251. (2) Confirm that output Y** has come ON first, and replace the designated I/O module. (3) Turn OFF the input condition, and turn OFF SM251. (This starts operation of the module after replacement.)	A designated I/O module can be replaced in the GPP function test mode. Any of RUN, STOP, or PAUSE status is possible for the QnACPU. Procedure (1) Connect a peripheral device capable of GPP functions to the QnACPU. (2) In the test mode, set the first two digits of the head I/O number of the module to be replaced in SD251. (3) In the test mode, set (turn ON) SM251. (4) In the monitor mode, confirm that SM252 has come ON , and replace the designated I/O module. (5) In the test mode, reset (turn OFF) SM251. (This starts operation of the module after replacement.)

REMARK

- 1) While SM251 is ON, the QnACPU does not perform the module verify and the fuse blown check. After replacing the module, turn OFF SM251 immediately.
- 2) "100H" is stored in SD251 as the default value.

9.8 System Display

The following items can be checked by connecting a peripheral device capable of GPP functions to the QnACPU:

- (1) The following information relating to the modules actually mounted on the base unit:
 - (a) Type
 - (b) No. of Occupied Points
 - (c) Head X/Y number

- (2) The following module information set in the parameters:
 - (a) Type
 - (b) No. of Occupied Points
 - (c) Type Name

- (3) The following information relating to the CPU module:
 - (a) Status of the RUN/STOP key switch
 - (b) Status of the system setting switches
 - (c) LED statuses

These items can be checked using the detail HELP display and CPU module panel items in the display menu of the GPP function PLC diagnostics mode.

9.9 LED Indications

The QnACPU module has LEDs on its front face that indicate the operating status of the CPU module.

In addition, Q3ACPU and Q4ACPU feature a LED indicator.

The following shows the meanings of the LED and LED indications.

9.9.1 LED indication

(1) The following shows the meanings of the indications of each of the LEDs are given.

LED Name	Indication Detail
RUN	Indicates the operating status of the CPU module. ON: Operating with the RUN/STOP key switch set to RUN or STEP RUN. OFF: Operation is stopped, with the RUN/STOP key switch in the STOP, PAUSE, or STEP RUN position. An error that stops operation has been detected. Flickering: The RUN/STOP key switch has been turned from STOP to RUN after writing a program in the STOP status. To light, either turn the RUN/STOP key switch RUN→STOP→RUN, or reset operation using the RUN/STOP key switch.
ERROR	Indicates the CPU module error detection status. ON: A self-diagnostics error that does not stop operation, other than a battery error, has been detected.(The operation mode at error occurrence has been set to "Resume" in PC RAS setting in the parameter mode.) OFF: Normal Flickering: An error that stops operation has been detected.
USER	Indicates the CHK instruction detection status, and annunciator (F) statuses. ON: An error has been detected by the CHK instruction, or an annunciator F has come ON. OFF: Normal Flickering: Executing latch clear.
BAT.ALARM	Indicates the battery statuses of the CPU module itself and the memory card. ON: A battery error has occurred due to low battery voltage. OFF: Normal
BOOT	Indicates status of the boot operation execution. ON: Execution has been completed. OFF: The boot operation has not been executed.

- (2) The following shows how to turn OFF an LED that is currently ON.(Excluding the reset operation).

Method for Turning OFF the LED	LED Name			
	ERROR	USER	BAT. ALARM	BOOT
Resolve the cause of the error, then execute the LEDR instruction.	○	○	○	×
Eliminate the cause of the error, then reset the error using special relay SM50 and special register SD50.(Restricted to error which do not stop operation.)* ¹	○	○	○	×
Turn OFF the LED by using special relay SM202 and special register SD202. * ¹	×	○	×	○

○: Valid ×: Not valid

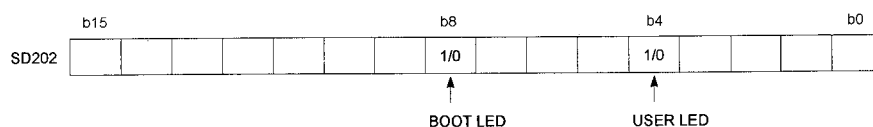
*¹ Explanation of special relays and special registers

SM50..... When turning OFF → ON, resets the error corresponding to the error code stored in SD50.

SD50..... Stores the error code of the error to be reset.
(For details on error codes, refer to Section 22.3.3.)

SM202..... When turning OFF → ON, turns OFF the LEDs corresponding to each of the bits of SD202.

SD202..... Designates the LED to be turned OFF.(The LEDs that can be turned OFF are the USER LED and the BOOT LED only.)



A bit setting of "1" indicates that the bit is to be turned OFF, "0" indicates that it is not to be turned OFF.

The following shows the setting possibilities (all hexadecimal notation):

- To turn both LEDs OFF: SD202 = 110H
- To turn only the BOOT LED OFF: SD202 = 100H
- To turn only the USER LED OFF: SD202 = 10H

- (3) Method for stopping ERROR LED, USER LED, and BAT.ALARM LED indications
- ERROR LED, USER LED and BAT. ALARM LED have the same priority order as described for display of Priority setting in Section 9.9.2.
- If an error item number is deleted from this order of priority, the LED does not light even if the error corresponding to that error item number occurs.
- (For details on the setting method, refer to the POINT in Section 9.9.2.)

9.9.2 Priority setting

In addition to LEDs, the Q3ACPU and Q4ACPU are provided with an LED indicator on the front face of the CPU module.

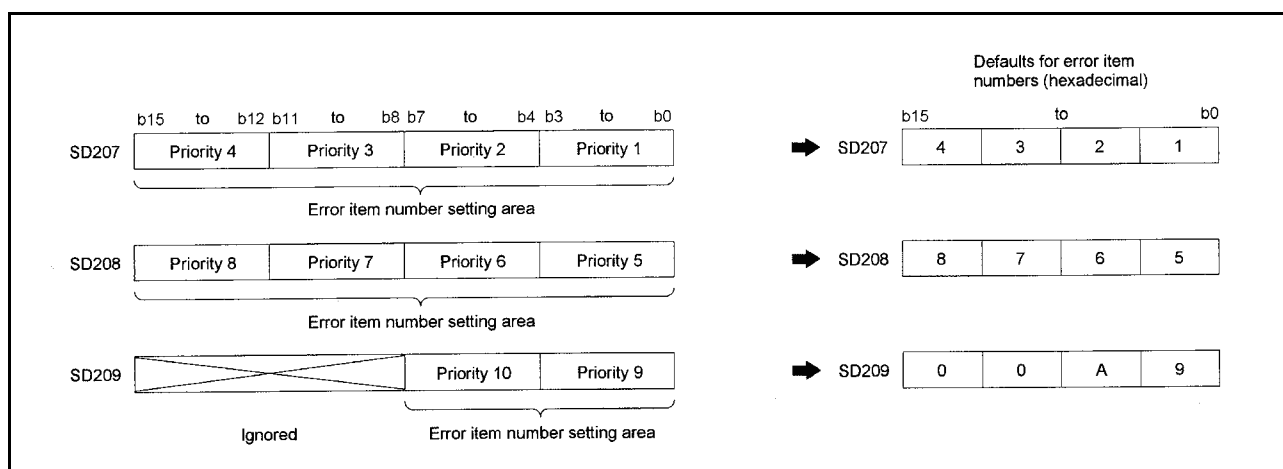
This indicator shows the following items:

- 1) Error message
- 2) CHK instruction numbers
- 3) Annunciator numbers, annunciator comments, the time when an annunciator was switched ON, etc.
- 4) Character string and comment displays in accordance with LED instructions
- 5) Clock data

If several errors occurred at a time, the indication conforms to the following conditions.

- 1) Stop error is indicated unconditionally.
- 2) Operation continue error are indicated in accordance with error item numbers in an order of priority set by default.
Priorities can be changed.(set with special registers SD207 to SD209)
- 3) If several errors with the same priority occur, a first detected error is indicated.

The following shows how to set priorities in special registers SD207 to SD209.



The following shows the details of the error item numbers and default for priorities which is set in special registers SD207 to SD209.

Order of priority	Error Item No. (Hex.)	Description	Remark
1	1	AC DOWN	AC power/DC power OFF
2	2	UNIT VERIFY ERR. FUSE BREAK OFF SP.UNIT ERROR	I/O module verification Fuse blown Special function module access error
3	3	OPERATION ERROR LINK PARA.ERROR SFCP OPE.ERROR SFCP EXE.ERROR	Operation error Link parameter error SFC instruction operation error SFC program execution error
4	4	ICM.OPE.ERROR FILE OPE.ERROR EXTEND INST.ERROR	Memory card operation error File access error Extended instruction error
5	5	PRG.TIME OVER	Constant scan setting time over error Low-speed execution monitoring timeout
6	6	CHK instruction	
7	7	Annunciators ^{*1}	
8	8	LED instruction	
9	9	BATTERY ERR.	
10	A	Clock data	

^{*1} For annunciators, it is possible to set alternating displays of comment and occurrence time by parameter setting (PC RAS setting).

Example: When setting to display comments and occurrence time in PC RAS setting in the parameter mode:



[Display of the 2nd occurrence time or later]

The occurrence time is displayed for the first annunciator only.

The second time or later are displayed as follows:

"--M--D--:--:--".

[Display of the 2nd comment or later]

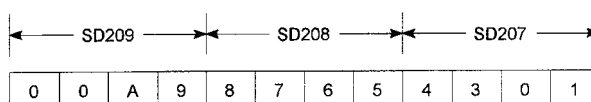
To display the 2nd annunciator comment or later, perform the following:

- Create one comment file.
- To create the comment file with the same file name as the program, describe the comment of the annunciator used for all comment files.

POINT

- (1) When LED and LED indicator are left OFF for the error occurrence above, set the factor number area to 0, which stores the applicable factor numbers from SD207 to SD209.

Example: To set the ERROR LED to remain OFF and the LED indicator to remain blank when a fuse blown error occurs, set "0" in the item number setting area whose item number is "2".



Since the item number "2" is not set, the ERROR LED and the LED indicator remains OFF even if a fuse blown error is detected. The ERROR LED and the LED indicator also remain OFF even if another error whose error item number is "2" is detected (I/O module verify error, special module access verify error).

- (2) Even if the LED and the LED indicator are set to remain OFF, SM0 (the diagnostics error flag) is still turned ON, SM1 (the self-diagnostics error flag) is still turned ON, and the error code is stored in SD0 (CPU diagnosis error register).

- (1) A displayed message can be cleared by the same procedure as used to turn an LED OFF. (Refer to Section 9.9.1 (2).)
However, if there are several display causes at a time, the next message is displayed when the currently displayed message is cleared.

10 OTHER FUNCTIONS

10.1 Function List

The following list shows the rest of the functions.

Item	Description	Reference
Constant scan	Performs a program at fixed intervals regardless of the actual program scan time.	Section 10.2
Latch function	Retains the device data when resetting the CPU module while the PLC power is OFF.	Section 10.3
Setting of the output status when switching from STOP to RUN	Sets the output (Y) status when the CPU module is switched from STOP to RUN (Re-outputting the outputs before STOP/Outputting the outputs after performing operation).	Section 10.4
Clock function	Runs the internal clock of the CPU module.	Section 10.5
Remote operation	Operates the QnACPU from a remote place.	Section 10.6
Remote RUN/STOP	Starts or stops the CPU module operation.	Section 10.6.1
Remote STEP-RUN	Performs a step operation to the CPU module.	Section 10.6.2
Remote PAUSE	Suspends the CPU module operation.	Section 10.6.3
Remote RESET	Resets the CPU module.	Section 10.6.4
Remote latch clear	Clears the CPU module latch data.	Section 10.6.5
Relationship between remote operation and CPU module RUN/STOP key switch	Explains the relationship between the CPU module RUN/STOP key switch setting and operation when performing remote operation.	Section 10.6.6
Terminal setting	Uses the Q6PU programming unit's indicator and key input.	Section 10.7
Message display	Displays messages on the indicator of the Q6PU.	Section 10.7.1
Key input operation	Reads key input from the Q6PU.	Section 10.7.2
Reading module access time intervals	Monitors the access time intervals (The time between the acceptance of one CPU module access and the acceptance of the next CPU module access) for special function modules, network modules, and peripheral devices.	Section 10.8

For details of GPP function operation, refer to the GX Developer Operating Manual or the Type SW□IVD-GPPQ GPP Software package Operating Manual (Online).
For details of the Q6PU operation, refer to the Q6PU Operating Manual.

10.2 Constant Scan

(1) Constant scan

In the QnACPU, the scan time varies since the processing time differs depend on the execution status of the instructions used in the sequence program.

Constant scan is a function whereby the sequence program is repeatedly performed while maintaining constant scan time.

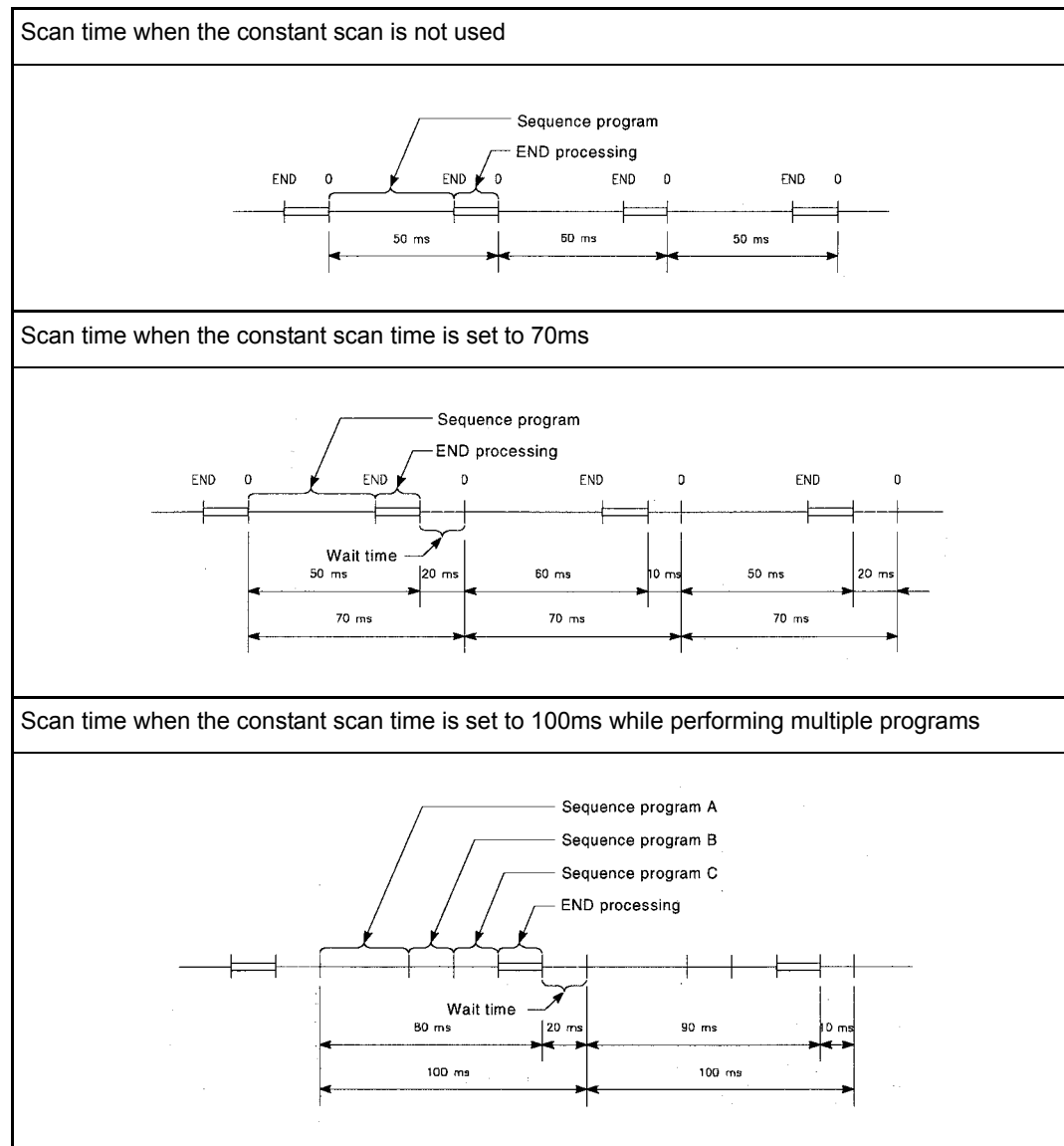


Fig. 10.1 Constant scan operation

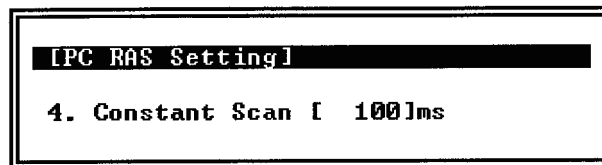
When the low-speed execution type program is used, either this constant scan function or a low-speed program execution time has to be set.

(For details, refer to the QnACPU Programming Manual (Fundamentals).)

10. OTHER FUNCTIONS

- (2) Setting the constant scan time
 - (a) The setting is made in "PC RAS" in the parameter mode of GPP function.
 - When performing the constant scan, set the constant scan time.
 - When not performing the constant scan, leave the field blank.

Example: When setting 100ms to "Constant scan"



- (b) Set constant scan time that is longer than the maximum scan time of the sequence program. If the scan time of the sequence program is longer than the set value for constant scan time, the QnACPU detects an error code (SD0 = 5010), and the sequence program is performed in the own scan time, ignoring the constant scan time setting.

Make sure that the constant scan time setting is shorter than the set time for WDT (Watchdog timer). If it is longer than the set time for WDT, the QnACPU detects a WDT error and the program execution is stopped.

Set the constant scan time within the following range.

Setting time for WDT > Setting time for constant scan > Maximum scan time of sequence program

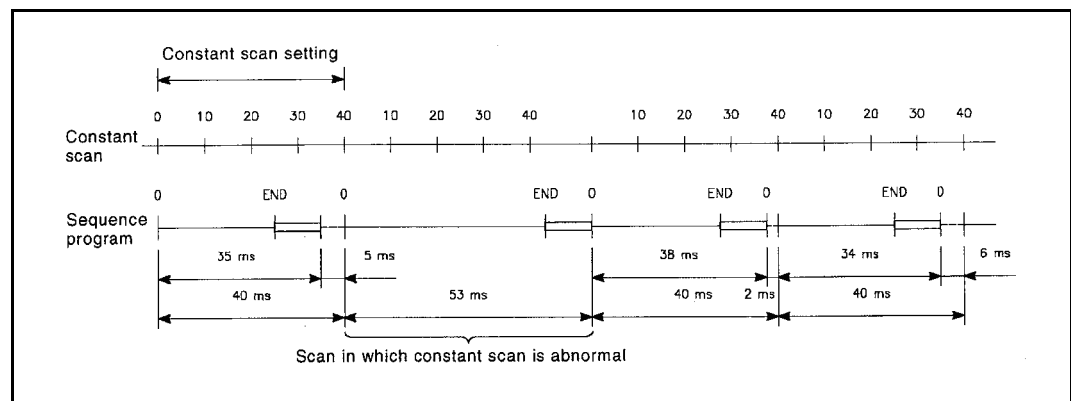


Fig. 10.2 Operation when scan time is longer than constant scan setting time

- (c) Sequence program processing is suspended in the wait time between the END processing of the sequence program and the start of the next scan. However, if an interrupt factor occurs after the execution of END processing, or if there is a low-speed execution type program, the interrupt program or the low-speed execution type program is performed.

(d) Constant scan time error

If there is a low-speed execution type program when performing the constant scan, the constant scan time may be shifted by the time shown below.

$$(\text{Error}) = \left[\begin{array}{l} \text{Maximum processing time} \\ \text{of one instruction in the} \\ \text{low-speed execution type} \\ \text{program} \end{array} \right] + \left[\frac{\text{low-speed END processing time}}{\left(\begin{array}{l} \text{Time taken to execute the END} \\ \text{processing for a low-speed} \\ \text{execution type program} \end{array} \right)} \right]$$

The low-speed execution type program is divided and performed within surplus time. Therefore, if one constant scan ends while performing the instruction takes long processing time, the constant scan is completed after finishing the processing of the instruction during execution. The time extended to complete the execution of the instruction is the constant scan error. For details of the instruction processing time, refer to the QCPU (Q mode)/QnACPU Programming Manual (Common Instructions).

10.3 Latch Function

When the PLC power is turned ON, the CPU module is reset using the RUN/STOP key switch, or a instantaneous power failure lasting longer than the allowable momentary power interruption time occurs, the all device values in the QnACPU are cleared, and the default values are set in the devices (Bit devices: OFF, word devices: 0).

The latch function retains the data in the devices when performing these operations. The operations in the program are the same whether or not the latch function is used.

(1) Application of the latch function

The latch function can be used when continuing the control to retain data such as production quantities, numbers of defects, addresses, etc., even if a instantaneous power failure longer than the allowable time occurs.

(2) Devices that can be latched

(a) The following devices can be latched.

- 1) Latch relay
- 2) Link relay
- 3) Annunciator
- 4) Edge relay
- 5) Timer
- 6) Retentive timer
- 7) Counter
- 8) Data register
- 9) Link register

POINT

Even if a latch designation is set for a device, the device will not be latched if a local device designation or device initial value designation is made.

(b) The latch range is set on the "Device" in the parameter mode of GPP function.

In latch range setting, it is possible to set a range within which the latch clear key is effective (Latch (1) Start) and a range within which the key is not effective (Latch (2) Start). For details on device latch ranges for each device, refer to the QnACPU Programming Manual (Fundamentals).

POINT

The devices data in the latch range are retained by the battery (A6BAT) installed in the CPU module.

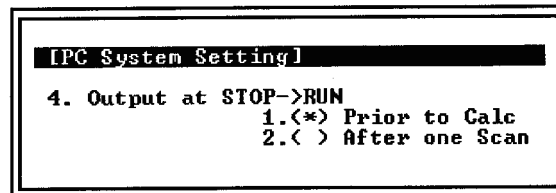
- (1) Even if a sequence program is written to a memory card and ROM operation is performed, the battery is required for the latch function.
- (2) If the battery connector is disconnected from the CPU module connector while the PLC power is OFF, the devices data in the latch range is lost.

- (3) Clearing the device data in the latch range
 - (a) To clear the devices data in a latch range and set the default values instead, perform "Latch clear". When the latch clear is performed, the devices data in the non-latched range is also cleared.
However, the devices for which the latch clear key has been set to Disable in the Parameter are not cleared by performing latch clear.
 - (b) For the methods of performing latch clear, refer to Section 12.4.

10.4 Setting of the Output (Y) Status When Switching from STOP to RUN

When the RUN or other status is changed to the STOP status, the CPU module stores the output (Y) in the RUN status into the PLC and turns all outputs (Y) OFF.

In this function, whether to re-output the outputs (Y) when switching from STOP to RUN or to output them after an operation can be set in the "PC system" in the parameter mode of GPP function .



- (a) Re-output (Prior to Calc).....The output (Y) status immediately before the STOP status is output, and then the sequence program is calculated.
- (b) Output after operation execution (After one Scan).....The output is OFF status. The output (Y) will be output after the sequence program operation is executed.

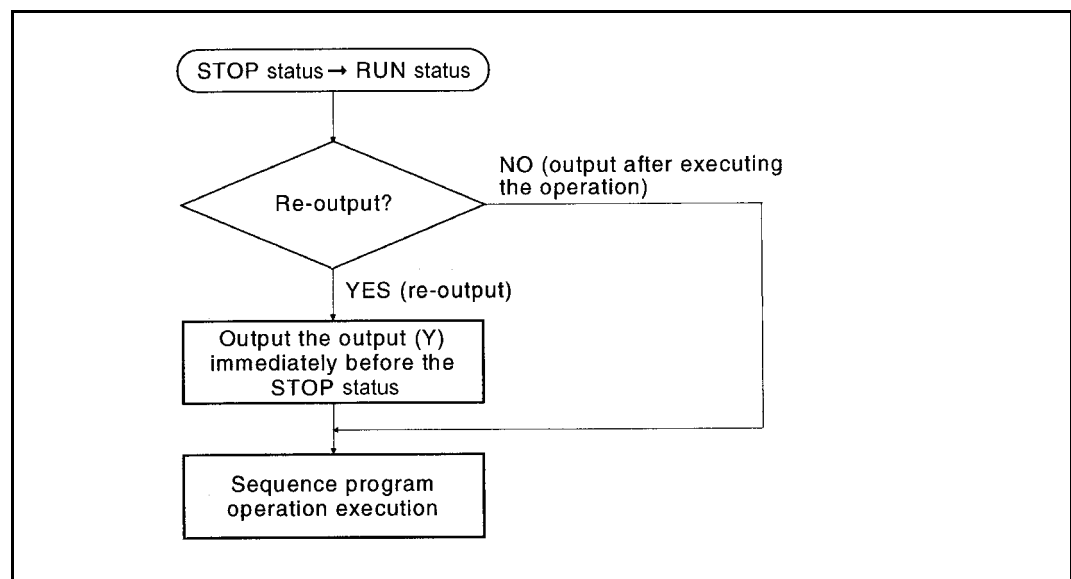


Fig. 10.3 Processing when a PLC is switched from STOP to RUN

10.5 Clock Function

The QnACPU has a clock in the CPU module.

Since the clock data can be read in the sequence program, it can be used for time control of the user system.

In addition, the clock data can also be used for time control to the functions performed by the CPU module, such as the breakdown history.

Clock operation by the clock function is continued with the battery when the PLC power is turned OFF or a instantaneous power failure lasting longer than the allowable momentary power interruption time occurs.

POINT	
	The CPU module system uses the clock data for a breakdown history. When using a CPU module, be sure to set the correct time first.

(1) Clock data

The clock data is composed of the year, month, day, hour, minute, second, and day of the week used by the clock element in the PLC CPU, as shown below.

Data name	Description	
Year	Last two digits of the year	
Month	1 to 12	
Day	1 to 31 (Leap year, automatic identification)	
Hour	0 to 23 (24-hour system)	
Minute	0 to 59	
Second	0 to 59	
Day of the week	0	Sunday
	1	Monday
	2	Tuesday
	3	Wednesday
	4	Thursday
	5	Friday
	6	Saturday

(2) Accuracy

The accuracy of the clock function depends on the ambient temperature, as shown below.

Ambient Temperature	Accuracy (daily variance)
0°C	-2.3s to + 4.4s (TYP. + 1.8s)
+25°C	-1.1s to + 4.4s (TYP. + 2.2s)
+55°C	-9.6s to 2.7s (TYP.-2.4s)

(3) Writing clock data to the clock elements

(a) Use the following procedure to write clock data to the clock elements.

1) Writing from a peripheral device

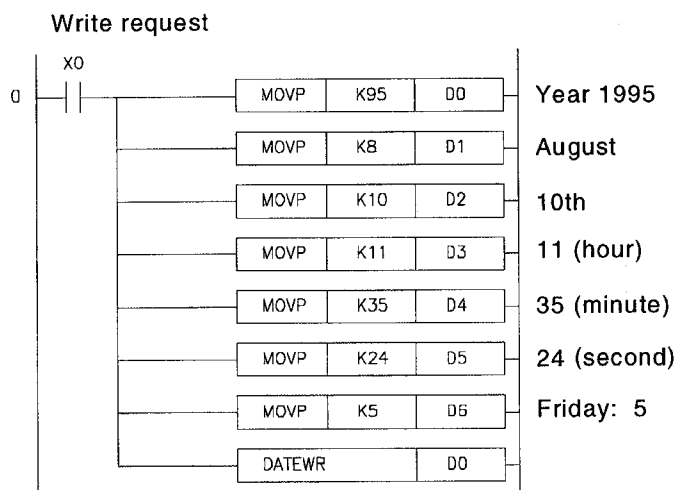
- When using GPP function, clock data can be written to the clock elements using the "Set clock" of the PLC menu in PLC diagnostics mode.
- When using the Q6PU, clock data can be written to the clock elements by using the clock monitor option in the monitor functions of the PLC system in the other mode.

(For details on the operation for each peripheral device, refer to the Operating Manual for each.)

2) Writing from a program

Clock data is written to the clock elements using the clock instruction (DATEWR).

The following shows the example of the program.



For details on the DATEWR instruction, refer to the QCPU (Q mode)/QnACPU Programming Manual (Common Instructions).

POINT

- (1) Clock data is not written to clock elements in advance. Write clock data to the clock elements before using the QnACPU.
- (2) Even if partly changing the clock data, rewrite all data to the clock elements.
- (3) If the nonexistent time is written to the clock elements, normal clock operation is impossible.

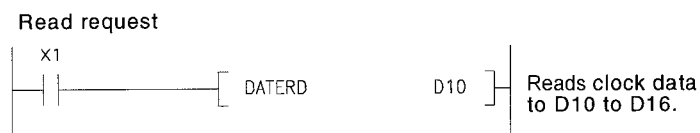
Example

Setting "13" to the month.
Setting "32" to the date.

(4) Clock data read

- (a) To read clock data to data registers, use the clock data read instruction (DATERD) in the program.

An example of a program using the instruction is shown below.

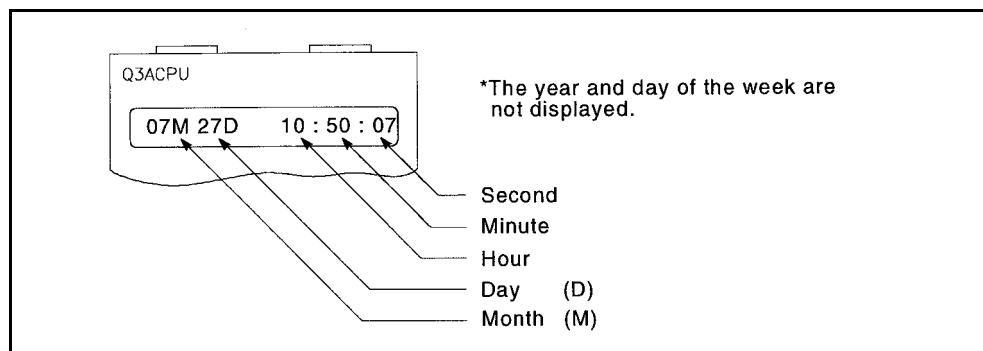


For details on the DATERD instruction, refer to the QCPU (Q mode)/QnACPU Programming Manual (Common Instructions).

- (b) To read the clock data to SD210 to SD213, turn SM213 ON from a sequence program or a peripheral device.
- (c) When using the CPU module with a 16-character LED indicator on the front panel, the clock data (Month, day, hour, minute, second) can be displayed on the LED indicator.

To display the clock data on the LED indicator, turn SM212 ON.

The clock data display has the lowest priority of any LED display, therefore, it will not be displayed if other message is displayed due to an error occurrence, etc.



(5) Special relays and special registers for reading/writing clock data

The section explains the special relays and special registers used for setting data and reading clock data for clock operation.

(a) Special relays used for the clock function

Device	Name	Description
SM210	Clock data set request	- Writes clock data to the special registers (SD210 to SD213) and performs clock operation. - Writes the clock data stored in SD210 to SD213 to the clock elements after execution of the END instruction in the scan in which SM210 turns from OFF to ON.
SM211	Clock data error	- Used to determine whether or not there are any errors when the clock data is set. - Turns ON if any data is not a BCD cord.
SM212 ^{*1}	Clock data display	- Displays clock data on the LED indicator on the front panel of a CPU module. - When SM212 is ON, the clock data is displayed on the LED indicator on the front panel of the CPU module.
SM213	Clock data read request	- Reads the clock data stored in special registers SD210 to SD213. - When SM213 is ON, the clock data is read to SD210 to SD213 after execution of the END instruction.

^{*1} Can only be used with the Q3ACPU and Q4ACPU.

(b) Special registers used for clock data

Device	Name	Description																
SD210	Clock data (year, month)	The year and month are recorded as follows. The year data is the last two digits of the year. b15 to b8 b7 to b0 Month (value in range 01 to 12 stored in BCD) Year (value in range 00 to 99 stored in BCD)																
SD211	Clock data (day, hour)	The day and hour are recorded as follows. b15 to b8 b7 to b0 Hour (value in range 00 to 23 stored in BCD) Date (value in range 01 to 31 stored in BCD)																
SD212	Clock data (minute, second)	The minute and second are recorded as follows. b15 to b8 b7 to b0 Second (value in the range 00 to 59 stored in BCD) Minute (value in the range 00 to 59 stored in BCD)																
SD213	Clock data (day of the week)	- The day of the week is recorded as follows. b15 to b4 b3 to b0 Day of the week (value in the range 0 to 6 stored in BCD) "0" is stored. - The settings for the day of the week are as follows: <table><tr><td>Day of the week</td><td>Sun</td><td>Mon</td><td>Tue</td><td>Wed</td><td>Thu</td><td>Fri</td><td>Sat</td></tr><tr><td>Storage data</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td></tr></table>	Day of the week	Sun	Mon	Tue	Wed	Thu	Fri	Sat	Storage data	0	1	2	3	4	5	6
Day of the week	Sun	Mon	Tue	Wed	Thu	Fri	Sat											
Storage data	0	1	2	3	4	5	6											

10.6 Remote Operation

With the QnACPU, the operating status of the CPU module can be controlled from external sources (GPP function, intelligent special function module, remote contact, etc.).

REMARK

In this chapter, a serial communication module is used as an example of an intelligent special function module.

10.6.1 Remote RUN/STOP

Remote RUN/STOP refers to the function that sets the QnACPU to RUN or STOP from an external source while the CPU module RUN/STOP key switch is set to the RUN position.

(1) Application of remote RUN/STOP

Remote RUN/STOP operation from remote location is useful in the following cases.

- (a) When the CPU module is installed in an inaccessible location
- (b) When setting the CPU module in a control panel to RUN/STOP from an external source

(2) Operation for remote RUN/STOP

The following shows the program operations to which remote RUN/STOP is performed.

- (a) Remote STOP..... The program is performed up to the END instruction, then STOP state is established.
- (b) Remote RUN..... When remote RUN is performed with the CPU in STOP set by remote STOP, the program will be in RUN state again and be performed from step 0.

(3) Method for performing remote RUN/STOP

The following two methods are available for performing remote RUN/STOP.

(a) Method using a remote RUN contact

The remote RUN contact is set in the PLC system in the parameter mode of GPP function.

The settable device range is from input X0 to 1FFF.

Remote RUN/STOP can be performed by switching the remote RUN contact ON/OFF.

- 1) When the remote RUN contact is OFF, the CPU module is in RUN state.
- 2) When the remote RUN contact is ON, the CPU module is in STOP state.

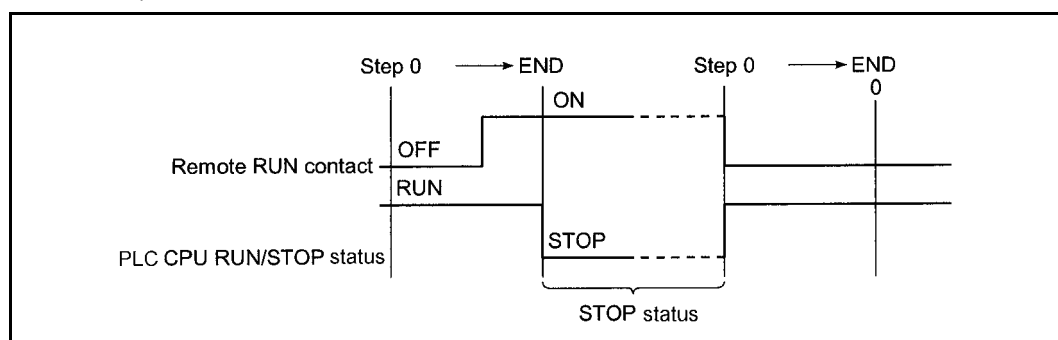


Fig. 10.4 Time chart for RUN/STOP switching with remote RUN contact

- (b) Method using GPP function, serial communication module, etc.

The CPU module can be set to RUN or STOP by remote RUN/STOP operation from GPP function, or a serial communication module, etc.

The operation using GPP function can be performed in the Remote operation of the PLC menu in any mode.

The control using a serial communication module is performed with the commands in the dedicated protocol.

For details on serial communication module control, refer to the Serial Communication Module User's Manual.

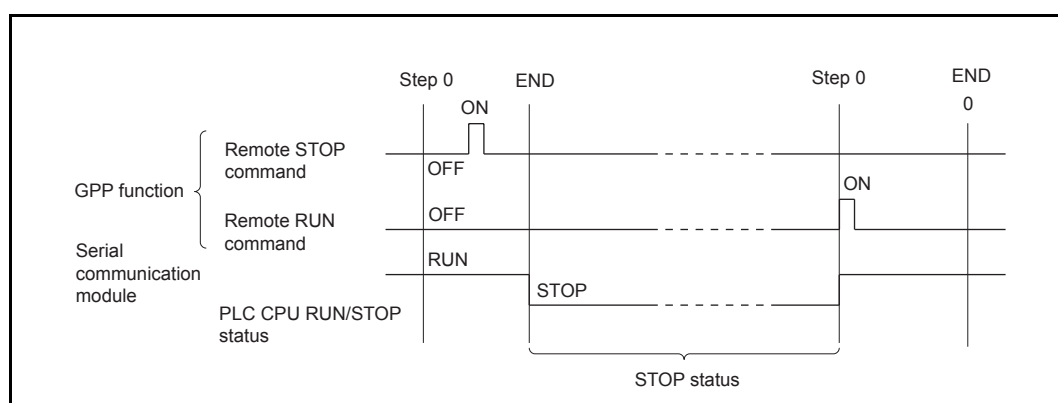


Fig. 10.5 Time chart for remote RUN/STOP switching with GPP function or a serial communication module

(4) Precautions

- (a) Since the STOP state has a priority in the QnACPU, pay attention to the following points.

- 1) In the QnACPU, if remote STOP is performed from any one of remote RUN contact, GPP function, serial communication module, etc., the QnACPU will be STOP.
- 2) In order to set the QnACPU to RUN again after it has been set to STOP by remote STOP, all external factors which set remote STOP (Remote RUN contact, GPP function, serial communication module, etc.) have to be set to RUN.

REMARK

The RUN/STOP status is defined as follows.

- RUN status..... Status in which the sequence program is repeatedly performed from step 0 to the END instruction.
- STOP status..... Status in which the sequence program operation is stopped and all outputs (Y) are OFF.

10.6.2 Remote STEP-RUN

Remote STEP-RUN refers to the function whereby the step run of the QnACPU is performed from GPP function while the RUN/STOP key switch of the module is in RUN position.

"Step run" is program execution that operates by one step at a time, starting from the designated step.

For details on step run, refer to Section 8.7.

(1) Application of remote STEP-RUN

When debugging the system, for example, the program can be performed while checking its execution and the contents of each device.

(2) Method for performing remote STEP-RUN

The procedure for remote STEP-RUN is as follows.

- 1) Set the RUN/STOP key switch of the CPU module to RUN position.
- 2) Perform STEP-RUN operation with GPP function.

10.6.3 Remote PAUSE

Remote PAUSE refers to the function that performs PAUSE function to the QnACPU from an external source while the CPU module RUN/STOP key switch is set to the RUN position.

The PAUSE function stops a CPU module operation while retaining the ON/OFF status of all outputs (Y).

(1) Application of remote PAUSE

This function can be used to retain the output (Y) with ON status even if the CPU module is in STOP due to process control.

(2) Methods for remote PAUSE

The following two methods are available for performing remote PAUSE.

(a) Method using a remote PAUSE contact

The remote PAUSE contact is set in the PLC system in the parameter mode of GPP function.

The settable device range is from input X0 to 1FFF.

- 1) When the scan END processing is performed with both the remote PAUSE contact and the PAUSE enable flag (SM206) are ON, the PAUSE status contact (SM204) turns ON.

When performing up to the END instruction of the scan following the scan in which the PAUSE status contact turned ON, the PAUSE state is established and operation is stopped.

- 2) When turning the remote PAUSE contact OFF or turning SM206 OFF with GPP function, the PAUSE status is reset and the sequence program operation is again performed from step 0.

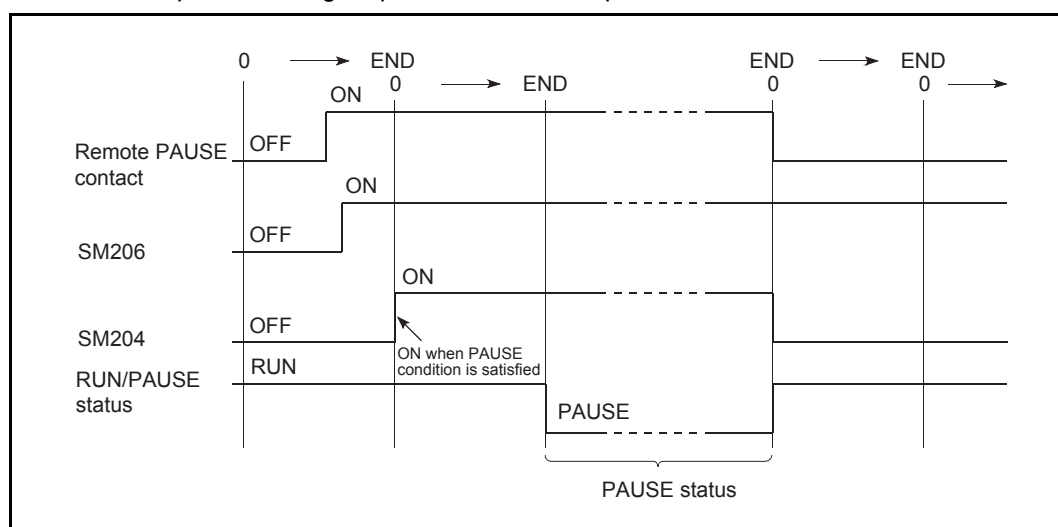


Fig. 10.6 Time chart for PAUSE with remote PAUSE contact

REMARK

When the remote RUN contact is made same as the remote PAUSE contact, the remote PAUSE contact will be invalid.

(b) Methods using GPP function or a serial communication module

The remote PAUSE operation can be performed from GPP function or from a serial communication module.

The operation using GPP function can be performed in the Remote operation of the PLC menu in any mode.

The control using a serial communication module is performed with the commands in the dedicated protocol.

For details on serial communication module control, refer to the Serial Communication Module User's Manual.

- 1) When the END processing of the scan in which the remote PAUSE command has received from GPP function is performed, the PAUSE status contact (SM204) turns ON.

When performing up to the END instruction of the scan following the scan in which the PAUSE status contact turned ON, the PAUSE status is established and the operation is stopped.

- 2) When the remote RUN command is received from GPP function, the sequence program operation is again performed from step 0.

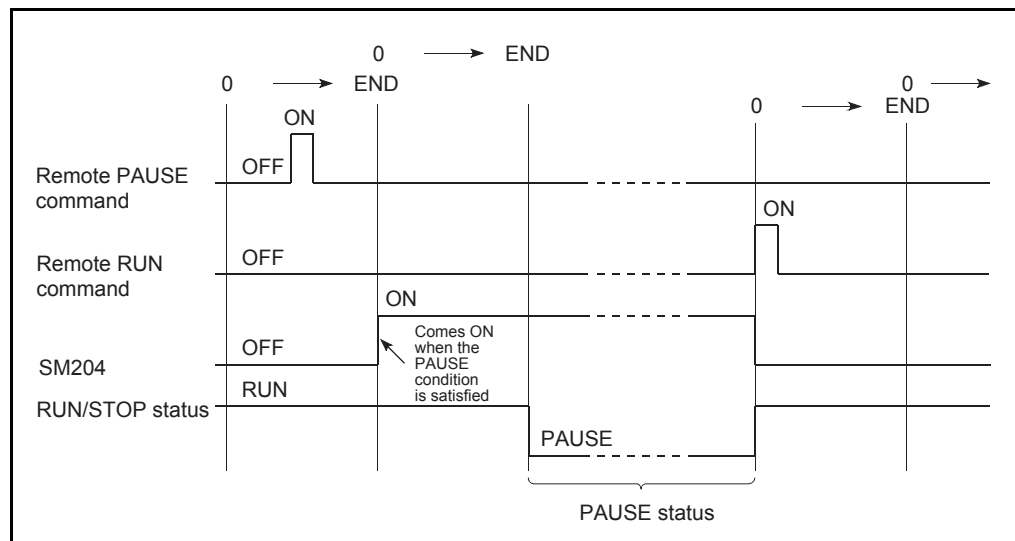
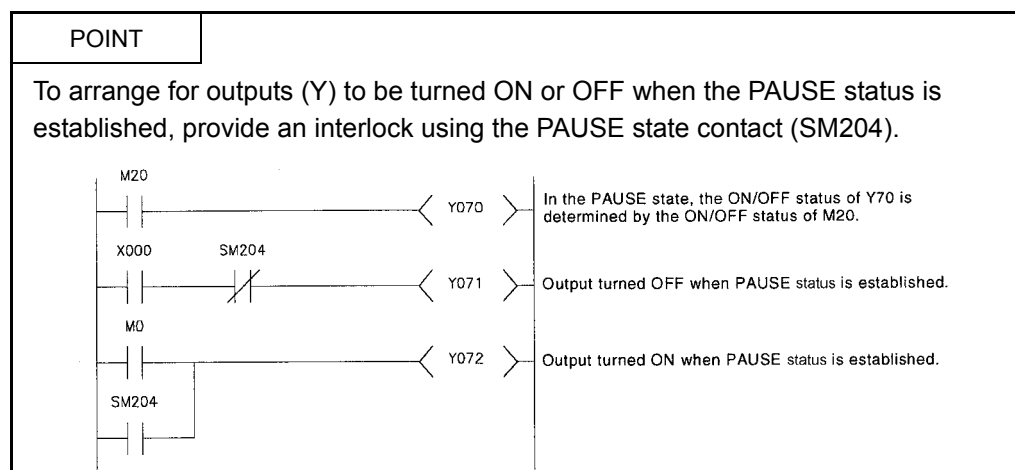


Fig. 10.7 Time chart for PAUSE with GPP function



10.6.4 Remote RESET

Remote RESET is a function for resetting the QnACPU by operation from an external device while the CPU module is in STOP.

Resetting is also possible even when the RUN/STOP key switch on the CPU module is set to the RUN position if the CPU module is stopped by an error detectable by the self-diagnostics function.

POINT	
	Remote RESET cannot be performed when the CPU module is in RUN.

(1) Application of remote RESET

Remote RESET can be used to reset the CPU module by remote operation when an error has occurred in the place from where the CPU module cannot be directly operated.

(2) Methods for remote RESET

Remote RESET can only be performed by operation from GPP function or a serial communication module.

- (a) Regardless of whether reset is performed from GPP function or a serial communication module, the setting to enable remote RESET has to be made in the Parameter before performing the reset operation.

The remote RESET "Enable/Disable" setting is made in the PLC system in the parameter mode of GPP function.

- (b) When the parameter is set to "Allow" in the "Remote reset" and written to the CPU module, resetting is performed with remote operation.
- When using GPP function, perform the reset in the PLC menu in any mode.
 - When using a serial communication module, perform the reset with dedicated protocol commands.

For details on serial communication module control, refer to the Serial Communication Module User's Manual.

10.6.5 Remote latch clear

Remote latch clear is a function for resetting the latched device data of the QnACPU while the CPU module is in STOP by using such as a GPP function.

POINT	
Remote latch clear cannot be performed when the CPU module is in RUN.	

- (1) Application of remote latch clear
Remote latch clear is useful for latch clear operation when the CPU module is at the locations below: In this case, the function is used in combination with the remote RUN/STOP function.
 - When the CPU module is installed in an inaccessible location
 - When performing latch clear to the CPU module in a control panel from an external source
- (2) Methods for remote latch clear
Remote latch clear can only be performed by operation from GPP function or a serial communication module.
 - The operation using GPP function can be performed in the Remote operation of the PLC menu in any mode.
 - The control using a serial communication module is performed with the commands in the dedicated protocol.

For details on serial communication module control, refer to the Serial Communication Module User's Manual.

POINT	
1. According to the device latch ranges set in "Device" in parameter mode, there are ranges within which latch clear is valid and ranges within which it is not valid. Remote latch clear is only valid for devices set in the range for which "Latch clear valid" is set. 2. When remote latch clear is performed, devices that are not latched are also cleared.	

10.6.6 Relationship between remote operation and CPU module RUN/STOP key switch

Using the combination of the remote operation and the RUN/STOP key switch of the CPU module explained in Section 10.6.1 through Section 10.6.5, the operating status of the QnACPU is determined as follows.

Key switch	Remote Operation					
	RUN* ¹	STEP-RUN	STOP	PAUSE* ²	RESET* ³	Latch Clear
RUN	RUN	STEP-RUN	STOP	PAUSE	Operation is not possible.* ⁴	Operation is not possible.* ⁴
STOP	STOP	STOP	STOP	STOP	RESET	Latch Clear

*1 If performed using a remote RUN contact, beforehand set "RUN-PAUSE contacts" in the PLC system in parameter mode.

*2 If performed using a remote PAUSE contact, beforehand set "RUN-PAUSE contacts" in the PLC system in parameter mode. Furthermore, the remote PAUSE enable coil (SM206) has to be turned ON in advance.

*3 "Remote reset" field in the PLC system has to be set to "Allow" in parameter mode.

*4 The operation status can be RESET if the CPU module is stopped by remote operation.

When the RUN/STOP key switch is set to RUN and multiple remote operation requests are received, the CPU module first performs the operation with the highest priority.

Remote operation	RUN	STEP-RUN	STOP	PAUSE	RESET	Latch Clear
Order of priority	4)	3)	1)	2)	-	-

The order of priority increases from (4) to (1).

10.7 Terminal Operation

This function sets the Q6PU programming unit in the terminal mode and performs the data communications shown below by using the instructions for peripheral devices of the QnACPU.

- 1) Display of messages from the QnACPU on the display of the Q6PU.
- 2) Storage of the Q6PU key input data in the devices of the QnACPU.

In this way, the Q6PU can be used as a terminal of the QnACPU.

These functions are explained from the next section.

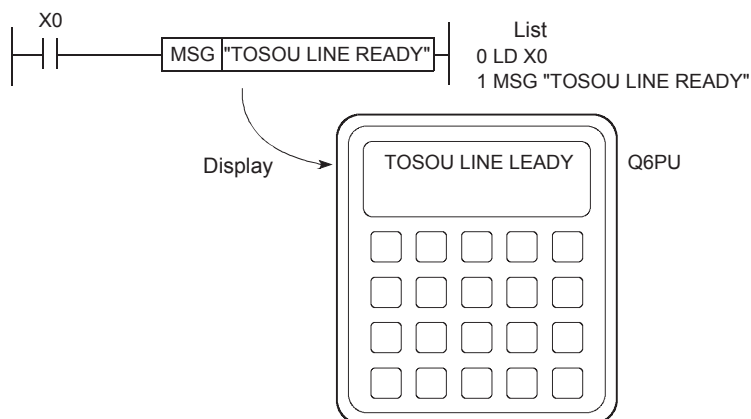
However, for details on the instructions for peripheral devices, refer to the QCPU (Q mode)/QnACPU Programming Manual (Common Instructions).

10.7.1 Operation for message display

Specified character strings can be displayed on the Q6PU using the MSG instruction for peripheral devices.

Furthermore, character strings can be displayed with GPP function by using the CPU messages of the Display menu in the PLC diagnostics mode.

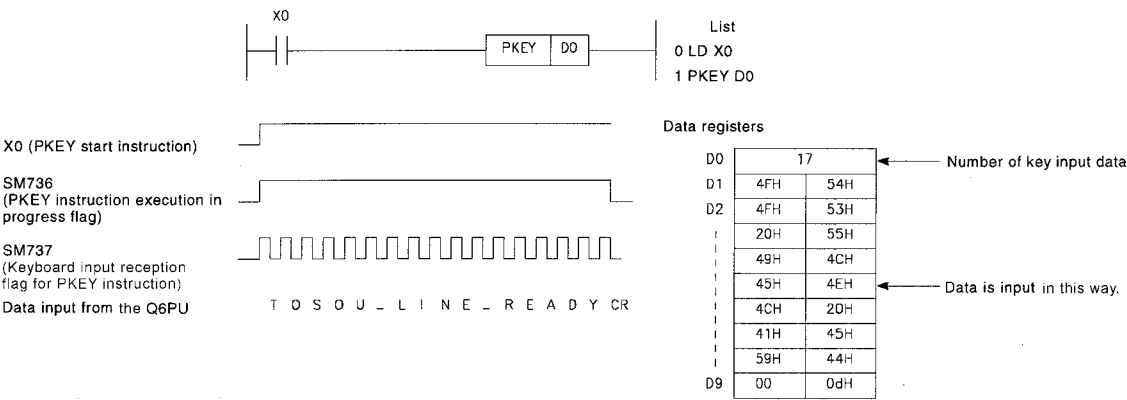
Example: Program to display "TOSOU LINE READY" as a message No.1 on the Q6PU when X0 is turned ON.



10.7.2 Key input operation

Character string data input at the Q6PU can be stored as ASCII data without change in specified devices by using the PKEY instruction for peripheral device. Data input ends when a CR code is input or when the 32nd character is input.

Example: Program to input "TOSOU LINE READY" on the Q6PU when X0 is turned ON.



10.8 Reading Module Access Time Intervals

The QnACPU can monitor the access interval time (The time between one access reception and the next access reception) for intelligent special function modules, network modules, data link modules, or GPP function. This enables to grasp the frequency of accesses to the CPU module from external sources.

The operation for reading the module access interval time involves the following special relay and special registers.

(1) Special relay

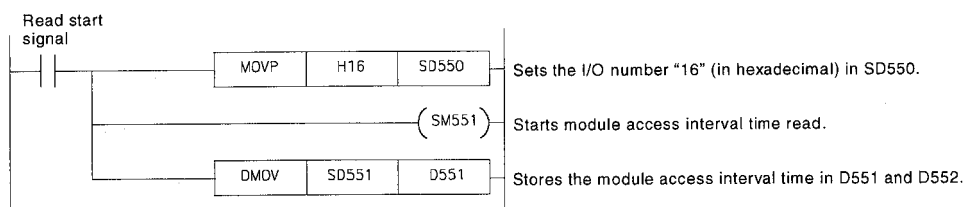
Number	Name	Description
SM551	Read module service interval	When this relay turns from OFF to ON, the module access interval time for the special function module specified in special register SD550 is read into special registers SD551 to SD552. ON : Read OFF : Ignored

(2) Special register

Number	Name	Description
SD550	Service interval measurement module	Set the I/O number of the module whose access interval time is to be measured. Set the I/O number of the peripheral device connected to the RS-422 interface of the CPU module to FFFFH. Also set the I/O number of the upper 2 digits in the 3-digit representation.
SD551 to SD552	Service interval time	When SM551 is turned ON, it stores the interval time for access from the module specified at SD550. SD551: 1ms units (Range: 0 to 65535) SD552: 1 μ s units (Range: 0 to 900, stored every 100 μ s) Example: When the module access interval time is 123.4ms: SD551=123, SD552=400

Program example:

Program for reading the module access interval time of the special function module at X/Y160.



POINT

To read the access interval time for access from GPP function at another station in the network, set the I/O number of the network module.

REMARK

- The module access interval includes a transient request interval such as a monitor, a test and a program read/write.
The access interval via cyclic communication from a network module or a data link module is not stored.

11 COMMENTS THAT CAN BE STORED IN QnACPU

11.1 Function List

The QnACPU can store various types of comments. This has improved the CPU module operability, allowing users other than programmers to read programs easily.
The types of comments that can be stored in the QnACPU are listed in the table below.

Item	Function	Refer to
PLC name	Naming the CPU module to be used.	Section 11.2
Drive title	Assigning a title to each drive.	Section 11.3
File title	Assigning a title to each file.	Section 11.4
Device comment	Assigning comments and/or labels to devices used in a program.	Section 11.5
Statements/notes	Assigning comments to each program step number or P or I pointer.	Section 11.6
Initial device value comment	Assigning a comment to the initial device value file.	Section 11.7

For details on the setting method for each function, refer to the GX Developer Operating Manual or SW□IVD-GPPQ Operating Manual (Offline).

11.2 PLC name

PLC name appends a comment to a CPU module to make it easier to confirm the CPU module when accessing the QnACPU by GPP function.

Two types of PLC names can be set: labels and comments. The settings are made on the "Define PC name" screen in the parameter mode of GPP function.

```

[Define PC Name]
1. Label [SYSTEM ]
2. Comment [SYSTEM No.1]
Execute<Y> Cancel<N>
Space:Select Esc:Close
  
```

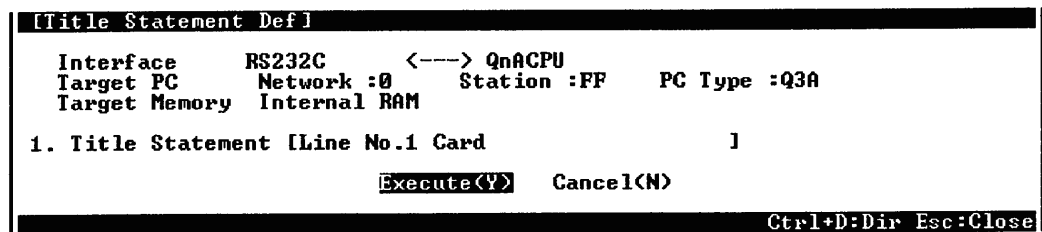
The setting details are indicated in the table below.

Item	Setting	Setting range	Default value
Label	Set a label for the CPU module.	Up to 10 characters	No setting
Comment	Set a comment for the CPU module.	Up to 64 characters	

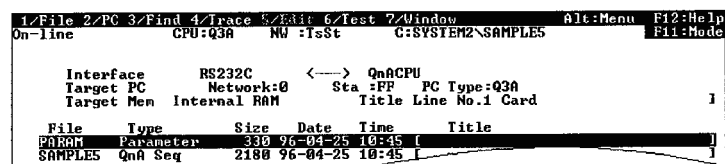
11.3 Drive Title

The drive title function assigns a title to a drive to allow users to easily identify what file is stored in the built-in RAM or memory card.

Drive titles are created on the "Title Statement Def" screen under the PC menu in the online mode of GPP function.



A created title is displayed on the screen as shown below.



POINT

Note that creating a drive title uses an area equivalent to one file in each memory.

11.4 File Title

The file title function allows file titles to be assigned to files so that the contents of the files can be figured out.

File titles are set in file setting performed when starting GPP function, or in PLC writing from the PLC menu in any mode. Up to 32 characters can be used.

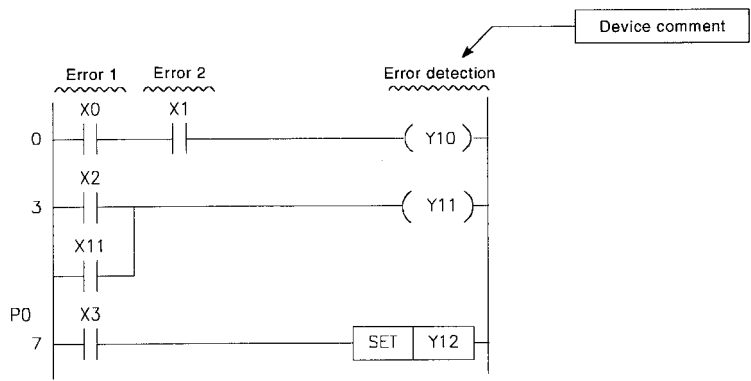
[Create]				
1. Drive/Path	IC:\GPPQ\USR			1
2. System	[SYSTEM1]	Title	[System No.1	1
3. Machine	[TRANSFER]	Title	[Transfer Line	1
4. File	[LINE1]	Title	[Line No.1 Program	1
		Execute<Y>	Cancel<N>	
Ctrl+L:List Ctrl+D:Dir Space:Select Esc:Close				

File titles are stored in the corresponding created files.

Note that they are not stored in any files for file registers.

11.5 Device Comment

The device comment function displays comments assigned to respective devices so that programs can be read easily.
In addition, by setting "Xtype" for the CPU type with GPP function, programs can be created using labels instead of devices.



POINT
A memory card is required to create device comments and store a device comment file in a CPU module.

- (1) Device comments are set in the documentation mode of GPP function.
Up to 32 characters are used for each comment and up to 10 characters for each label (device label name).

1/ File 2/ PC 3/ Find 5/ Edit 7/ Window 8/ Option										Alt: Menu		F12: Help
Document	Device	CPU: Q3A		C:\SYSTEM2\SAMPLES				<Ins>		F11: Mode		
	Device	Comment				Device Label						
	X	0	[	12345678901234567890123456789012	]	1	[	1234567890	]			
	X	1	[		]	2	[		]			
	X	2	[		]	3	[		]			
	X	3	[		]	4	[		]			
	X	4	[		]	5	[		]			
	X	5	[		]	6	[		]			
	X	6	[		]	7	[		]			
	X	7	[		]	8	[		]			
	X	8	[		]	9	[		]			
	X	9	[		]							
	X	A	[		]							

- Comments and labels can be assigned to the following devices.
Device name: X, Y, M, L, F, SM, B, SB, V, T (present value), C (present value), ST (present value), D, SD, W, SW, R, ZR, P, I, U□\G□,
J□\X, J□\Y, J□\B, J□\SB, J□\W, J□\SW, BL□\S, BL□\TR
(When P or I comments are used as pointers for programs such as subroutine or interrupt programs, they are not displayed. To display these comments, make them displayed as pointer statements. (Refer to Section 11.6))

- (2) When using comments with application instructions (LEDC, PRC, etc.), if a device comment file has been written to the CPU module, enable one of the options in the parameter setting for the device comment file.
- This setting is made at "2. Comment file used in a command" on the "PLC file" screen in the parameter mode of GPP function.

[PC File Setting]	
1. File Register	3. Device Initial Value
1.<*> Not Used	1.< > Not Used
2.< > Program Name is Used	2.<*> Program Name is Used
Drive []	Drive [0]
3.< > Use the Following Files	3.< > Use the Following Files
Drive []	Drive []
File []	File []
Capacity [] K	
2. Comment File Used by Instruction	4. File for Local Device
1.<*> Not Used	1.<*> Not Used
2.< > Program Name is Used	2.< > Use the Following Files
Drive []	Drive []
3.< > Use the Following Files	File []
Drive []	
File []	
Execute<Y> Cancel<N>	
Space:Select Esc:Close	

The setting details are as follows:

1. "Not Used":

No setting is made for the comment file to be used. To use the comment file, use the QCDSET instruction. (For details on the QCDSET instruction, refer to the QCPU (Q mode)/QnACPU Programming Manual (Common Instructions).)

2. "Program Name is Used":

Use the comment file with the same file name as the program that exists in the specified drive and is currently being executed.

When the program is changed, the comment file is also changed.

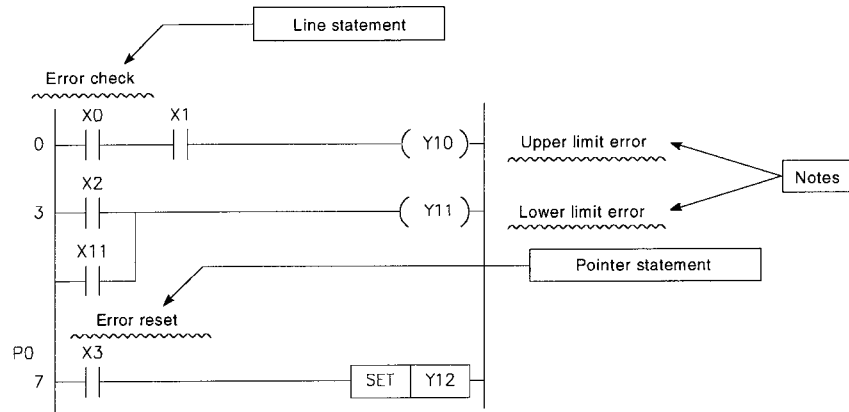
3. Using the designated device comment file:

Use the name of the file that is stored in the drive specified by the parameter.

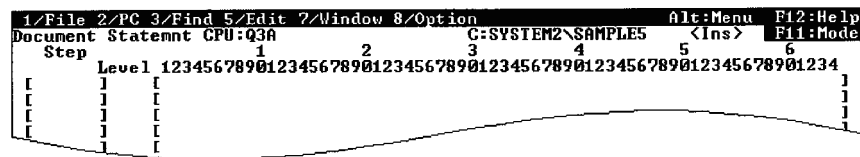
POINT
(1) When using the QCDSET instruction, note the following points. (a) When the above 1) or 2) has been set, the file set with the QCDSET instruction is valid for all program files. (b) When 3) is set, the file set with the QCDSET instruction is valid only for the program file for which the QCDSET instruction is executed. (2) Even if the file set with the parameter does not exist in the specified drive, no CPU module error is generated. Since no file exists, however, the CPU module does not display any comments.

11.6 Statements/Notes

Statements and notes are assigned to each program step, or to P or I pointers, in order to facilitate program reading.



- (1) Statements or notes are set on the "Pointer statement", "Statement", or "Note" screen displayed from the edit menu in the documentation mode of GPP function.



- (2) The details of each comment are as follows:
 - (a) Statement (Line statement)

A comment can be appended to a ladder block provided for individual function to explain the meaning and usage of the function.
 - (b) Pointer statement

A comment can be appended to a pointer placed in the head of a subroutine or interrupt program to explain the meaning and usage of each program.
 - (c) Note

A comment can be appended to individual ladder blocks to explain the meaning and usage of the function.

11.7 Initial Device Value Comment

Initial device value comments are assigned to initial device value files so that individual file contents can be figured out.

Initial device value comments are stored in an initial device value file.

They are set on the "Device Initial Value Range" screen displayed from the edit menu in the device mode of GPP function.

[Device Initial Value Range]				
#	# of Dev	First Device	Last Device	Comment
1	[16]	[D0	] -> [D15	] Production Indication data
2	[0]	[	] -> [	] 1
3	[0]	[	] -> [	
4	[0]	[	] -> [	

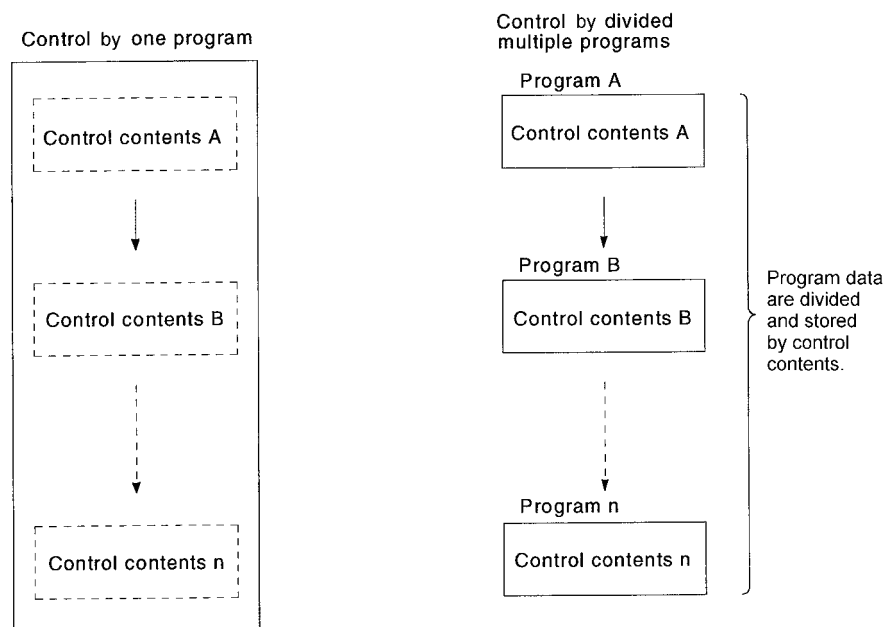
12 OVERVIEW OF PROCESSING PERFORMED BY THE QnACPU

12.1 Program Execution Types

Programs to be executed by the QnACPU are stored in the built-in RAM of the CPU module or in a memory card.

While all of the data can be stored as one program in the built-in RAM or a memory card, they can be also divided into several programs based on control units and stored.

When programming is undertaken by more than one designer, all the programming process can be divided into several parts based on the processing units for each designer and all of the programming data can be stored in the built-in RAM of a CPU module or a memory card.



When dividing a program data into multiple programs, set "execution type" for each program in program setting in the parameter mode of GPP function.

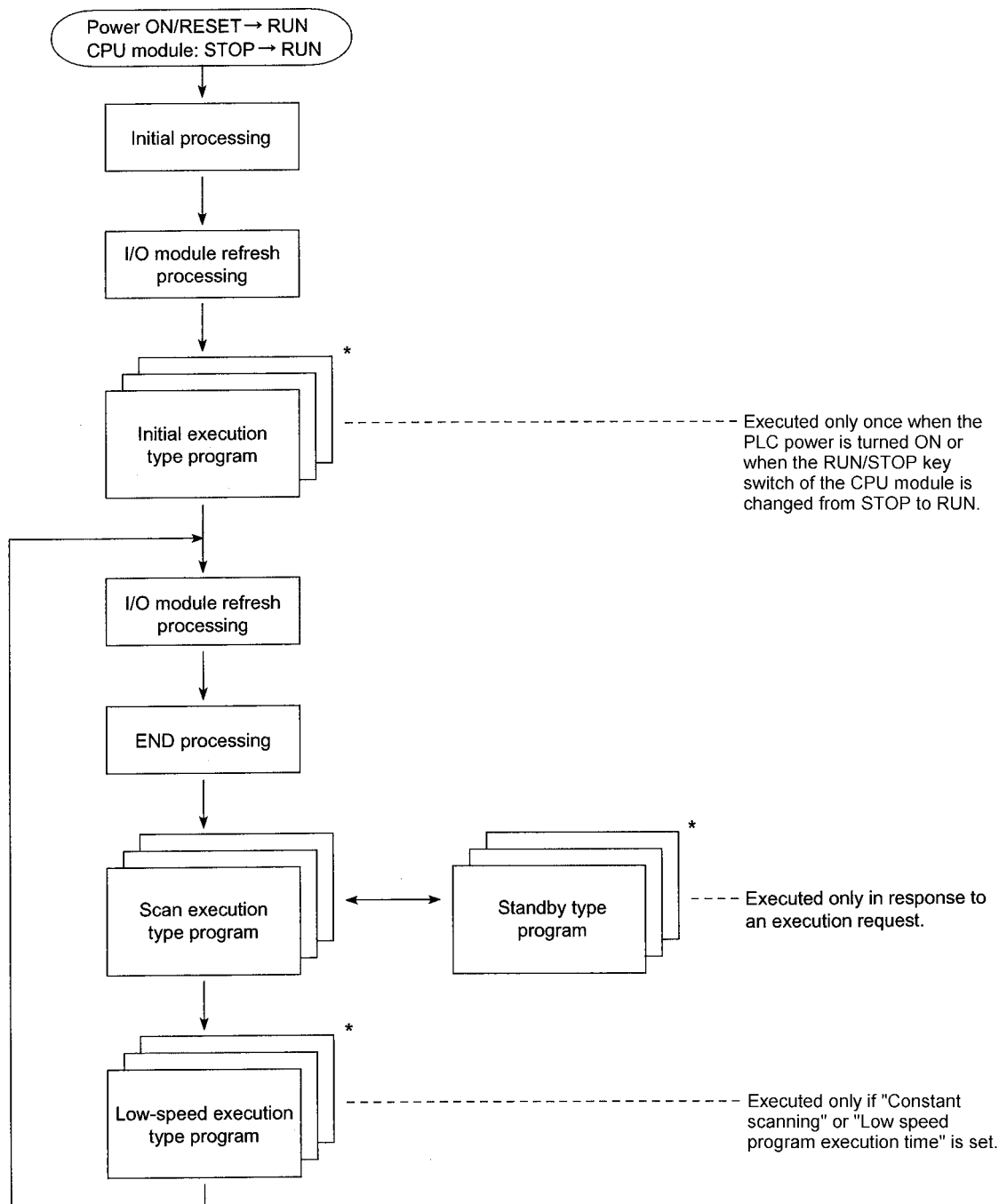
The QnACPU executes each execution type program in order of setting.

There are four executions types: "Initial execution type", "Scan execution type", "Low-speed execution type", and "Standby type".

- Initial execution type : Program executed only once when a PLC is powered ON, when a CPU module is reset, or when the RUN/STOP key switch of the CPU module is switched from STOP to RUN. (Refer to Section 12.1.1)
- Scan execution type : Program that is executed once per scan, starting from the next scan after execution of the initial execution type program. (Refer to Section 12.1.2)

- Low-speed execution type : Program that is executed only in the surplus scan time after execution of a scan execution type program in the constant scan setting, or only when the low-speed type program execution time is set.
(Refer to Section 12.1.3)
- Standby type : Program that is only executed when an execution request is made for it.
(Refer to Section 12.1.4)

The following shows the flow of operation processing when a PLC is powered ON, when a CPU module is reset, or when the RUN/STOP key switch of a CPU module is switched from STOP to RUN.



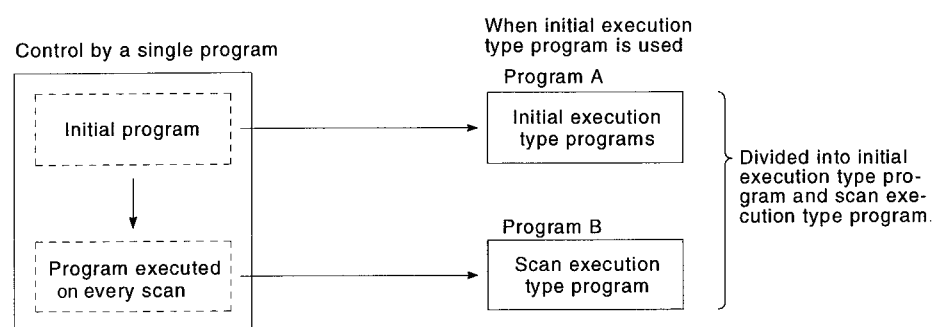
POINT

For the QnACPU, all execution types need not be set. Use initial execution type, low-speed execution type, and standby type programs marked with asterisks if required.

12.1.1 Initial execution type programs

(1) Definition

- (a) The initial execution type program is a program executed only once when a PLC is powered ON, when a CPU module is reset, or when the RUN/STOP key switch of the CPU module is switched from STOP to RUN.
- (b) The execution type is set to "Init" in program setting in the parameter mode of GPP function.
- (c) Initial execution type programs can be used for applications such as the initial processing for a special function module, where once the program has been executed, it need not be executed from the next scan.*

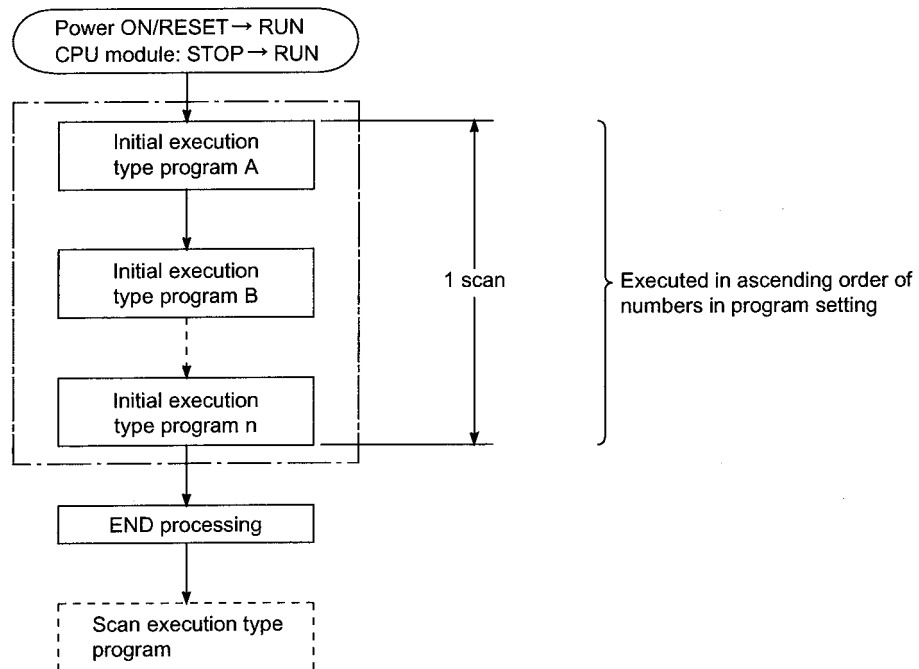


(2) Execution of multiple initial execution type programs

If there are more than one initial execution type program, they are executed in ascending order of the program numbers set in the parameter mode.

(3) END processing

When execution of all initial execution type programs is completed, END processing is performed and a scan execution type program is executed from the next scan.



POINT

- * Instructions that contain a completion device cannot be used in initial execution type programs.

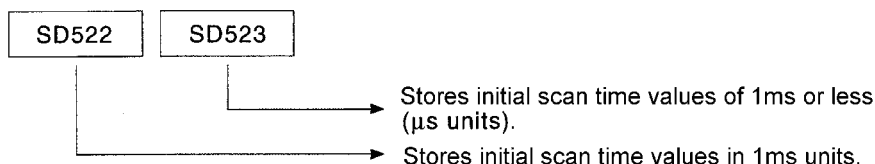
(4) Initial scan time

- (a) This is the execution time of an initial execution type program.

If multiple initial execution type programs are to be executed, it is the time required to complete execution of all these programs.

- (b) The QnACPU measures the initial scan time and stores it in special registers SD522 and SD523.*1

The initial scan time can be checked by monitoring SD522 and SD523.



Example:

If "3" and "400" are stored in SD522 and SD523 respectively, the initial scan time is 3.4ms.

*1 The accuracy of each scan time stored in the special registers is ± 0.1 ms. Note that, even if a watchdog timer (WDT) reset instruction is executed in the sequence program, measurement of the initial scan time is continued.

(5) Initial execution monitoring time

This is a timer for monitoring the execution time of initial execution type programs; no default value is set.

To monitor the execution time of an initial execution type program, a value can be set within the range of 10ms to 2000ms in "PLC RAS" in the parameter mode. (Unit: 10 ms)

If the initial scan time exceeds the set initial execution monitoring time, a "WDT ERROR" occurs and the QnACPU stops its operation.

POINT	
	An error may be generated in the range of 0 to 10ms in measurement of the initial execution monitoring time. Because of this, if the initial execution monitoring time (t) is set as 10ms, a WDT ERROR will occur when the initial scan time exceeds the limit within the range of $10\text{ms} \leq t < 20\text{ms}$.

12.1.2 Scan execution type program

(1) Definition

- (a) The scan execution type program is a program that is executed once for every scan, starting from the next scan after execution of the initial execution type program.
- (b) The execution type is set to "Scan" in program setting in the parameter mode of GPP function.

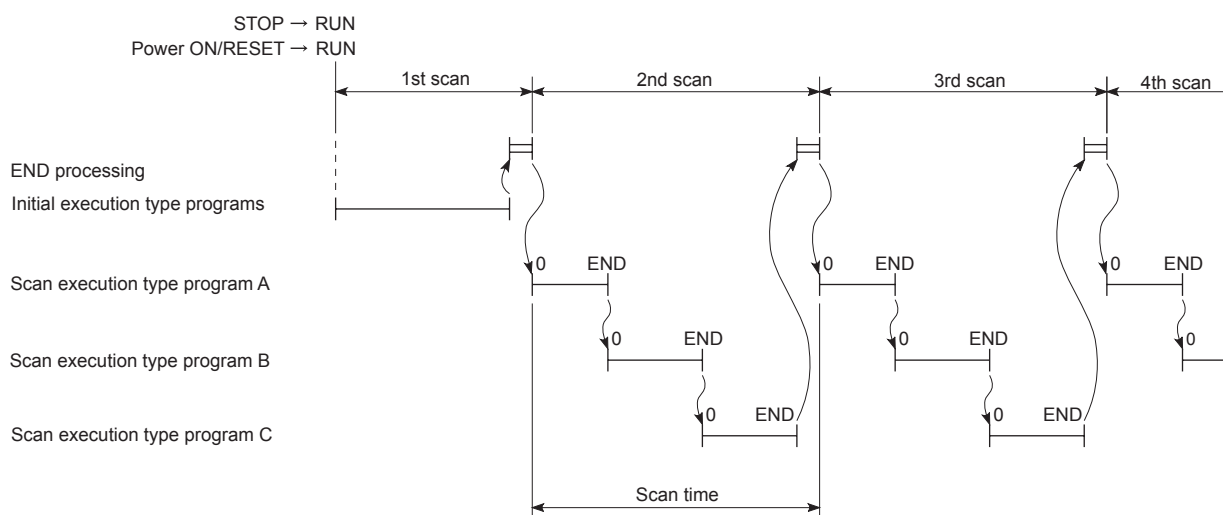
(2) Execution of multiple scan execution type programs

If there are more than one scan execution type program, they are executed in ascending order of the program numbers set in the parameter mode.

(3) END processing

When all the scan execution type programs have been executed, END processing is performed and then the first scan execution type program is executed again.

By inserting a COM instruction at the end of a scan execution type program, END processing (general data processing, link refresh) can be executed for each program.

(4) When constant scan time is set^{*1}

When constant scan is set, the scan execution type program is executed once for every preset constant scan time.

REMARK

- ^{*1} Constant scan is a function whereby a scan execution type program is repeatedly executed at fixed intervals.
See Section 10.2.

POINT

- (1) For the index register processing in the case where an interrupt program is executed during execution of a scan execution type program, refer to the QnACPU Programming Manual (Fundamentals).

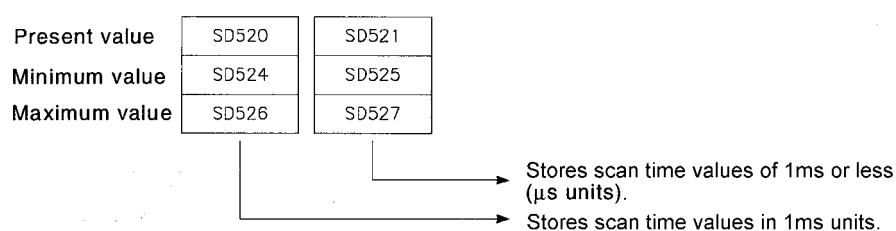
(5) Scan time

- The scan time is a total of the scan execution type program execution time, the END processing time, and either the low-speed program execution time or the constant scan waiting time.*1

When more than one scan execution type program is executed, "the execution time of the scan execution type program" is the time required for completing execution of all these programs.

*1 Refer to Section 12.1.3.

- The QnACPU measures the present, minimum, and maximum values for the scan time and stores them in special registers SD520, SD521, and SD524 to SD527.*2 The scan time can be checked by monitoring these special registers.



Example: If "3" and "400" are stored in SD520 and SD521 respectively, the scan time is 3.4ms.

*2 The accuracy of each scan time stored in the special registers is ± 0.1 ms. Note that, even if the watchdog timer (WDT) reset instruction is executed in the sequence program, measurement of each scan time is continued.

(6) WDT (watchdog timer)

This is a timer that monitors the scan time; and 200ms is set as a default value. WDT is set within the range of 10ms to 2000ms in "PLC RAS" in the parameter mode. (Unit: 10ms).

When using a low-speed execution type program(s), make sure that the specified WDT value is greater than the sum of the scan time and the low-speed execution type program execution time.

If the scan time (total of execution times for scan execution type programs and low-speed execution type programs, END processing time, and low-speed END processing time) exceeds the time set for WDT, a "WDT ERROR" occurs and the QnACPU stops its operation.

POINT	
	The WDT measurement error is 0 to 10ms. Because of this, when WDT (t) is set to 10ms, a WDT ERROR may not occur even if the scan time exceeds the limit within the range of $10\text{ms} \leq t < 20\text{ms}$.

12.1.3 Low-speed execution type program

(1) Definition

- (a) The low-speed execution type program is a program that is executed only in the surplus time of constant scan operation or in the preset low-speed execution program execution time.
- When using a fixed scan time to give priority to control accuracy, set the constant scan time in "PLC RAS" in the GPP function's parameter mode.
(Setting range: 5 to 2000ms; Unit: 5ms)
 - To ensure the execution time for low-speed execution type programs in each scan and to make these programs operate properly, set the low-speed program execution time in "PLC RAS" in the parameter mode.
(Setting range: 1 to 2000ms; Unit: 1ms)
 - In order to execute low-speed execution type programs, either the constant scan time or the low-speed program execution time must be set.
- (b) Set "Slow" as the execution type in program setting in the parameter mode.
- (c) This execution type is used for programs that do not have to be executed every scan, such as a program for printer output.

(2) Execution of multiple low-speed execution type programs

If there are more than one low-speed execution type program, they are executed in ascending order of the program numbers set in the parameter mode.

- (3) Execution time for low-speed execution type program executed in one scan
- (a) When operation of all low-speed execution type programs is completed within one scan and there is surplus time, the subsequent processing varies depending on the setting status of special relay SM330 and the execution condition for the low-speed execution type programs.
- Non-synchronization method (SM330 = OFF) : Operation of a low-speed execution type program is continuously executed within surplus time.
 - Synchronization method (SM330 = ON) : Even if there is surplus time, operation of a low-speed execution type program is not executed and another operation starts from the next scan.

Operation method of low-speed execution type program	Setting status of SM330	Execution condition of low-speed execution type program	
		Constant scan setting	Low-speed program execution time setting
Non-synchronization method	OFF	Re-executes low-speed execution type program.*1	Re-executes low-speed execution type program.*2
Synchronization method	ON	Constant scan wait time occurred*3	Starts scan execution type program operation.*4

*1 When the constant scan time is set, the low-speed execution type program is repeatedly executed for the surplus time of the constant scan.
Accordingly, the execution time of the low-speed execution type program is different at each scan. If surplus time in constant scan is less than 2ms, the low-speed execution type program is not executable.

When using a low-speed execution type program, set a proper constant scan time so that surplus time will be 2ms or longer.

*2 When the low-speed program execution time is set, a low-speed execution type program is repeatedly executed for the set time duration.
Accordingly, the scan time is different at each scan.

*3 When the constant scan time is set, surplus time after completion of the low-speed END processing is used as wait time. When the set constant scan time is reached, the scan execution type program is executed.

Wait time for constant scan

$$= (\text{Set constant scan time}) - (\text{Scan time}) - (\text{Low-speed scan time})$$

Therefore, the scan time for each scan is constant.

If surplus time in constant scan is less than 2ms, the low-speed execution type program is not executable. When using a low-speed execution type program, set a proper constant scan time so that surplus time will be 2ms or longer.

*4 When the low-speed program execution time is set, operation of the scan execution type program is started ignoring the surplus time after completion of the low-speed END processing.

Surplus time in low-speed program execution time

$$= (\text{Set low-speed program execution time}) - (\text{Low-speed scan time})$$

Accordingly, the scan time is different at each scan.

- (b) If the low-speed execution type program is not processed within surplus time of the constant scan time or within the low-speed program execution time, the program execution is interrupted and is resumed in the next scan.

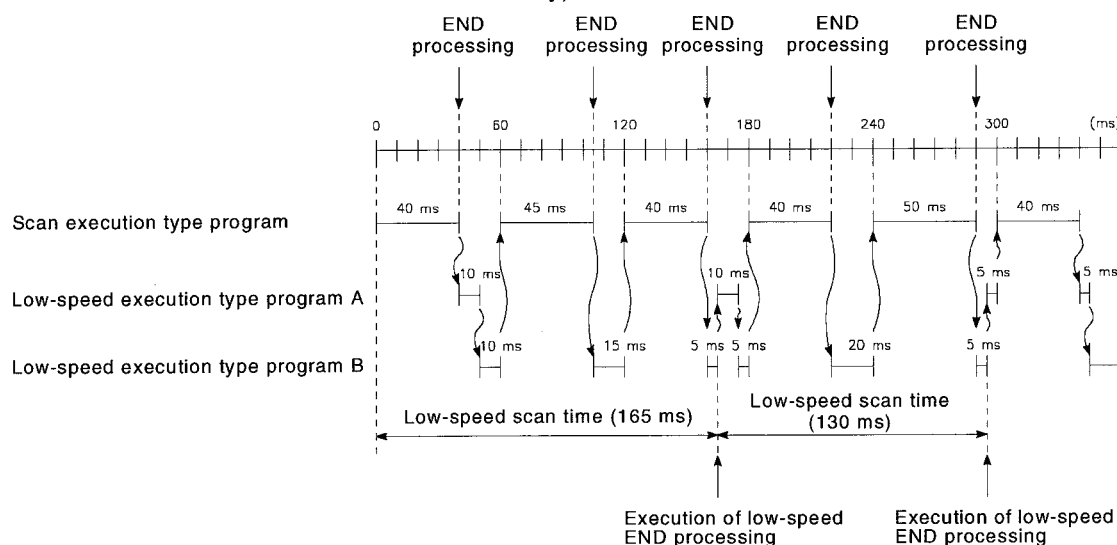
POINT	
(1)	For the index register processing in the case where a scan execution type program is switched to a low-speed execution type program, refer to the QnACPU Programming Manual (Fundamentals).
(2)	For the index register processing in the case where an interrupt program is executed during execution of a low-speed execution type program, refer to the QnACPU Programming Manual (Fundamentals).
(3)	Set a proper low-speed program execution time so that the value obtained by adding it to the scan time is smaller than the set WDT value.
(4)	The COM instruction cannot be used in the low-speed program.
(5)	When "Constant scan time" and "Low-speed program execution time" are set, PRG. TIME OVER (Error code: 5010) occurs in the case of (Surplus time of constant scan) < (Low-speed program execution time) Execute the low-speed execution type program either in the constant scan time or in low-speed program execution time.

1: For non-synchronous method:

(1) When "Constant scanning" is set

The operation when a low-speed execution program is executed under the following conditions is shown below.

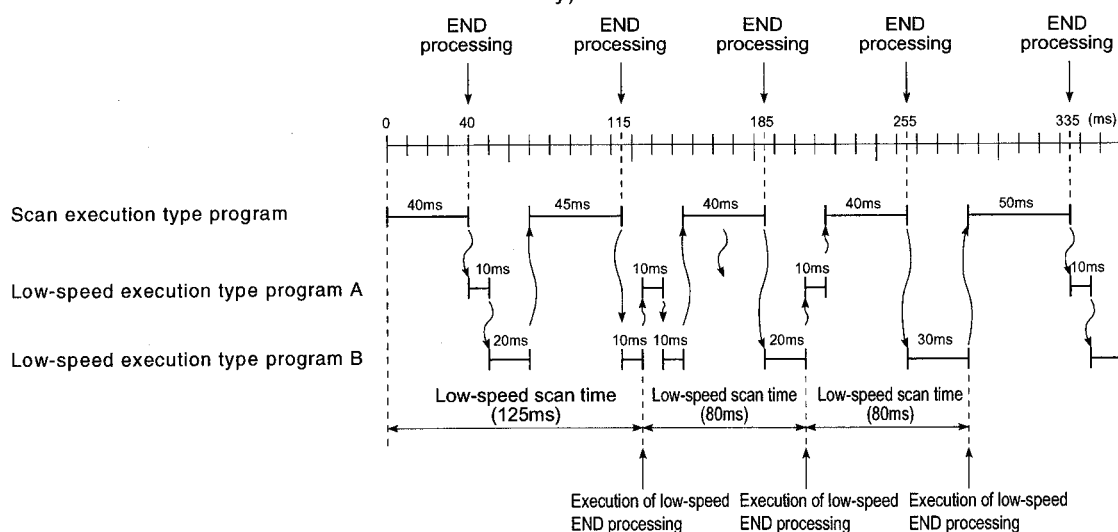
- Constant scan time: 60 ms
- Total for scan execution type programs: 40 ms to 50 ms
- Execution time for low-speed execution type program A: 10 ms
- Execution time for low-speed execution type program B: 30 ms
- END processing: 0 ms (assuming 0 ms here to make the explanation easy)
- Low-speed END processing: 0 ms (assuming 0 ms here to make the explanation easy)



(2) When a low-speed program execution time is set

The operation when a low-speed execution program is executed under the following conditions is shown below.

- Low-speed program execution time: 30 ms
- Total for scan execution type programs: 40 ms to 50 ms
- Execution time for low-speed execution type program A: 10 ms
- Execution time for low-speed execution type program B: 30 ms
- END processing: 0 ms (assuming 0 ms here to make the explanation easy)
- Low-speed END processing: 0 ms (assuming 0 ms here to make the explanation easy)

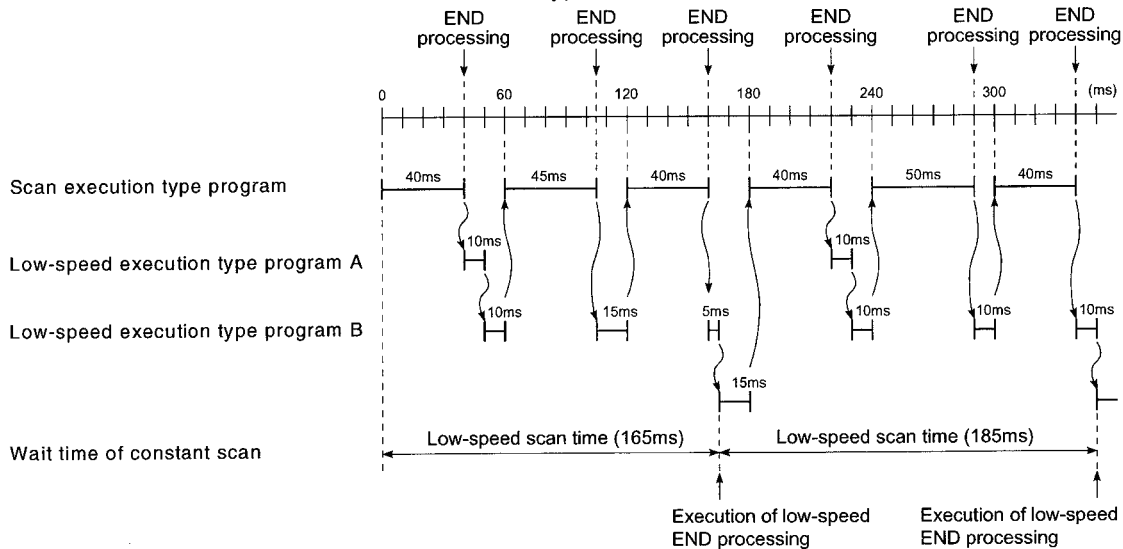


2: For synchronous method:

(1) When "Constant scanning" is set

The operation when a low-speed execution program is executed under the following conditions is shown below.

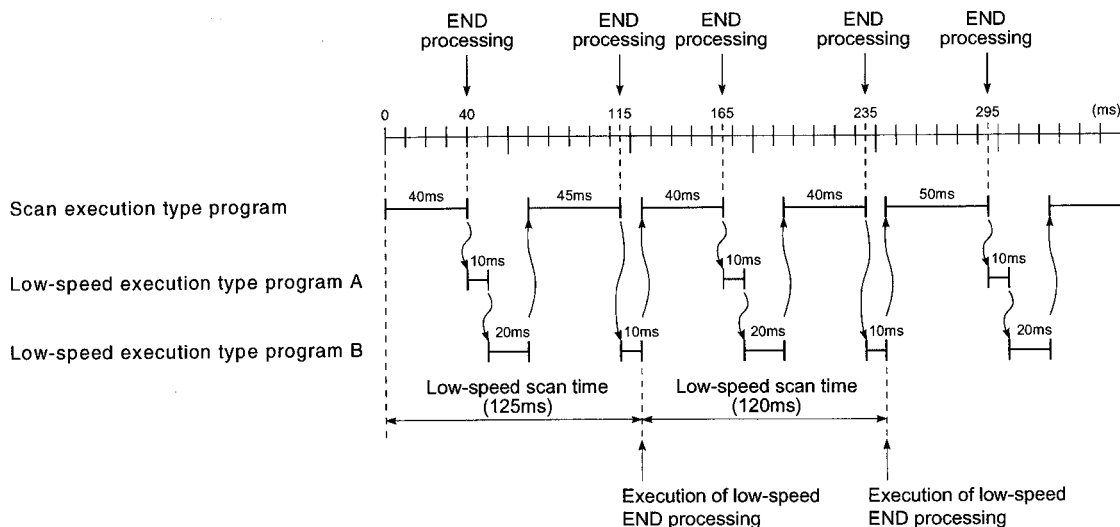
- Constant scan time: 60 ms
- Total for scan execution type programs: 40 ms to 50 ms
- Execution time for low-speed execution type program A: 10 ms
- Execution time for low-speed execution type program B: 30 ms
- END processing: 0 ms (assuming 0 ms here to make the explanation easy)
- Low-speed END processing: 0 ms (assuming 0 ms here to make the explanation easy)



(2) When a low-speed program execution time is set

The operation when a low-speed execution program is executed under the following conditions is shown below.

- Low-speed program execution time: 30 ms
- Total for scan execution type programs: 40 ms to 50 ms
- Execution time for low-speed execution type program A: 10 ms
- Execution time for low-speed execution type program B: 30 ms
- END processing: 0 ms (assuming 0 ms here to make the explanation easy)
- Low-speed END processing: 0 ms (assuming 0 ms here to make the explanation easy)



(6) Low-speed execution monitoring time

This is a timer for monitoring the execution time of low-speed execution type programs; no default value is set.

To monitor the execution time of an low-speed execution type program, a value can be set within the range of 10ms to 2000ms in "PLC RAS" in the parameter mode. (Setting units: 10ms).

If the low-speed scan time exceeds the set low-speed execution monitoring time, a "PRG TIME OVER" error occurs. The QnACPU however continues its operation.

POINT	
	The low-speed execution monitoring time is measured in low-speed END processing. Because of this, when the low-speed execution monitoring time (t) is set to 100ms, a "PRG TIME OVER" error occurs if the low-speed scan time measured in low-speed END processing exceeds 100ms.

12.1.4 Standby type program

(1) Definition

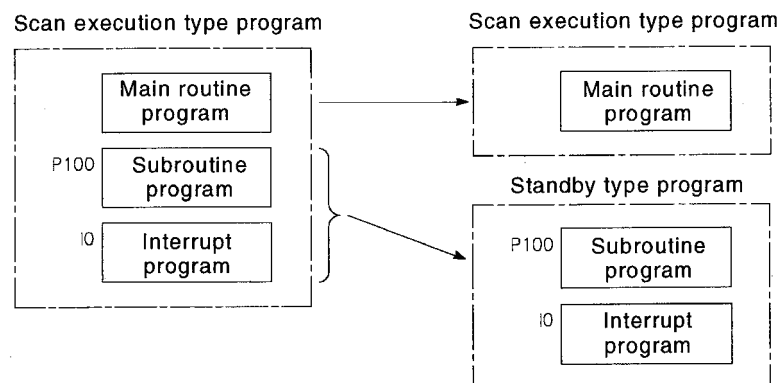
- (a) The standby type program is a program that is executed only in response to an execution request.
- (b) The standby type program has the following applications:
 - 1) Program library
Subroutine programs and interrupt programs are set as standby type programs and controlled separately from the main program.
 - 2) Set-up of programs
The main routine program is registered to the standby type program and programs required for control are changed to the scan execution type programs. Programs not used for control are changed to the standby type programs.

(2) Program library

(a) Library creation of program

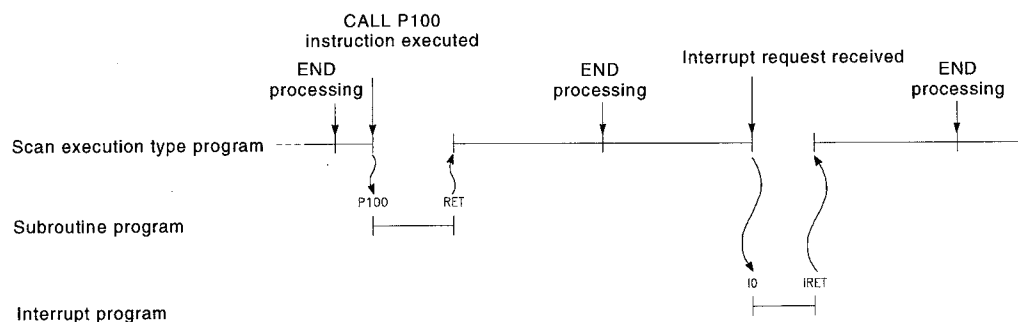
- 1) Program library is used to control subroutine programs and interrupt programs separately from the main routine program.

It is possible to create multiple subroutine programs and interrupt programs as one standby type program.



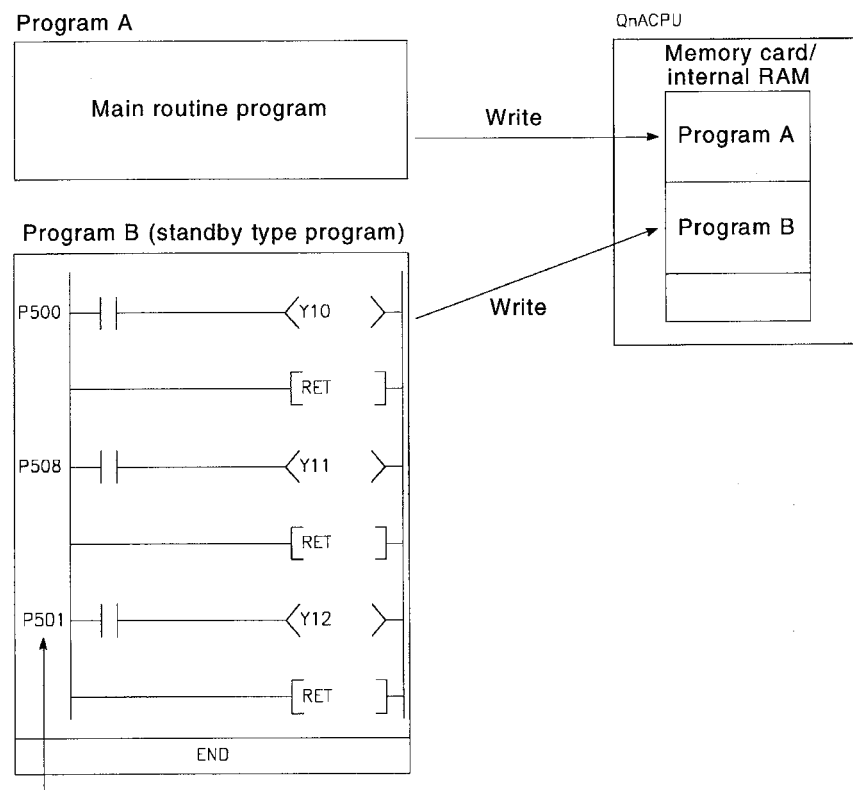
- 2) When a standby type program execution is completed, control returns to the program that was being executed before execution of the standby type program.

The following shows the operation performed when a subroutine program and an interrupt program in a standby type program are executed.



POINT
(1) Timers are not to be used in standby type programs because they update present values and turn ON/OFF the contacts when the OUT T□ instruction is executed. (2) When setting a subroutine program as a standby type program, use a common pointer. Standby type programs that use local pointers are not executable. For details on common and local pointers, refer to the QnACPU Programming Manual (Fundamentals).

- (b) When grouping several subroutine programs into one
- 1) Create subroutine programs in order starting from step 0 in the standby type program.
An END instruction is required at the end of the subroutine programs.
 - 2) Since there are no restrictions on the order of creation of subroutine programs, there is no need to arrange pointers in ascending order of pointer numbers when creating multiple subroutine programs.
 - 3) Use common pointers.*
Subroutine programs using common pointers can be called from all the programs that are being executed by the QnACPU.

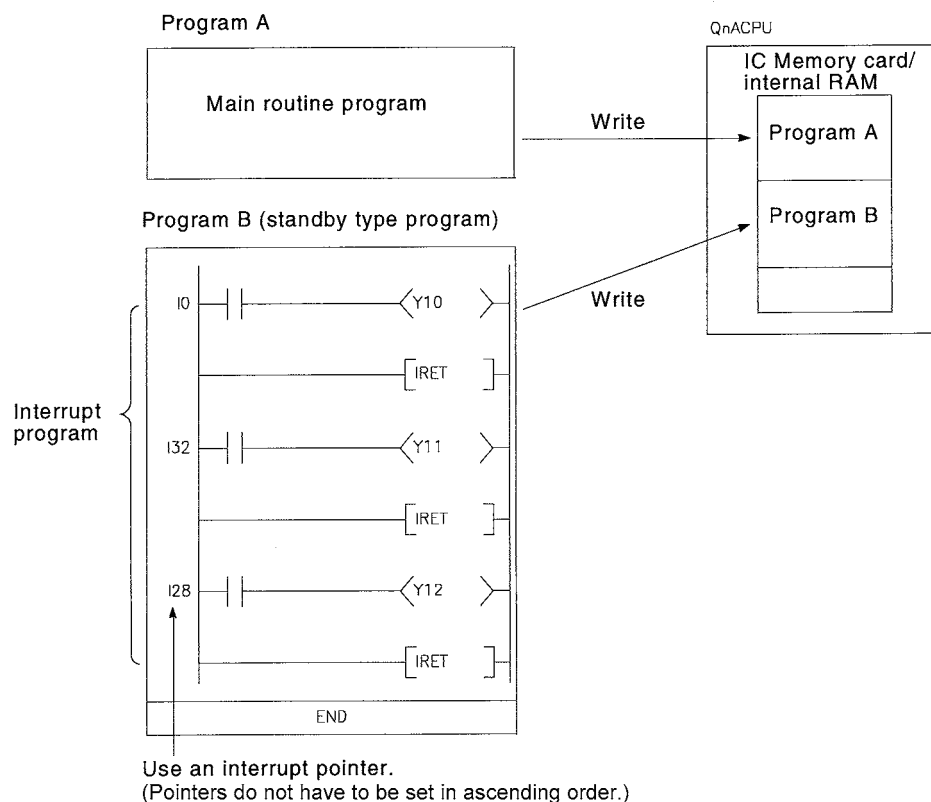


Use a common pointer.*
(Pointers do not have to be set in ascending order.)

REMARK

* For details on common pointers, refer to the QnACPU Programming Manual (Fundamentals).

- (c) When grouping several interrupt programs into one
- 1) Create interrupt programs in order starting from step 0 in the standby type program.
An END instruction is required at the end of the interrupt programs.
 - 2) Since there are no restrictions on the order of creation of interrupt programs, there is no need to arrange pointers in ascending order of pointer numbers when creating multiple interrupt programs.

**REMARK**

For details on interrupt pointers, refer to the QnACPU Programming Manual (Fundamentals).

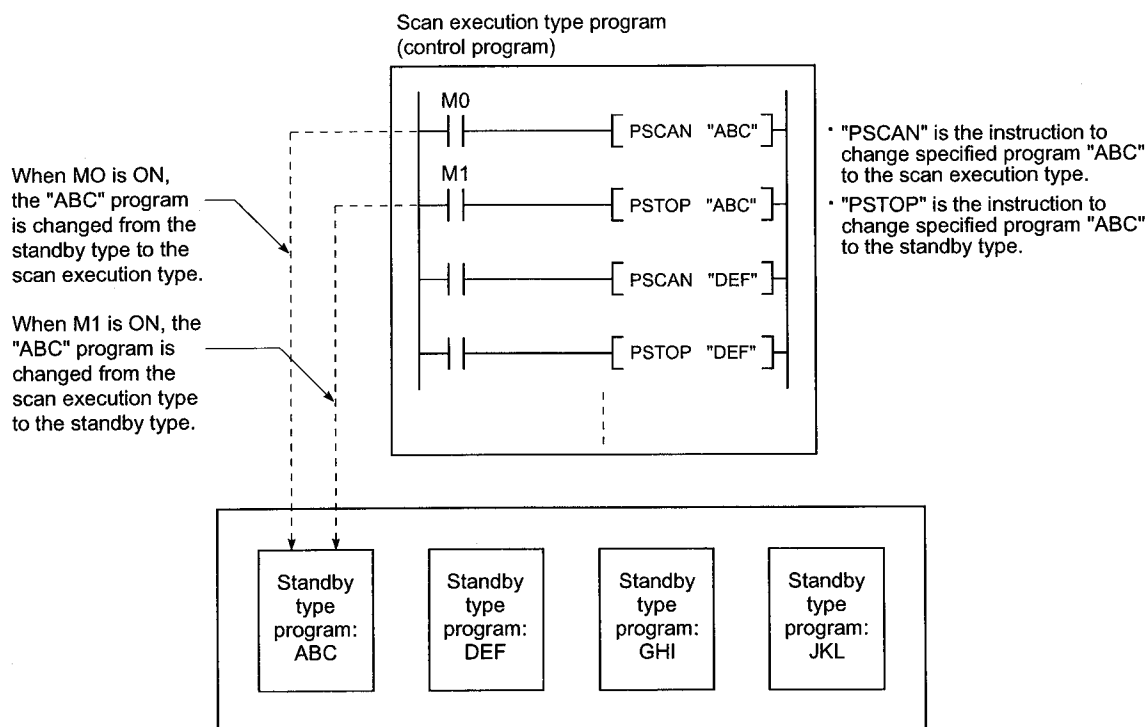
(3) Set-up of programs

- (a) Programs corresponding to all of the systems can be created in advance, and thereby necessary programs only can be executed.

Programs set as the standby type with parameters can be changed to the scan type programs in the sequence program for execution.

Use the following instructions to change the execution type in the QnACPU:

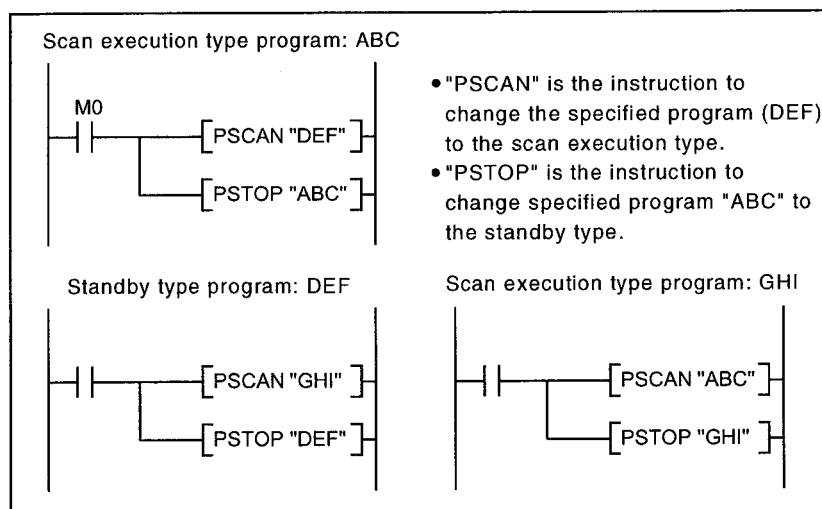
- 1) PSCAN instruction : Changes the program type from the standby type to the scan execution type.
 - 2) PLOW instruction : Changes the program type from the standby type to the low-speed execution type.
 - 3) PSTOP instruction : Changes the program type from the scan execution/low-speed execution type to the standby type.
- (b) The following methods are available to switch programs for execution:
- 1) When selecting programs to be executed in a control program:
 - Defining the scan execution type program as the control program, the QnACPU switches between the standby type program and the scan execution type program according to the set conditions to control the program to be executed.
 - The following shows how the execution types of standby programs, "ABC," "DEF," "GHI" and "JKL" are changed in the control program.



2) When changing the execution type of another program from the scan execution type program:

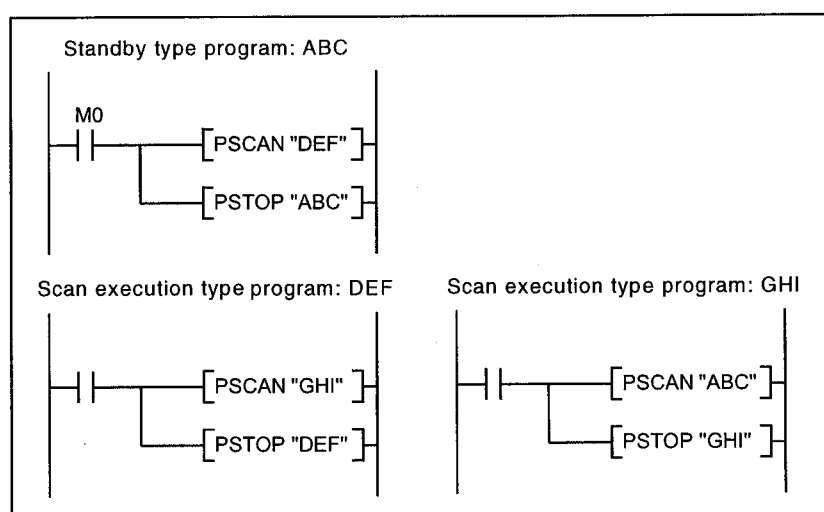
- In the scan execution type program in execution, the type of the program to be executed next is changed from the standby type to the scan execution type.
- The following shows the operation that the QnACPU switches the standby type program "DEF" to the scan execution type, and the scan execution program "ABC" to the standby type program when M0 in program "ABC" turns on.

[Before execution of PSCAN and PSTOP instructions]



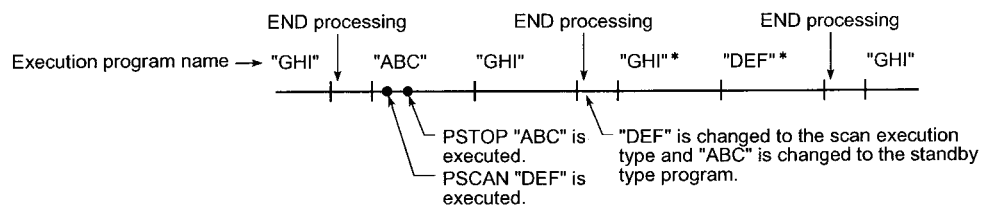
↓ When M0 is ON

[After execution of PSCAN and PSTOP instructions]



- (c) The program execution type is changed by the PSCAN or PSTOP instruction in the END processing.

Therefore, it is not changed during program execution.

**REMARK**

* The "GHI" and "DEF" programs are executed in the sequence set with parameters in the program setting.

12.1.5 Initial processing

Initial processing is the pre-processing for executing sequence operations.

The QnACPU executes it only once in the case of the CPU module status described in the following table.

Once the initial processing is completed, the CPU module is placed into the operation status set by the RUN/STOP switch.

Item	Status of the CPU module		
	At Power ON	At RESET	STOP → RUN Status*1
Initialization of I/O module	○	○	×
Initialization of devices outside latched range (Bit device: OFF, Word device: 0)	○	○	×
Self-diagnostics	○	○	○
Auto allocation of module I/O No.	○	○	○
Setting MELSECNET/10 network info and MELSECNET(II)/B data link info	○	○	×
Setting CC-Link info and MELSECNET/MINI-S3 info	○	○	×
Setting initial device values	○	○	○
Bootting from memory card	○	○	×

○: Executed ×: Not executed

- *1 Indicates the case that the CPU enters RUN status without being reset after changing a parameter or program in STOP status.
(The RUN/STOP key switch is operated as follows: STOP→RUN→(RUN LED is flickering.)→STOP→RUN.)
Note that the instructions for conversion into pulse (PLS, □P) may not function properly since the previous information may not be retained depending on the program change (write during RUN in STOP status, or write to PLC).

12.1.6 Refresh processing of I/O module

Refresh processing of I/O modules is executed.

(Refer to the QnACPU Programming Manual (Fundamentals).)

12.1.7 END processing

This is a post-process to finish one cycle of operation processing of the sequence program and to return the execution of the sequence program to step 0.

- (a) Self-diagnostic checks are performed for fuse blown, module verify, or low battery. (Refer to Section 9.3)
- (b) When data read/write is requested from a peripheral device or an intelligent special function module (computer link module, serial communication module, Ethernet module, etc.), data are exchanged between the PLC CPU and the peripheral device or intelligent special function module.
- (c) Refresh processing is performed when a refresh request is issued from a network module or a link module.
- (d) When the trace point for sampling trace is set to each scan (after execution of END instruction), the status of the set device is stored into the sampling trace area.
- (e) Refresh processing based on the MELSECNET/MINI-S3 automatic refresh function is performed. (Refer to Chapter 7))

POINT	
(1)	If the constant scan function (see Section 10.2) is set, the END processing time result is retained during the period between completion of END processing and start of the next scan.
(2)	If a low-speed execution type program (see Section 12.1.3) is executed, low-speed END processing is performed separately from normal END processing. In low-speed END processing, the special relays and special registers for low-speed execution programs are set.

12.2 Operation Processing of RUN, STOP, PAUSE, and STEP-RUN

The QnACPU has four kinds of operation statuses: RUN, STOP, PAUSE, and step operation (STEP-RUN) statuses.

Operation processing of PLC CPU in each operation status is explained here.

- (1) RUN status operation processing
 - (a) The RUN status represents a status in which sequence program operation is repeated in the order from step 0 → END (FEND) instruction → step 0.
 - (b) When entering the RUN status, the CPU outputs the output status data saved in STOP status according to the output mode setting parameter for STOP → RUN.
 - (c) Processing time from switching STOP → RUN to the start of the sequence program operation is usually one to three seconds, although it may vary depending on the system configuration.
Note that it may be longer than this depending on the conditions.
- (2) STOP status operation processing
 - (a) The STOP status is a status in which sequence program operation is stopped by the RUN/STOP key switch or due to remote STOP (see Section 10.6.1).
 - (b) When entering the STOP status, the CPU saves the output status data and turns all output points to OFF. Data memories except for output (Y) are retained.
- (3) PAUSE status operation processing
 - (a) The PAUSE status represents a status in which operation of sequence program is suspended with the output and data memory statuses retained. (Refer to Section 10.6.3)
- (4) Step operation (STEP-RUN) operation processing
 - (a) STEP operation is an operation mode in which operation processing of a sequence program can be paused/continued by each instruction using GPP function. (Refer to Section 8.7)
 - (b) Since an operation processing is paused while retaining the output and data memories, the execution condition can be confirmed.

(5) Operation processing of QnACPU when RUN/STOP key switch is operated

RUN/STOP state	QnACPU Operation Processing				
	Operation processing of sequence program	External output	Data memory		Remark
			M, L, S, T, C, D	Y	
RUN→STOP	Executes up to the END instruction, then stops.	OS saves the output status, and sets all the output points to OFF.	Retains the condition immediately before entering the STOP status.	OS saves the output status, and sets all the output points to OFF.	
STOP→RUN	Starts from step 0.	Depends on the output mode set by the parameter for STOP→RUN.	Starts operations from the condition immediately before entering the STOP status.	Depends on the output mode set by the parameter for STOP→RUN.	

POINT
The QnACPU executes the following processing in any of RUN state, STOP state, or PAUSE status. • Refresh processing of I/O modules • Data communication with peripheral devices, computer link modules, and/or serial communication modules. • Link refresh processing. Thus, even in the STOP state or PAUSE state, I/O monitoring and test operations using a peripheral device, reading/writing from computer link modules or serial communication modules, and communication with other stations via MELSECNET can be performed.

12.3 Operation Processing for Instantaneous Power Failure

The QnACPU detects a momentary power failure when the input power voltage supplied to the power supply module becomes lower than the specified range.

When the QnACPU detects an instantaneous power failure, the following operation processing is performed.

- (1) When an instantaneous power failure shorter than the allowable momentary power failure period occurred:
 - (a) When an instantaneous power failure occurs, the output statuses are held and the operation processing is suspended after the name of the currently accessing file and error history have been stored.
(The timer count continues.)
 - (b) If there is an SFC continuous operation designation, system save processing is executed.
 - (c) When power is restored, the operation processing will be continued.
 - (d) While the operation is interrupted due to an instantaneous power failure, measurement of the watchdog timer (WDT) continues. For example, if 200ms is set for the WDT parameter setting, power failure of 15ms in the scan time of 190ms will cause a watchdog timer error.

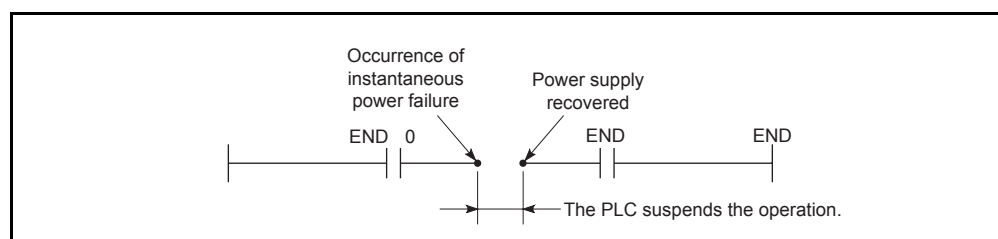


Fig. 12.1 Operation Processing for Instantaneous Power Failure

- (2) When power failure longer than the allowable momentary power failure period occurred:
The QnACPU starts from the first.
The operation processing is the same as that performed at PLC power-up or at CPU module reset by the RUN/STOP key switch.

12.4 Data Clear Processing

The QnACPU clears data other than the following by turning the RUN/STOP key switch to RESET or by resetting the PLC power (ON, OFF and ON):

- (a) Data in the built-in RAM (except data specified for memory clear in the boot specification)^{*1}
- (b) Data in the memory card
- (c) Data of latch-specified devices(Latch clear key enabled)
- (d) Data of latch-specified devices(Latch clear key disabled)
- (e) File register data
- (f) Local device data
- (g) Fault history data

^{*1} For the boot specification, refer to the QnACPU Programming Manual (Fundamentals).

Data given in (c) and (g) are cleared by latch clear operation using the RUN/STOP key switch (Refer to Section 15.3.) or by remote latch clear operation from GPP function (Refer to Section 10.6.5.)

The latch range is specified for each device on the "Device" screen in the parameter mode of GPP function. There are the following two latch range setting options.

- 1) Latch clear key enabled : Used to set a latch range which can be cleared by the latch clear operation using the RUN/STOP key switch.
- 2) Latch clear key disabled: Used to set a latch range which cannot be cleared by the latch clear operation using the RUN/STOP key switch.

Devices for which the latch clear key is disabled can be cleared by an instruction or by the clear operation of GPP function.

{	1) Clearing by an instruction : Reset by RST instruction , or transfer K0 with MOV instruction . 2) Clearing by GPP function : Execute device memory all clear from the PLC menu in the online mode.	}

For details on device latch ranges, refer to the QnACPU Programming Manual (Fundamentals).

For details on the operation method of GPP function, refer to the GX Developer Operating Manual or Type SW□IVD-GPPQ Software Package Operating Manual (Online)/(Offline).

POINT	
	To clear file registers or local devices, reset them with the RST instruction or transfer KO with the MOV instruction.

MEMO

[illegible]

13 PARAMETER LIST

The parameters set for the QnACPU are listed in the table below.

For details on each parameter, refer to the section or reference manual indicated.

Item		Parameter No.	Description	
PLC name		—	Set labels and/or comments for peripheral devices on the CPU module. This setting does not affect CPU module operation.	
	Label	0000H	Set a label for the CPU module.	
	Comment	0001H	Set a comment for the CPU module.	
PLC system		—	Make various settings that are required for the CPU module system.	
Timer limit setting	Low-speed timer	1000H	Set the low-speed or high-speed timer limit.	
	High-speed timer			
RUN-PAUSE contacts		1000H	Set the contact to control RUN/PAUSE of the CPU module.	
Remote reset		1002H	Enable or disable the remote reset operation.	
Output at STOP→RUN		1003H	Set the output mode for switching from STOP to RUN.	
Common pointer No.		1005H	Set the first common pointer number.	
General data processing		1006H	Set the number of modules that are processed in one general data processing.	
Points occupied by empty slot		1007H	Set the number of points occupied by empty slots.	
System interrupt	Interrupt counter	1008H	Set the first interrupt counter number, and the fixed scan interval for the interrupt pointer.	
	Fixed scan interval			
PLC file		—	Set various kinds of files used by the CPU module.	
File register		1100H	Set a file register file to be used.	
Comment file used in a command		1101H	Set a comment file used in an instruction.	
Initial device value		1102H	Set a file for initial device values to be used.	
File for local device		1103H	Set a file for local devices to be used.	

13. PARAMETER LIST

MELSEC-QnA

	Setting		Reference Section/Reference Manual
	Default value	Setting range	
	–	–	Section 11.2
	No setting	Up to 10 characters	
	No setting	Up to 64 characters	
	–	–	–
	100ms	10ms to 1000ms (in 10ms units)	QnACPU Programming Manual (Fundamentals)
	10ms	1ms to 100ms (in 1ms units)	
	No setting	X0 to X1FFF	Section 10.6.1, Section 10.6.3
	Disabled	Enabled/disabled	Section 10.6.4
	Before operation	Before operation/After 1 scan	Section 10.4
	No setting	P0 to P4095	QnACPU Programming Manual (Fundamentals)
	1 module	1 to 6 modules	Section 6.3
	16 points	0 point to 64 points (in 16-point units)	Section 5.3
	No setting	C0 to C65535	QnACPU Programming Manual (Fundamentals)
	I28→100ms I29→40ms I30→20ms I31→10ms	5ms to 1000ms (in 5ms units)	
	–	–	–
	Not used	• Not used • Use the same file name as the program. • Use the following file.	QnACPU Programming Manual (Fundamentals)
	Not used	• Not used • Use the same file name as the program. • Use the following file.	Section 11.5
	Use the same file name as the program.	• Not used • Use the same file name as the program. • Use the following file.	QnACPU Programming Manual (Fundamentals)
	Not used	• Not used • Use the following file.	QnACPU Programming Manual (Fundamentals)

13. PARAMETER LIST

MELSEC-QnA

Item		Parameter No.	Description	
Device		—	Set the number of points, latch range, etc., for each device.	
Device points		2000H	Set the number of device points used.	
Latch (1) start (Enable C/L key)		2001H	Set the latch range for which latch clear key operation is enabled.	
Latch (2) start (Disable C/L key)		2002H	Set the latch range for which latch clear key operation is disabled.	
Local device		2003H	Set the range of devices to be set as local devices.	
PLC RAS		—	Set various kinds of settings for the RAS function.	
WDT setup	WDT setting	3000H	Set the watchdog timer for the CPU module.	
	Initial execution monitoring time			
	Low speed execution monitoring time			
Error check		3001H	Set whether to detect the specified errors or not.	
Operating mode when there is an error		3002H	Set the operation mode in which the CPU module enters when an error is detected.	
Constant scan		3003H	Set the constant scan time.	
Annunciator display mode	Display F No.	3004H	Set the display mode that is activated when an annunciator comes ON.	
	Comment display			
	Time of occurrence			
Breakdown history		3005H	Set where the CPU module breakdown history is stored.	
Low speed program execution time		3006H	Set the time required for execution of low-speed execution type programs.	

13. PARAMETER LIST

MELSEC-QnA

	Setting		Reference Section/Reference Manual
	Default value	Setting range	
	—	—	—
	X→ 8k points Y→ 8k points M→ 8k points L→ 8k points B→ 8k points F→ 2k points SB→ 2k points V→ 2k points S→ 8k points T→ 2k points ST→ 0k point C→ 1k point D→ 12k points W→ 8k points SW→ 2k points	Fixed to X (8k points), Y (8k points), S (8k points), SB (2k points), SW (2k points). Up to 32k points per device within a range of 28.8k words, including the above points However, the total for bit devices is 64k points.	QnACPU Programming Manual (Fundamentals)
	No setting	1 range only for each device	Section 10.3
	No setting	1 range only for each device	Section 10.3
	No setting	1 range only for each device	QnACPU Programming Manual (Fundamentals)
	—	—	—
	200ms	10ms to 2000ms (in 10ms units)	Section 9.2
	No setting	10ms to 2000ms (in 10ms units)	Section 12.1.1
	No setting	10ms to 2000ms (in 10ms units)	Section 12.1.3
	Checked	Error checked	Section 9.3
	Stop	Stop/Continue	Section 9.3
	No setting	5ms to 2000ms (in 5ms units)	Section 10.2
	Displayed	Displayed/Not displayed	Section 9.9.2
	Not displayed	Displayed/Not displayed	
	Not displayed	Displayed/Not displayed	
	Stored in built-in RAM	Stored in built-in RAM/specified history file	Section 9.4
	No setting	1ms to 2000ms (in 1ms units)	QnACPU Programming Manual (Fundamentals)

13. PARAMETER LIST

MELSEC-QnA

Item		Parameter No.	Description	
I/O Assign		—	Set the mounting status of each module.	
Slot setting	Classification	4000H	Set the module type, number of points, head I/O No., etc.	
	Number of points			
	Start XY			
	Model Name			
Base setting	Power model name	4001H	Set model names of a power supply module and/or extension cables. This setting does not affect CPU module operation.	
	Extension cable			
MELSECNET/Ethernet setting		—	Set link parameters for the MELSECNET (II) data link system, network parameters for the MELSECNET/10 network system or Ethernet parameters.	
	Unit count	5000H		
	Valid module for access to other station	5001H		
MELSECNET (II) and MELSECNET/10 network setting	Inter-device transfer parameters	5002H		
	Routing parameter	5003H		
	Network setting	5NM0H		
	Network refresh parameter	5NM1H		
	Common parameter	5NM2H		
	Station inherent parameter	5NM3H		
	I/O assignment	5NM4H		
Ethernet network setting	Group No.	9N00H		
	IP address			

13. PARAMETER LIST

MELSEC-QnA

	Setting		Reference Section/Reference Manual
	Default value	Setting range	
	—	—	—
	No setting	Empty/Input/Output/Special	Section 5.3
	No setting	0 to 64 points (in 16-point units)	
	No setting	0 to 1FFFH (in 10H units, hexadecimal)	
	No setting	Up to 16 characters	
	No setting	Up to 16 characters	Section 5.3
	—	For QnA/Q4AR MELSECNET/10 Network System Reference Manual	For QnA/Q4AR MELSECNET/10 Network System Reference Manual MELSECNET, MELSECNET/B Data Link System Reference Manual

* N and M indicate the following:
N: Number of the module counted from the first.
M: Network type

M	Network type	M	Network type	M	Network type
0H	MELSECNET/10 (Default)	7H	MELSECNET (Local station)	DH	MELSECNET/10 (Multiple remote submaster, No remote master in the host CPU module)
1H	MELSECNET/10 (Control station)	8H	MELSECNET II mixed (Local station)		
2H	MELSECNET/10 (Normal station)	9H	MELSECNET II (Local station)	EH	MELSECNET/10 (Multiple remote submaster, There is a remote master in the host CPU module.)
3H	MELSECNET/10 (Remote master station)	AH	MELSECNET/10 (Standby station)		
4H	MELSECNET (Master station)	BH	MELSECNET/10 (Multiple remote master)	FH	MELSECNET/10 (Parallel remote submaster)
5H	MELSECNET II mixed (Master station)	CH	MELSECNET/10 (Parallel remote master)		
6H	MELSECNET II (Master station)				

13. PARAMETER LIST

MELSEC-QnA

Item		Parameter No.	Description	
MELSECNET/MINI setting		—	Make the settings for automatic refresh of the MELSECNET/MINI system.	
Number of master modules		6000H	Set the number of MELSECNET/MINI master modules to be used.	
MELSECNET/ MINI detailed settings	Master module head I/O No.	600NH*	Make the detailed setting required for automatic refresh of the MELSECNET/MINI system.	
	Model name & number of stations			
	Receive data batch refresh			
	Send data batch refresh			
	Retry count for communication errors			
	FROM/TO instruction access priority			
	Receive data clear at communication error			
	Faulty station detection bit data			
	Error No.			
	MINI link operation when CPU stopped			
	Circuit error check			
Supplementary settings		7000H	Perform various settings required when multiple programs are used.	
Program setting			Set programs to be executed among multiple programs.	
Boot file setting			Set the file for boot operation and other settings.	
SFC		—	Perform various settings required for SFC programs.	
SFC program start mode		8002H		
Start condition		8003H		
Output mode when the block is stopped		8005H		
Acknowledge XY assignment		—	Allows confirmation of the settings made in I/O assignment. This setting does not affect CPU module operation.	

* N means the number of the master module counting from the first. (N: 1 to 8)

13. PARAMETER LIST

MELSEC-QnA

	Setting		Reference Section/Reference Manual
	Default value	Setting range	
	–	–	Chapter 7
	0	0 to 8	
	No setting	Number of I/O points of CPU module	
	MINIS3	MINIS3/MINI() stations	
	X1000 to 200H	X, M, L, B, T, ST, C, D, W, R, ZR, none (Bit device: multiples of 16)	
	Y1000 to 200H	Y, M, L, B, T, ST, C, D, W, R, ZR, none (Bit device: multiples of 16)	
	5 times	0 to 32 times	
	CPU	CPU/Link	
	Clear	Clear/Hold	
	No setting	M, L, B, T, ST, C, D, W, R, ZR, none	
	No setting	D, W, T, ST, C, R, ZR	
	Stop	Continue/Stop	
	Latch data	Test message/OFF data/Latch data	
	–	–	QnACPU Programming Manual (Fundamentals)
	No setting	Program name/Scan/Low-speed/Initial/Standby	
	No setting	File name/Type/Transfer source drive/ Transfer destination drive	
	–	QCPU (Q mode)/QnACPU Programming Manual (SFC)	QCPU (Q mode)/QnACPU Programming Manual (SFC)
	–	–	GX Developer Operating Manual SW□IVD-GPPQ Software Package Operating Manual (Offline)

14 SELECTING MEMORY CARD MODELS

Since the QnACPU has a built-in RAM as a standard feature to store parameters and programs, programs can be executed without installing a memory card.
Each CPU model has a built-in RAM of the following program capacity.

Q2ACPU.....	28k steps	(112k bytes)
Q2ACPU-S1.....	60k steps	(240k bytes)
Q3ACPU.....	92k steps	(368k bytes)
Q4ACPU.....	124k steps	(496k bytes)

14.1 Applications of Memory Cards

A memory card is required in the following cases:

- (1) To perform a boot operation
Parameters, programs, initial device values, comments, and boot files are stored in a memory card, and they are loaded to the built-in RAM at the time of program execution.
- (2) To use file registers. ^{*1}
- (3) To use local devices. ^{*2}
- (4) To use a simulation data file with the simulation function. ^{*2}
- (5) To use the sampling trace function. ^{*2}
- (6) To use the status latch function. ^{*2}
- (7) To use the program trace function. ^{*2}
- (8) To store the breakdown history data in a file. ^{*2}
- (9) To execute programs of the maximum number of steps available for the QnACPU.
When a program of the maximum capacity is stored in the built-in RAM, the parameter files and initial device values must be stored in a memory card.
- (10) To use the SFC trace function. ^{*2}

^{*1} They will be read-only in programs if they are set in the ROM area of the memory card.

^{*2} Can only be set in the RAM area of the memory card.

14.2 Selecting Memory Card Capacity

Select a memory card capacity according to the types and sizes of files to be stored in the memory card. The sizes of files are calculated using the formulas presented below.

Function	Approximate File Capacity (Unit: Bytes)
Drive title	64
Keyword	72
Parameters ^{*3}	MELSECNET, NET/10 None → 330 When MELSECNET (II, /B) set → Max. 4096 per module
Boot file	(Number of files × 18) + 67
Sequence program ^{*3}	(Number of steps × 4) + 122
Device comments ^{*3}	(Total comment data size of each device) + 74 - Setting with GX Developer The comment data size of 1 device is as follows: 10250 × a + 40 × b + 10 (Quotient of (No. of devices / 256) is substituted for a and the remainder for b.) - Setting with SW□ IVD-GPPQ Although the size varies depending on EMS capacity, it is equivalent to or less than the size obtained in the above DX Developer case.
Initial device value ^{*3}	(Number of device points × 2) + (device types ^{*1} × 44) + 66
File register	Number of points for file registers × 2 bytes
Local device	(72 + (6 × No. of Setting range ^{*4}) + (2 × No. of word devices) + $\frac{\text{No. of bit devices}}{8} \times \text{No. of program files used}$ Round-up
Simulation data	(Number of word device points × 2) + $\frac{\text{number of bit device points}}{16} \times 2$ + (device ranges ^{*2} × 44) + 66 Rounded up
Sampling trace data	362 + (No. of word device points + No. of bit device points) × 12 + (N1 + N2 + N3 + No. of word device points × 2 + (No. of bit device points / 16) × 2) × trace count (total count) ^{*5} According to the items set in the added trace information on the trace device setting screen, the following values are added for N1 to N3. (Refer to Section 8.5 (2) (b)) N1: When setting time, "4" is added. N2: When setting step No., "10" is added. N3: When setting the program name, "8" is added.
Status latch data	For all devices : 58576 For detailed devices : (Number of word device points × 2) + $\frac{\text{number of bit device points}}{16} \times 2$ + (device types × 8) + 352 Rounded up
Program Trace Data	Same as sampling trace
Breakdown history data	54 × number of faults stored + 72 bytes
SFC trace data	Max. 48k (in 1 kbyte units)

*1 "Device types" represents the number of registered device names.

For example, if D, W, and T are registered, it is 3.

*2 "Device ranges" represents the number of registered range settings.

*3 These files can be transferred from the memory card to the built-in RAM in the boot operation.

*4 The total number of setting ranges is the total number of types of the devices that are set as local devices.

*5 Decimal fraction of "number of bit device points/16" is rounded up.

POINT	
	Note that the capacity may be rounded up as follows depending on the memory area used for storage: Built-in RAM..... 4096 bytes (1k step) units Memory card..... 512 bytes units Note that, when a file is transferred from the memory card to the built-in RAM in boot operation, the reserved capacity is changed after transfer.

15 HARDWARE SPECIFICATIONS OF CPU MODULES

15.1 SPECIFICATIONS

The general specification common to various modules is shown.

Specifications

Item	Specifications					
Operating ambient temperature	0 to 55℃					
Storage ambient temperature	-20 to 75℃					
Operating ambient humidity	10 to 90 % RH, No-condensing					
Storage ambient humidity	10 to 90 % RH, No-condensing					
Vibration resistance	Conforming to JIS B 3502, IEC 61131-2		Frequency	Acceleration	Amplitude	Sweep count
		Under intermittent vibration	10 to 57Hz	—	0.075mm (0.003 inch)	10 times each in X, Y, Z directions (for 80min.)
			57 to 150Hz	9.8m/s ²	—	
		Under continuous vibration	10 to 57Hz	—	0.035mm (0.001inch)	
			57 to 150Hz	4.9m/s ²	—	
Shock resistance	Conforming to JIS B 3502, IEC 61131-2 (147m/s ² , 3 times in each of 3 directions XYZ)					
Operation ambience	No corrosive gasses					
Operating elevation ^{*3}	2000m (6562 ft.) or less					
Installation location	Control panel					
Overvoltage category ^{*1}	II or lower					
Pollution degree ^{*2}	2 or lower					
Equipment category	Class I					

*1 This indicates that the equipment is assumed to be connected to which power distributor in the area from the public electrical power distribution network to machinery in the premises. Category II applies to equipment to which electrical power is supplied from fixed facilities. The surge voltage withstand level for up to the rated voltage of 300V is 2500V.

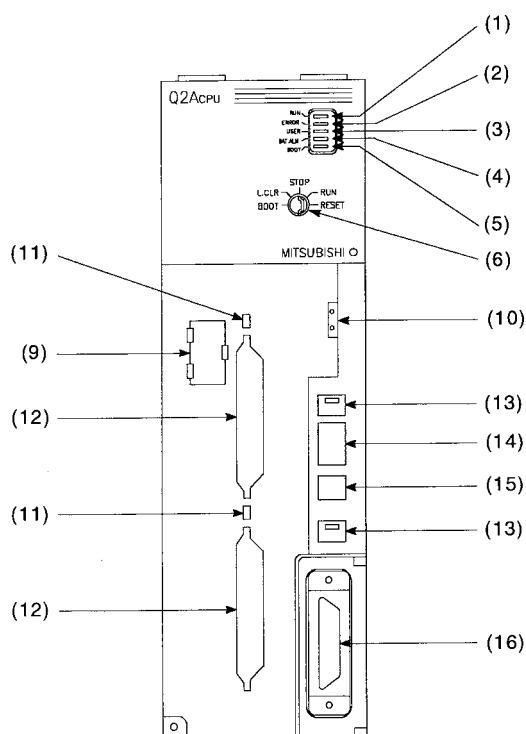
*2 This index indicates the degree of conductive material generation in the environment where the equipment is used.
In Pollution degree 2, only non-conductive pollution occurs. Occasionally, however, temporary conductivity caused by condensation can be expected.

*3 Do not use or store the PLC in the environment where the pressure is higher than the atmospheric pressure at sea level. Otherwise, malfunction may result.
To use the PLC in high-pressure environment, please contact your local Mitsubishi representative.

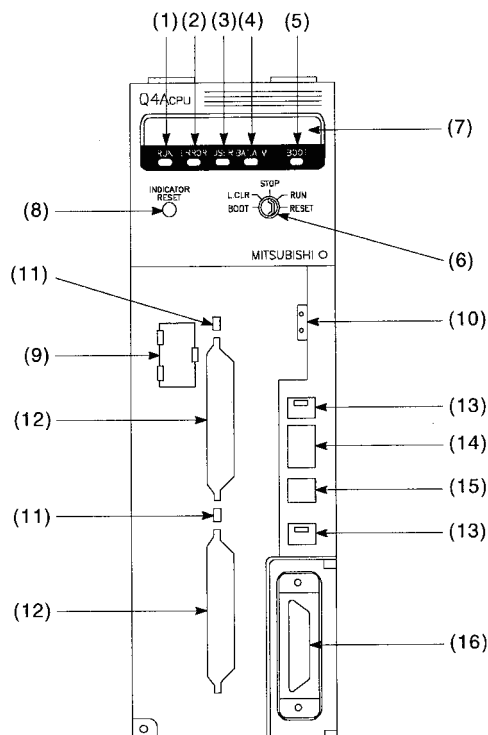
15.2 Part Names

The names of module parts and their settings are described here.

(1) Q2ACPU, Q2ACPU-S1



(2) Q3ACPU, Q4ACPU

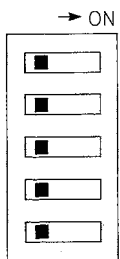
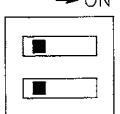


Viewed with the front cover open

No.	Name	Application
(1)	RUN LED	Indicates the operating state of the CPU module. ON: Operating with the RUN/STOP key switch set to RUN or STEP RUN. OFF: Stopped with the RUN/STOP key switch set to STOP, PAUSE, or STEP RUN. Or, an error that stops operation was detected. Flashing: The RUN/STOP key switch was shifted from STOP to RUN after writing a program in the STOP state. The CPU module is not in the RUN state. To restore the RUN state, turn the RUN/STOP key switch from RUN to STOP and back to RUN. Alternatively, reset it with the RUN/STOP key switch. (For the Q3ACPU and Q4ACPU, the message "PRG.CHECK!!" is displayed on the LED display.)
(2)	ERROR LED	ON: A self-diagnostic error except for a battery error, which does not stop operation, was detected. (When the parameter setting is made for operation to continue when an error occurs.) OFF: Normal Flashing: An error that stops operation was detected.
(3)	USER LED	ON: An error was detected by the CHK instruction, or an annunciator, F, turned ON. (For the Q3ACPU or Q4ACPU, a message or a comment for the annunciator is displayed on the LED display.) OFF: Normal Flashing: When latch clear is performed. (For the Q3ACPU and Q4ACPU, the message "L.CLR RDY" is displayed on the LED display.)
(4)	BAT.ALARM LED	ON: A battery error occurred due to low battery voltage in the CPU module or memory card. OFF: Normal

15. HARDWARE SPECIFICATIONS OF CPU MODULES

MELSEC-QnA

No.	Name	Application																																
(5)	BOOT LED	ON: Execution of the boot operation is completed. OFF: No boot operation has been executed.																																
(6)	RUN/STOP key switch	RUN/STOP: Starts/stops sequence program operation. L.CLR: Clears all data in the latch area (to "OFF" or "0") which is set with parameters. Clears sampling trace and status latch registrations. RESET: Resets the hardware. Resets and initializes operation when an operation error occurred.																																
(7)	LED display (Q3A, Q4ACPU only)	Can display up to 16 characters. Displays comments for errors detected in self-diagnosis, comments by LED display instructions, clock data by SET SM212, or annunciator F number comments by SET F instructions.																																
(8)	Display reset switch (Q3A, Q4ACPU only)	Switch used to clear the current LED display. The next data is displayed, if any.																																
(9)	Battery (A6BAT)	Backup battery for the built-in RAM and the power failure compensation function.																																
(10)	Battery connector pin	Used for connection of the battery lead wire. (To prevent battery drain, the battery lead wire is disconnected from the connector before shipment. See Section 18.6.)																																
(11)	Memory card EJECT button	Used to eject the memory card from the CPU module. (Refer to Section 18.7)																																
(12)	Memory card installing connector	Connector for installing the memory card in the CPU module.																																
(13)	Memory card in/out switch (with built-in LED) 	Used to enable/disable memory card installation or removal while the power is ON. Factory-set to OFF . ON: Cannot be removed (LED lit) OFF: Can be removed (LED unlit) Refer to Section 15.3 (3) and (4) for installation or removal of a memory card.																																
(14)	System setting switch 1 	Settings required to operate the CPU module are made. All switches are set to OFF before shipment.																																
		SW1: Boot setting Setting of the memory used for operation. ON: Boot operation OFF: Boot operation is not performed.																																
		SW2 to 4: Parameter area Setting of the memory in which parameters are written.																																
		<table><tr><th rowspan="2">System setting switch 1</th><th rowspan="2">Built-in RAM</th><th colspan="2">Memory Card A</th><th colspan="2">Memory Card B</th><th rowspan="2">*SW2 to 4 are valid even if SW1 is OFF.</th></tr><tr><th>RAM</th><th>ROM</th><th>RAM</th><th>ROM</th></tr><tr><td>SW2</td><td>OFF</td><td>ON</td><td>OFF</td><td>ON</td><td>OFF</td><td></td></tr><tr><td>SW3</td><td>OFF</td><td>OFF</td><td>ON</td><td>ON</td><td>OFF</td><td></td></tr><tr><td>SW4</td><td>OFF</td><td>OFF</td><td>OFF</td><td>OFF</td><td>ON</td><td></td></tr></table>	System setting switch 1	Built-in RAM	Memory Card A		Memory Card B		*SW2 to 4 are valid even if SW1 is OFF.	RAM	ROM	RAM	ROM	SW2	OFF	ON	OFF	ON	OFF		SW3	OFF	OFF	ON	ON	OFF		SW4	OFF	OFF	OFF	OFF	ON	
		System setting switch 1			Built-in RAM	Memory Card A		Memory Card B		*SW2 to 4 are valid even if SW1 is OFF.																								
			RAM	ROM		RAM	ROM																											
		SW2	OFF	ON	OFF	ON	OFF																											
SW3	OFF	OFF	ON	ON	OFF																													
SW4	OFF	OFF	OFF	OFF	ON																													
SW5: System protect Prohibition of all writing and control directions to the CPU module. ON: System protection enabled OFF: System protection disabled																																		
(15)	System setting switch 2 	Settings required to operate the CPU module are made. All switches are set to OFF before shipping.																																
		SW1: Not used. (Fixed to OFF.)																																
		SW2: Peripheral protocol. Select the type of the peripheral device connected to the peripheral interface of the CPU module. (When accessing an ACPU on another station from a peripheral device for ACPU, set this switch to "ON". The setting becomes valid immediately after switching.) ON: Peripheral device for ACPU OFF: Peripheral device for QnACPU																																

15. HARDWARE SPECIFICATIONS OF CPU MODULES

MELSEC-QnA

No.	Name	Application
(16)	RS-422 connector	Connector for connecting to a peripheral device.

15.3 Relationship between Switch Operations and LEDs/LED Display

(1) Writing programs with the CPU module in STOP state

To write a program to the CPU module while it is in the STOP state, use the following procedure.

1) Set the RUN/STOP key switch to STOP.

RUN LED	:OFF	CPU module in STOP state → Program write (program write executed)
Display on Q3ACPU, Q4ACPU	:OFF	

2) Set the RUN/STOP key switch to RESET

RUN LED	:OFF	CPU module in RESET state
Display on Q3ACPU, Q4ACPU	:OFF	

3) Set the RUN/STOP key switch to STOP → RUN

RUN LED	:ON	CPU module in RUN state
Display on Q3ACPU, Q4ACPU	:OFF	

POINT						
(1)	For the QnACPU, after writing a program (except for writing to PLC during RUN), set the CPU module to RESET and then to RUN.					
(2)	If the key switch is set to RUN without resetting, the CPU module will remain in STOP state displaying as follows:					
	<table> <tr> <td>RUN LED</td> <td>:Flashing</td> <td rowspan="2">} *1</td> </tr> <tr> <td>Display on Q3ACPU, Q4ACPU</td> <td>:Displays "PRG.CHECK!!"</td> </tr> </table>	RUN LED	:Flashing	} *1	Display on Q3ACPU, Q4ACPU	:Displays "PRG.CHECK!!"
RUN LED	:Flashing	} *1				
Display on Q3ACPU, Q4ACPU	:Displays "PRG.CHECK!!"					
	After this occurs, the CPU can be placed into RUN state by setting the RUN/STOP key switch to RESET.					
	In this case, internal CPU module data such device data are cleared.					
(3)	To prevent the internal CPU module information from being cleared, switch the RUN/STOP key switch STOP → RUN again without resetting.					

*1 If Remote STOP → RUN is performed for the CPU module, the CPU will be in RUN status, not in "PROG.CHECK" status.

(2) Performing latch clear

To perform latch clear, operate the RUN/STOP key switch as follows.

1) Turn the RUN/STOP key switch to L.CLR three times.

USR LED	: Flashing	Ready for latch
Display on Q3ACPU, Q4ACPU	: Displays "L.CLR RDY".	clear

2) Turn the RUN/STOP key switch to "L.CLR" once again.

USR LED	: ON for 2 seconds	Latch clear
Display on Q3ACPU, Q4ACPU	: Displays "L.CLR OK"	completed
	for 2 seconds	

POINT	
(1)	The latch clear operation can be set enabled or disabled for each device in the device setting in the parameter mode.
(2)	Remote latch clear executed by the GPP function is an alternative method other than using the RUN/STOP key switch. (Refer to Section 10.6.5).

(3) Removing a memory card while the PLC power is ON:

When removing a memory card with the PLC power ON, operate the memory card in/out switch as follows:

1) In/out switch: ON.

LED in the switch	:ON	Memory card removal prohibited

2) In/out switch: OFF

LED in the switch	:OFF	Memory card removal permitted
		Removal of memory card

POINT	
(1)	The LED in the in/out switch may not come OFF if the memory card is being used for a CPU module system function (sampling trace, status latch, etc.) or by a program. In this case, abort the function or program that is using the memory card. After aborting it, confirm that the LED in the in/out switch has gone OFF, then remove the memory card.
(2)	When a file register, local device or breakdown history set with parameters is present, the memory card cannot be removed. Even if the memory card in/out switch is turned OFF, its built-in LED does not turn OFF. When the file register is set to "Not used" with the QDRSET (P) instruction, the memory card can be removed.
(3)	After removing the memory card, do not turn the memory card in/out switch ON. Doing so will result in an error.

- (4) Installing a memory card while the PLC power is ON:

When installing a memory card with the PLC power ON, operate the memory card in/out switch as follows:

1) Install the memory card.

2) In/out switch: ON

LED in the switch :ON Memory card removal prohibited

POINT	
(1)	After installing the memory card, set the memory card in/out switch to ON. If it is not set to ON, the memory card cannot be used.
(2)	During one scan after the memory card installation, mounting processing is performed again. Note that the scan time may be increased by 10ms at maximum.

16 POWER SUPPLY MODULE

This section describes the specifications and selection of power supply modules.

16.1 Specifications

16.1.1 Power supply module specifications

(1) Standard power supply module

Power supply module specifications

Item		Specifications						
		A61P	A61PN	A62P	A63P	A65P	A66P	A67P
Slot position		Power supply module slot					I/O module slot	Power supply module slot
Input power supply		100VAC to 120VAC ^{+10%} _{-15%} (85VAC to 132VAC)			24VDC ^{+30%} _{-35%} (15.6VDC to 31.2VDC)	100VAC to 120VAC ^{+10%} _{-15%} (85VAC to 132VAC)		110VDC (85VDC to 140VDC)
		200VAC to 240VAC ^{+10%} _{-15%} (170VAC to 264VAC)				200VAC to 240VAC ^{+10%} _{-15%} (170VAC to 264VAC)		
Input frequency		50/60Hz ± 5%			—	50/60Hz ± 5%		—
Input voltage distortion		Within 5% (See Section 19.8)			—	Within 5% (See Section 19.8)		—
Max. input apparent power		160VA		155VA	65W	110VA	95VA	65W
Inrush current		20A, 8ms or less*4			100A, 1ms or less	20A, 8ms or less*4		20A, 8ms or less
Rated output current	5VDC	8A		5A	8A	2A	—	8A
	24VDC	—		0.8A	—	1.5A	1.2A	—
Overcurrent protection*1	5VDC	8.8A or higher		5.5A or higher	8.5A or higher	2.2A or higher	—	8.5A or higher
	24VDC	—		1.2A or higher	—	2.3A or higher	1.7A or higher	—
Overvoltage protection*2	5VDC	5.5 to 6.5V		5.5 to 6.5V	5.5 to 6.5V	5.5 to 6.5V	—	5.5 to 6.5V
	24VDC	—						
Efficiency		65% or higher						
Dielectric withstand voltage		Between AC external terminals and ground, 1500V AC, 1 minute Between DC external terminals and ground, 500V AC, 1 minute						
Noise durability		Checked by noise simulator of noise voltage 1500Vp-p, noise width 1 μs, and noise frequency 25 to 60Hz			Checked by noise simulator of noise voltage 500Vp-p, noise width 1 μs, and noise frequency 25 to 60Hz	Checked by noise simulator of noise voltage 1500Vp-p, noise width 1 μs, and noise frequency 25 to 60Hz		
Insulation resistance		Between AC external terminals and ground, 5MΩ or higher by 500VDC insulation resistance tester						
Power indicator		LED indication of power supply						
Terminal screw size		M4 × 0.7 × 6					M3 × 0.5 × 6	M4 × 0.7 × 6

16. POWER SUPPLY MODULE

MELSEC-QnA

Item	Specifications						
	A61P	A61PN	A62P	A63P	A65P	A66P	A67P
Applicable wire size	0.75 to 2mm ²						
Applicable solderless terminal	R1.25-4, R2-4 RAV1.25, RAV2-4					R1.25-3, R2-3 RAV1.25-3, RAV2-3	R1.25-4, R2-4 RAV1.25-4, RAV2-4
Applicable tightening torque	78 to 118N · cm					39 to 59N · cm	78 to 118N · cm
External dimensions	250(H)mm (9.8inch) × 55(W)mm (2.1inch) × 121(D)mm (4.7inch)					250(H)mm (9.8inch) × 37.5(W)mm (1.5inch) × 121(D)mm (4.7inch)	250(H)mm (9.8inch) × 55(W)mm (2.1inch) × 121(D)mm (4.7inch)
Weight	0.98 kg	0.75 kg	0.94 kg	0.8 kg	0.94 kg	0.75 kg	0.8 kg
Allowable momentary power failure period ^{*3}	20ms or less			1ms or less	20ms or less	—	20ms or less (at 100V DC)

REMARK

- 1) The number of occupied slots for the A66P is 1.

(2) CE-compliant power supply module

Power supply module specifications

Item		Performance specifications	
		A61PEU	A62PEU
Slot position		Power supply module slot	
Input power supply		100 to 120/200 to 240VAC +10%/-15%	
Input frequency		50/60Hz ± 5%	
Input voltage distortion		Within 5% (See Section 19.8)	
Max. input apparent power		130VA	155VA
Inrush current		20A, 8ms or less*4	
Rated output current	5VDC	8A	5A
	24VDC	–	0.8A
Overcurrent protection*1	5VDC	8.8A or higher	5.5A or higher
	24VDC	–	1.2A or higher
Overvoltage protection*2	5VDC	5.5 to 6.5V	–
	24VDC	–	
Efficiency		65% or higher	
Dielectric withstand voltage	Between primary side and FG	2830V AC rms/3 cycles (altitude 2000m (6562ft.))	
Noise durability		Checked by noise simulator of noise voltage IEC801-4, 2kV, 1500Vp-p, noise width 1 μs, and noise frequency 25 to 60Hz	
Power indicator		LED indication of power supply	
Terminal screw size		M4 × 0.7 × 6	
Applicable wire size		0.75 to 2mm ²	
Applicable solderless terminal		RAV1.25-4, RAV2-4	
Applicable tightening torque		98 to 137N · cm	
External dimensions		250(H)mm (9.8inch) × 55(W)mm (2.1inch) × 121(D)mm (4.7inch)	
Weight		0.8 kg	0.9 kg
Allowable momentary power failure period*3		20ms or less	

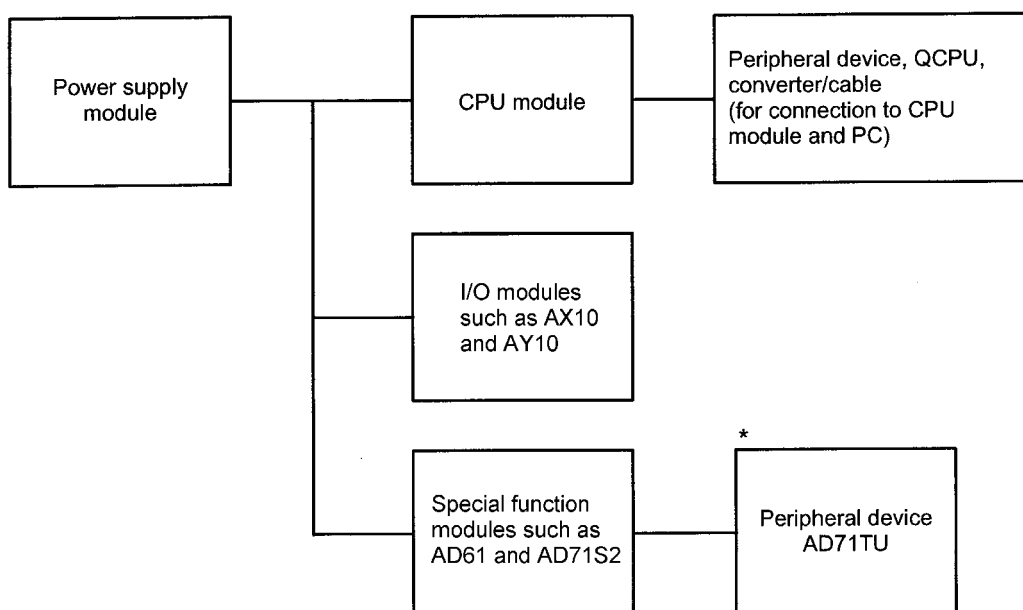
POINT	
*1	Overcurrent protection (a) The overcurrent protector shuts off the 5VDC and/or 24VDC circuit(s) and stops the system if the current exceeding the specified value flows in the circuit(s). As this results in voltage drop, the power supply module LED turns OFF or is dimly lit. (b) When this device is activated, eliminate probable causes such as insufficient current capacity or short circuit, and then start the system. When the current has reached the normal value, the system will start from the first.
*2	Overvoltage protection The overvoltage protector shuts off the 5VDC circuit and stops the system if overvoltage of 5.5 to 6.5V is applied to the circuit. The power supply module LED turns OFF. When restarting the system, switch the input power OFF, then back ON. The system is started up with an initial start. If the system is not booted and the LED remains off, this means that the power supply module has to be replaced.
*3	Allowable momentary power failure period The allowable momentary power failure period of PLC CPUs varies depending on the power supply module used. In the system using the A63P, it is the time from when the primary side of the stabilized power supply supplying 24VDC to the A63P turns OFF until the voltage (secondary side) has dropped from 24VDC to the specified value (15.6VDC) or less.
*4	Inrush current If power is reapplied immediately after power OFF (within 5 seconds), an inrush current exceeding the specified value may flow (for 2ms or less). Therefore, before reapplying power, make sure that 5 seconds have elapsed after power off. When selecting a fuse or breaker for an external circuit, consider the above as well as meltdown and detection characteristics.

16.1.2 Power supply module selection

A power supply module is selected based on to the total current consumption of I/O modules, special function modules and peripheral devices to which power is supplied by the power supply module. When an extension base unit, A52B, A55B, or A58B is used, take into consideration that power to the module is supplied by the power supply module on the main base.

For 5VDC current consumption of I/O modules, special function modules and peripheral devices, refer to Section 3.3.

For devices purchased by users, refer to the manual for each device.



- * When selecting a power supply module, take account of the current consumption of the peripheral devices connected to special function modules.
For example, when connecting the AD71TU to AD71-S2, the current consumption of the AD71TU should also be taken into consideration.

- (1) Selecting a power supply module when using extension base unit(s), A52B, A55B, and/or A58B

When an extension base unit, A52B, A55B, or A58B is used, 5VDC power supply is supplied from the power supply module on the main base unit via an extension cable. Thus, when one of these units is used, pay attention to the following:

- (a) When mounting a power supply module on the main base unit, select a model that can cover 5VDC current consumed by modules mounted on the A52B, A55B, and/or A58B.

Example

If 5VDC current consumptions on the main base unit and on the A55B are 5A and 2A respectively, the power supply module to be installed to the main base unit is the A61P (5VDC, 8A).

- (b) Since power to the A52B, A55B, or A58B is supplied via an extension cable, a voltage drop occurs through the cable. It is necessary to select a power supply module and cables with proper length so that 4.75VDC or more is available on the receiving end.

For details of voltage drop, refer to Section 17.3 Application Standards of Extension Base Units.

- (2) Handling precautions for the A66P

- (a) Use the A66P on the base unit where no module, a dummy module or a blank cover is installed to the rightmost slot or the right adjacent slot.
- (b) The A66P output current (24VDC) depends on the left-hand adjacent module as shown below.

Left Hand Adjacent Module	Power Supply Module	Input Module Dummy Module	Output Module Special Function Module	Empty
Configuration	Power supply module A66P Empty	Input module Dummy module A66P Empty	Output module Special function module A66P Empty	Vacant A66P Empty
Max. output current for 24 VDC	0.5 A	1.2 A	1.0 A	1.5 A

16.1.3 Fuse specifications

This section describes the specifications of fuses used for the power supply modules and output modules.

Fuse specifications

Item	Model Name							
	GTH4 or FGTA250V 4A	SM6.3A or FGTA250V 6A	MF51NM8 or FGMA250V 8A	HP-32	HP-70K	MP-20	MP-32	MP-50
Application	Power supply module For A61P, A61PN, A61PEU, A62P, A62PEU, A65P, A66P, A67P	Power supply module For A63P	Output module For AY11E, AY13E	Output module For AY23	Output module For AY22	Output module For AY50, AY80	Output module For AY60	Output module For AY60E
Type	Cartridge type	Cartridge type	Cartridge type	Plug type	Plug type	Plug type	Plug type	Plug type
Rated current	4A	6.3A	8A	3.2A	7A	2A	3.2A	5A
External dimensions	$\phi 6 (0.2) \times 32 (1.2)$ mm (inch)	$\phi 6 (0.2) \times 32 (1.2)$ mm (inch)	$\phi 5.2 (0.2) \times 20 (0.8)$ mm (inch)	30.3mm (1.2inch) $\times$ 8mm (0.3inch) $\times$ 20mm (0.8inch)	30.3mm (1.2inch) $\times$ 8mm (0.3inch) $\times$ 20mm (0.8inch)	17.2mm (0.7inch) $\times$ 5.5mm (0.2inch) $\times$ 19mm (0.7inch)	17.2mm (0.7inch) $\times$ 5.5mm (0.2inch) $\times$ 19mm (0.7inch)	17.2mm (0.7inch) $\times$ 5.5mm (0.2inch) $\times$ 19mm (0.7inch)

16.2 Handling precautions

**CAUTION**

- Use the PLC under the environment specified in the user's manual.
Otherwise, it may cause electric shocks, fires, malfunctions, product deterioration or damage.
- Insert the module fixing projection into the fixing hole in the base unit to mount the module.
Incorrect installation could result in malfunction, failure, or a drop of the module.
For use in an environment of frequent vibrations, secure the module with screws.
Tighten the screws within the specified torque range.
If the screw is too loose, it may cause a drop of the module, a short circuit or malfunctions.
If too tight, it may cause damage to the screws and/or module, resulting in an accidental drop of the module, short circuit or malfunctions.
- Connect the extension cable to the connector of the base unit or module.
Check for incomplete connection after installing it.
Poor electrical contact may cause incorrect inputs and/or outputs.
- Insert the memory card and fully press it to the memory card connector.
Check for incomplete connection after installing it.
Poor electrical contact may cause malfunctions.
- Be sure to shut off all phases of the external power supply used by the system before mounting or removing the module.
Failure to do so may damage the module.
- Do not directly touch the conductive part or electronic components of the module.
Doing so may cause malfunctions or a failure of the module.

This section explains some notes on handling the CPU module, I/O module, special function module, power supply module, and base unit.

- (1) Do not drop or allow any impact to the module case, memory card, terminal block connector, and pin connector since they are made of resin.
- (2) Do not remove the printed-circuit board from the module case. Doing so may cause a malfunction.
- (3) Use caution to prevent foreign matter, such as wire chips, from entering the module during wiring.
If any foreign matter has entered the module, remove it.

- (4) Tighten the module installation screws and terminal block screws within the tightening torque range specified shown in the table below.

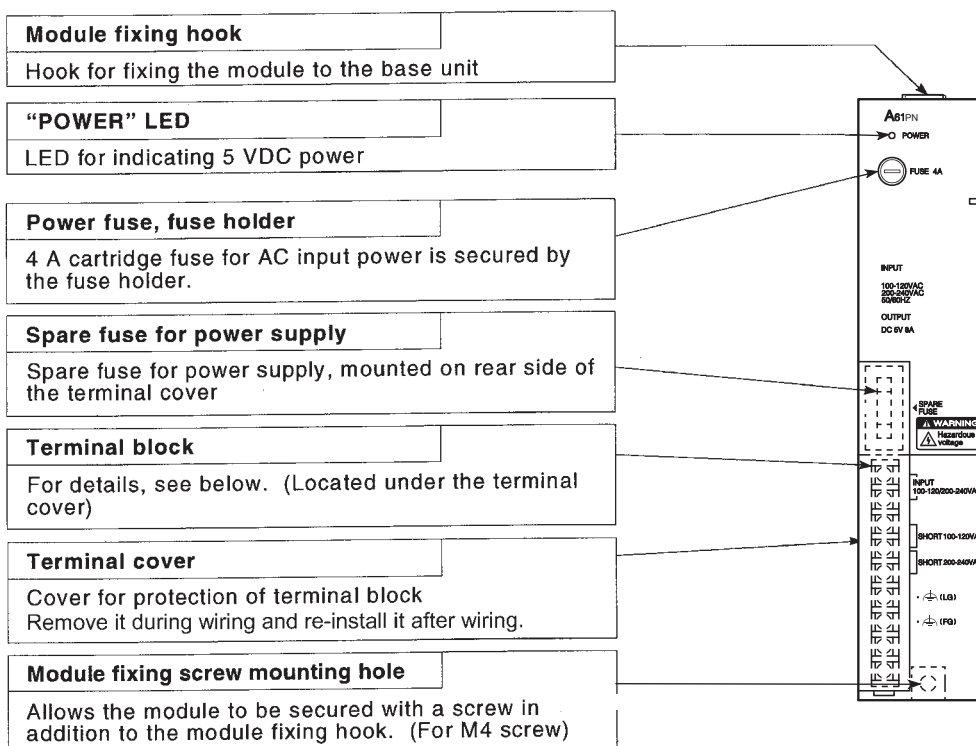
Screw	Tightening torque range
Module mounting screws (M4) (Optional)	78 to 118N · cm
Terminal block screws	98 to 137N · cm

- (5) When installing the module to the base unit, press the module completely so that its hook is locked into the base. To remove the module, push the hook to unlock, and pull it after confirming it is completely disengaged from the base.

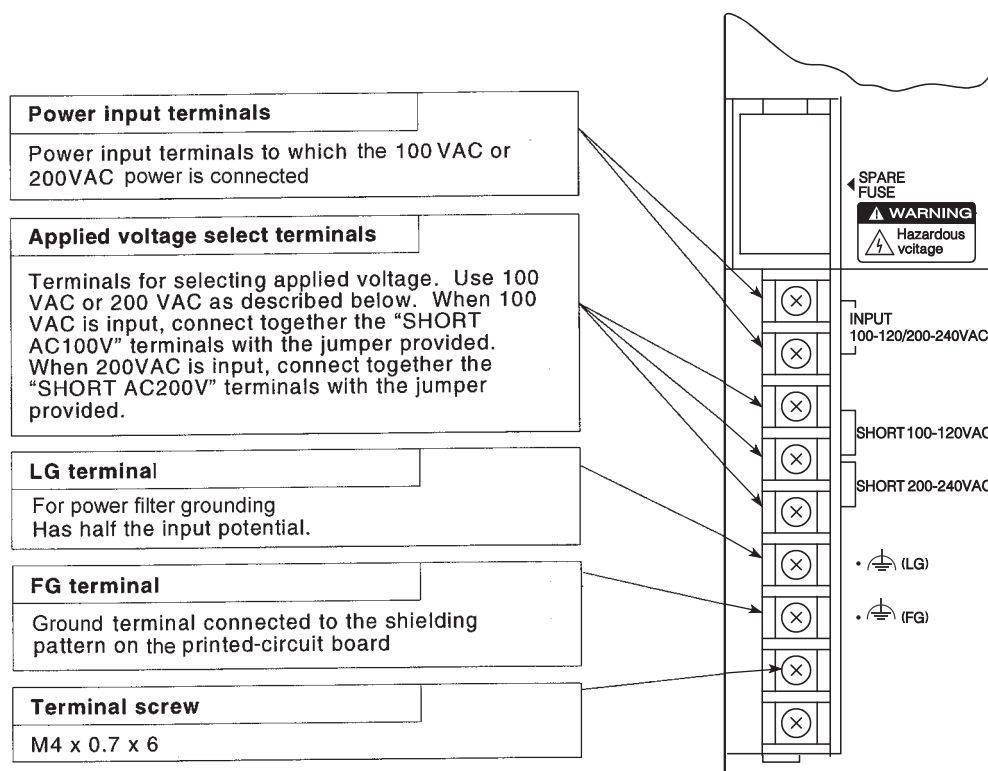
16.3 Part Names

Part names of the power supply modules are shown here.

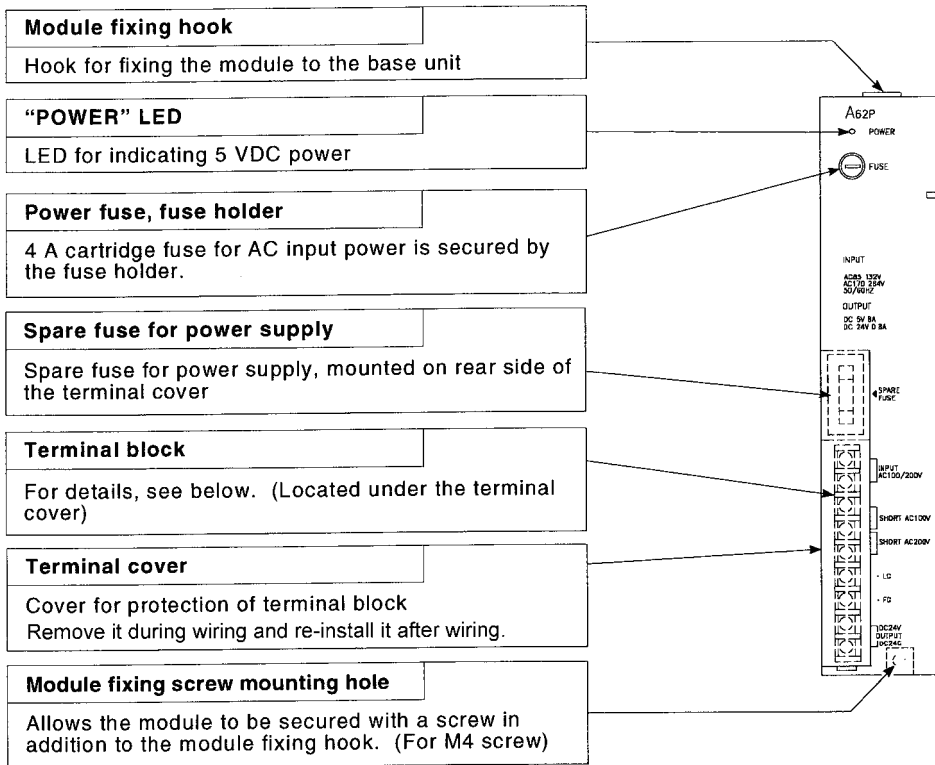
(1) Names and description of parts of the A61P, A61PN and A61PEU module



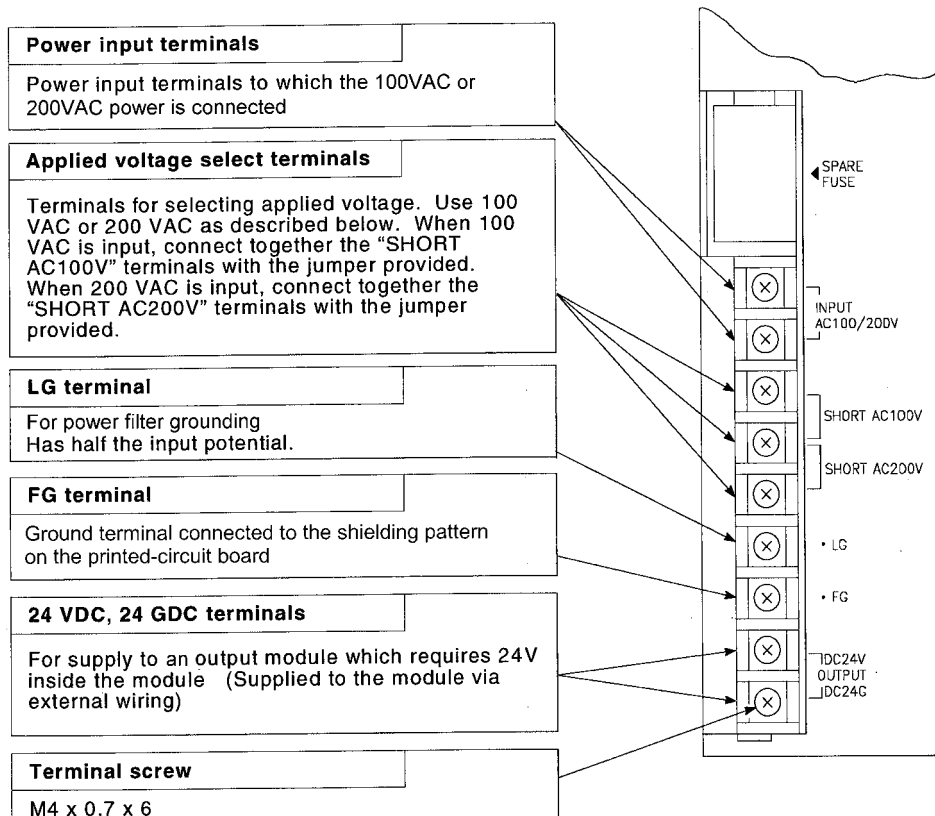
Terminal details



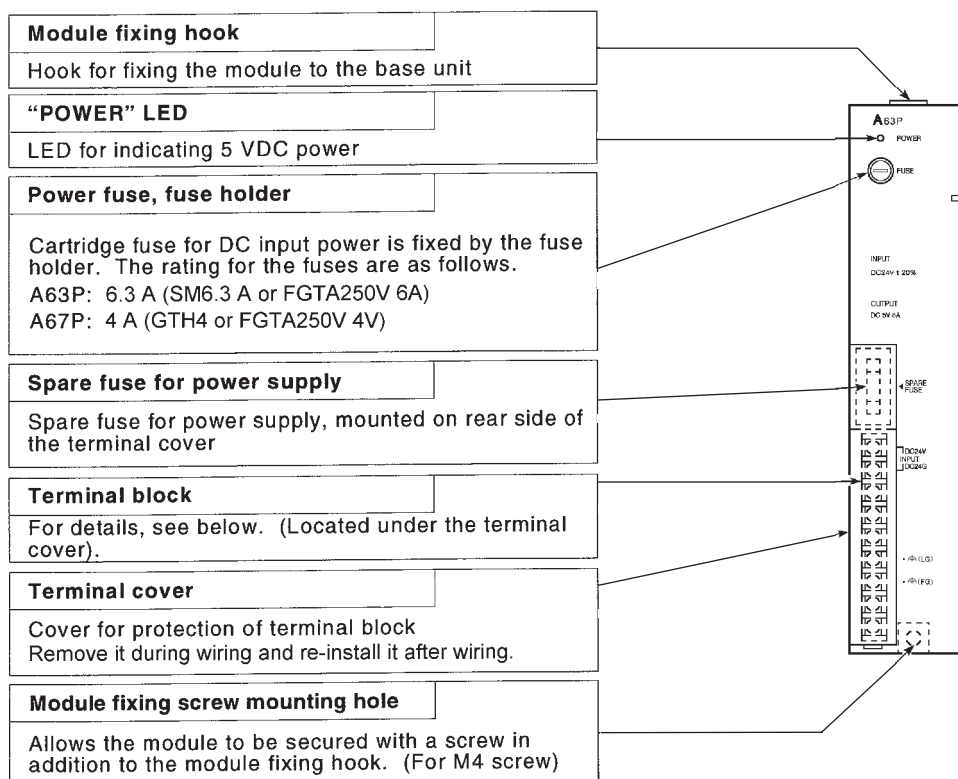
(2) Names and description of parts of the A62P, A62PEU and A65P module



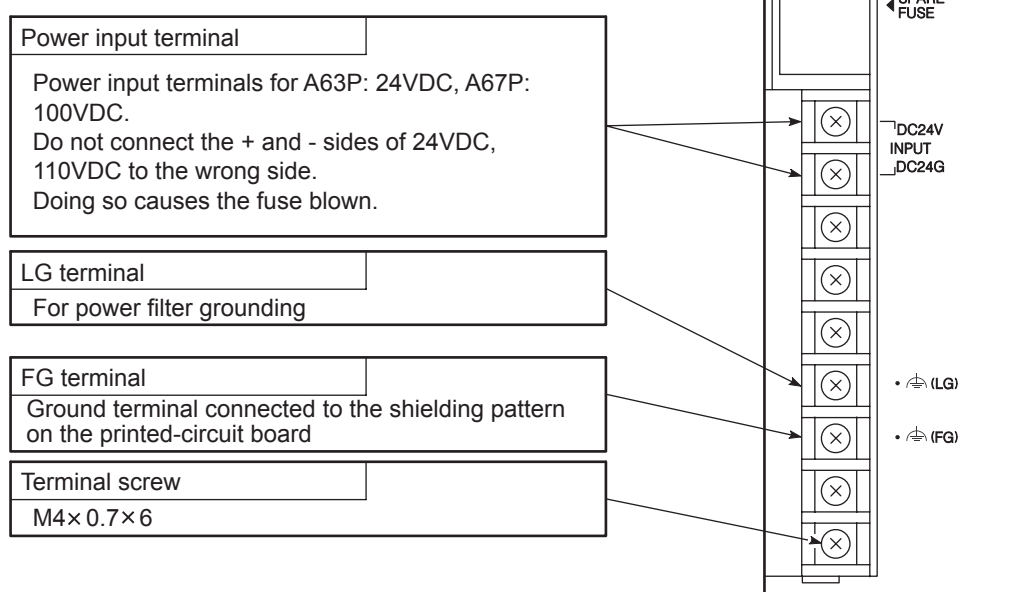
Terminal details



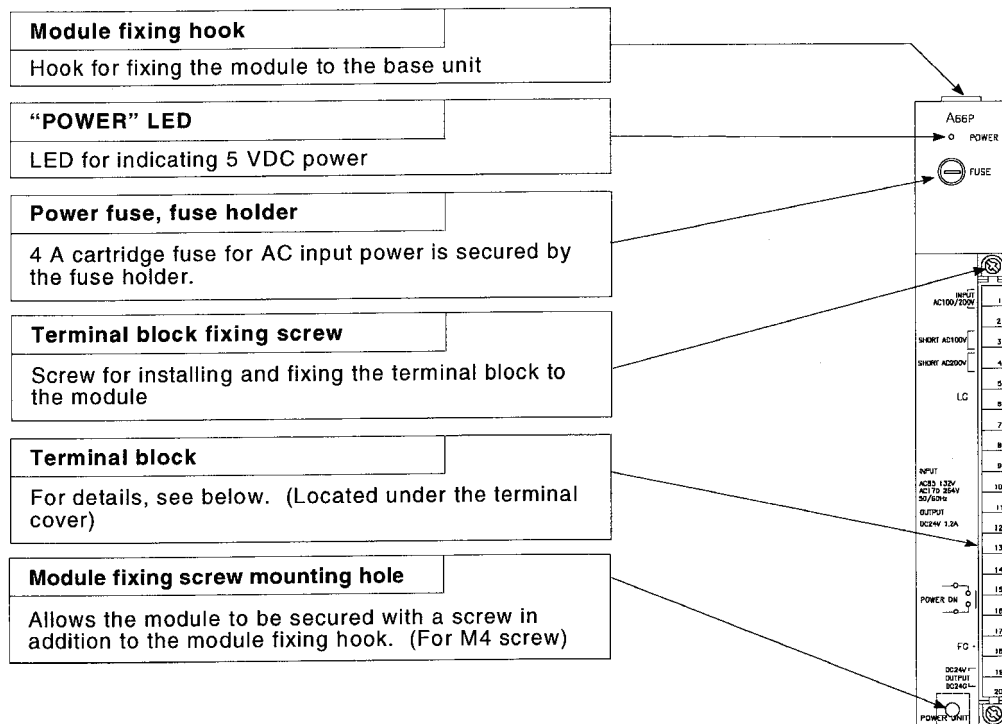
(3) Names and description of parts of the A63P and A67P module



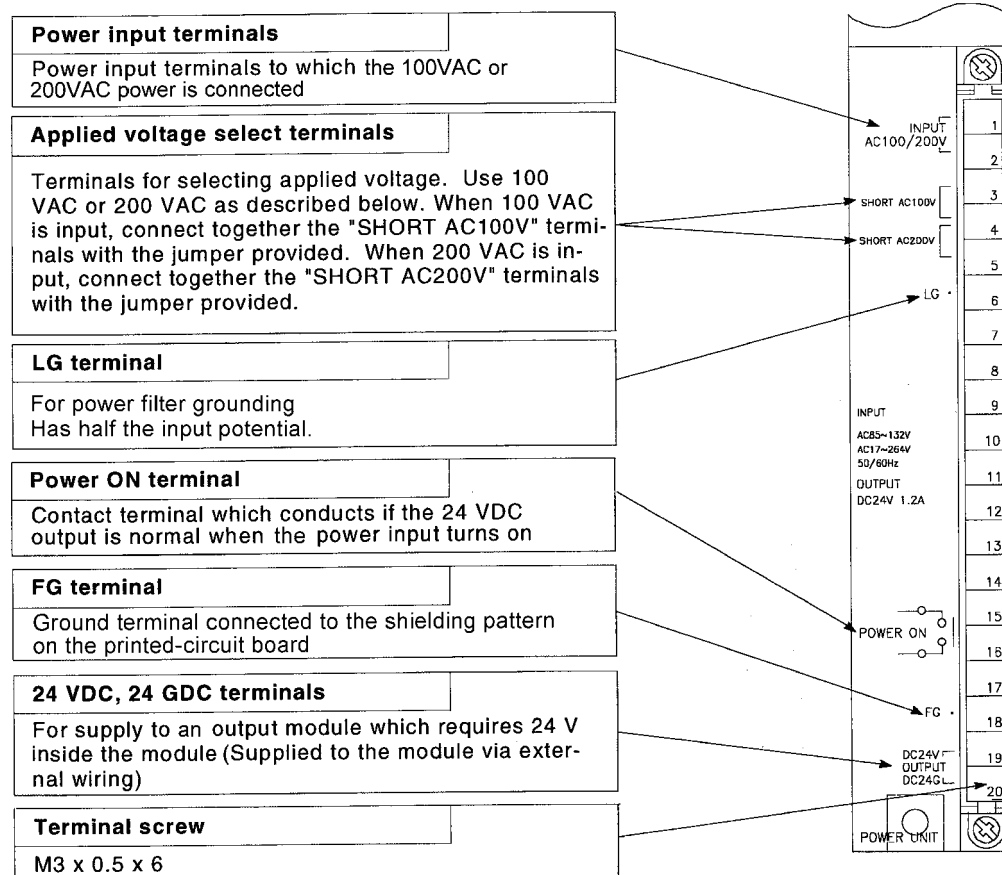
Terminal details



(4) Names and description of parts of the A66P

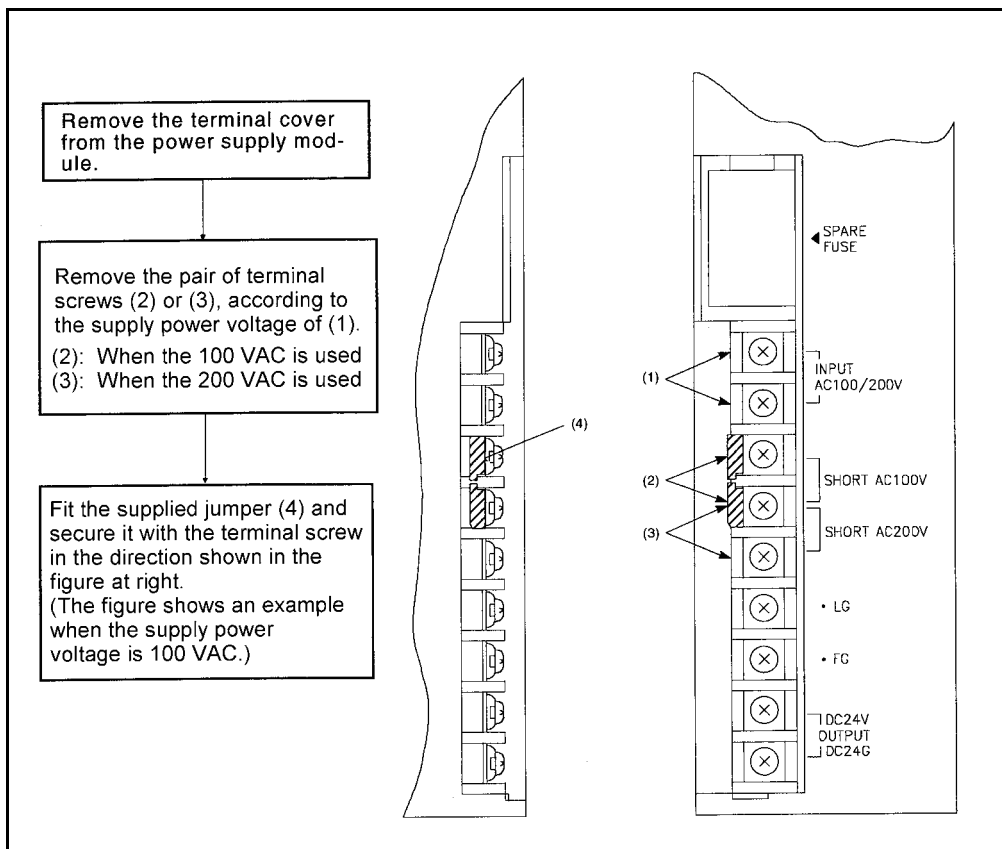


Terminal details



(5) Setting

On the A61P(EU), A62P(EU), A65P or A66P power supply module, the input voltage select terminals must be short-circuited by a jumper (accessory). The following explains the way of setting.



POINT

If the setting differs from the supply power voltage, the following occurs. Be sure to set it correctly.

	Supply Power Voltage	
	100VAC	200VAC
Set to 100VAC (jumper fitted as indicated at (2))	—	The power supply module is damaged. (The CPU module is not damaged.)
Set to 200VAC (jumper fitted as indicated at (3))	No fault occurs in the module. However, the CPU module does not operate.	—
No setting (jumper not fitted)	No fault occurs in the module. However, the CPU module does not operate.	

17 BASE UNIT AND EXTENSION CABLE

This section explains the specifications of the base units (the main and extension base units) and extension cables available for the systems, and the application standards for use of extension base units.

17.1 Specifications of Base Units

(1) Main base unit specifications

Item	Model Name			
	A32B	A32B-S1	A35B	A38B/A38HB/A38HBEU
I/O module installation range	2 modules can be installed.		5 modules can be installed.	8 modules can be installed.
Extension possibility	Not extendable	Extendable	Extendable	Extendable
Installation hole size	$\phi 6$ bell-shaped holes (for M5 screws)			
External dimensions	247mm (9.6inch) × 250mm (9.8inch) × 29mm (1.1inch)	268mm (10.5inch) × 250mm (9.8inch) × 29mm (1.1inch)	382mm (14.9inch) × 250mm (9.8inch) × 29mm (1.1inch)	480mm (18.7inch) × 250mm (9.8inch) × 29mm (1.1inch)
Weight	0.96kg	1.3kg	1.5kg	1.9kg

(2) Extension base unit specifications

Item	Model Name					
	A62B	A65B	A68B	A52B	A55B	A58B
I/O module installation range	2 modules can be installed.	5 modules can be installed.	8 modules can be installed.	2 modules can be installed.	5 modules can be installed.	8 modules can be installed.
Power supply module loading	Power supply module required			Not required. (See POINT .)		
Installation hole size	$\phi 6$ bell-shaped holes (for M5 screws)			$\phi 6$ bell-shaped holes (for M5 screws)		
Terminal screw size	—			M4 × 0.7 × 6 (FG terminal)		
Applicable wire size	—			0.75 to 2mm ²		
Applicable solderless terminal	—			(V)1.25-4, (V)1.25-YS4, (V)2-YS4A Applicable tightening torque: 78 to 118N · cm		
External dimensions	283mm (11.0inch) × 250mm (9.8inch) × 29mm (1.1inch)	352mm (13.7inch) × 250mm (9.8inch) × 29mm (1.1inch)	466mm (18.2inch) × 250mm (9.8inch) × 29mm (1.1inch)	183mm (7.1inch) × 250mm (9.8inch) × 29mm (1.1inch)	297mm (11.6inch) × 250mm (9.8inch) × 29mm (1.1inch)	411mm (16.0inch) × 250mm (9.8inch) × 29mm (1.1inch)
Weight	1.1kg	1.4kg	1.9kg	1.0kg	1.2kg	1.7kg
Accessory	—			*1 Dustproof cover (for I/O module): 1 pc.		

*1 1 For the attachment of the dustproof cover, refer to Section 19.6.

POINT	
(1)	The 5 VDC power of the A52B, A55B, and A58B is supplied from the power supply module mounted on the main base unit.
(2)	Before using the A52B, A55B or A58B, refer to Section 16.1.2 "Power supply module selection" and Section 17.3 "Application Standards of Extension Base Units".

17.1.1 Main base unit for high-speed access (A38HB/A38HBEU)

The main base units, (A38HB/A38HBEU) for high-speed access have been improved in the speed of access to the buffer memory of the special function module mounted on A38HB/A38HBEU.

POINT	
(1)	The A38HB/A38HBEU can perform high-speed access to the buffer memories of special function modules only. I/O devices of I/O modules are not accessed at high speed but at the same access speed as that of a conventional main base unit.
(2)	When an extension base unit is connected to the A38HB/A38HBEU, the buffer memories of the special function modules on the extension base unit are not accessed at high speed. The access speed is the same as the one in the case of connecting to a conventional main base unit.

REMARK

- (1) The A38HB/A38HBEU base unit is dedicated to the QnACPU and cannot be used with the ACPU.
- (2) When using the simulation module A6SIM-X64Y64, set its base unit specification to "1" or later.
If "0" is set, the A6SIM-X64Y64 does not operate normally.
When "0" is to be set for the base unit specification of the A6SIM-X64Y64, replace the base unit with the A38B.

17.2 Extension Cable Specifications

The specifications of the extension cables used for the QnACPU system are shown below:

Item	Model Name		
	AC06B	AC12B	AC30B
Cable length	0.6m (2.05ft.)	1.2m (3.9ft.)	3m (9.8ft.)
Resistance value of 5VDC supply line (at 55 °C)	0.019 Ω	0.028 Ω	0.052 Ω
Application	▪ For connection between main base and extension base ▪ For connection between extension bases		
Weight	0.34kg	0.52kg	1.06kg

**CAUTION**

- Connect the extension cable to the connector of the base unit or module.
Check the cable for incomplete connection after connecting it.
Poor electrical contact may cause incorrect inputs and/or outputs.
- When using extension cables, keep them away from the main circuit cables (high voltage, large current).

17.3 Application Standards of Extension Base Units (A52B, A55B, A58B)

To the A52B, A55B and A58B extension base units, 5VDC is supplied from the power supply module on the main base unit. (Power is not supplied from any power supply module on the A62B, A65B and A68B.)

Therefore, if a voltage drop occurs on an extension cable, the specified voltage may not be supplied to the receiving end, resulting in erroneous inputs and outputs.

It is recommended to connect the A52B, A55B and/or A58B after a main base unit to minimize a voltage drop.

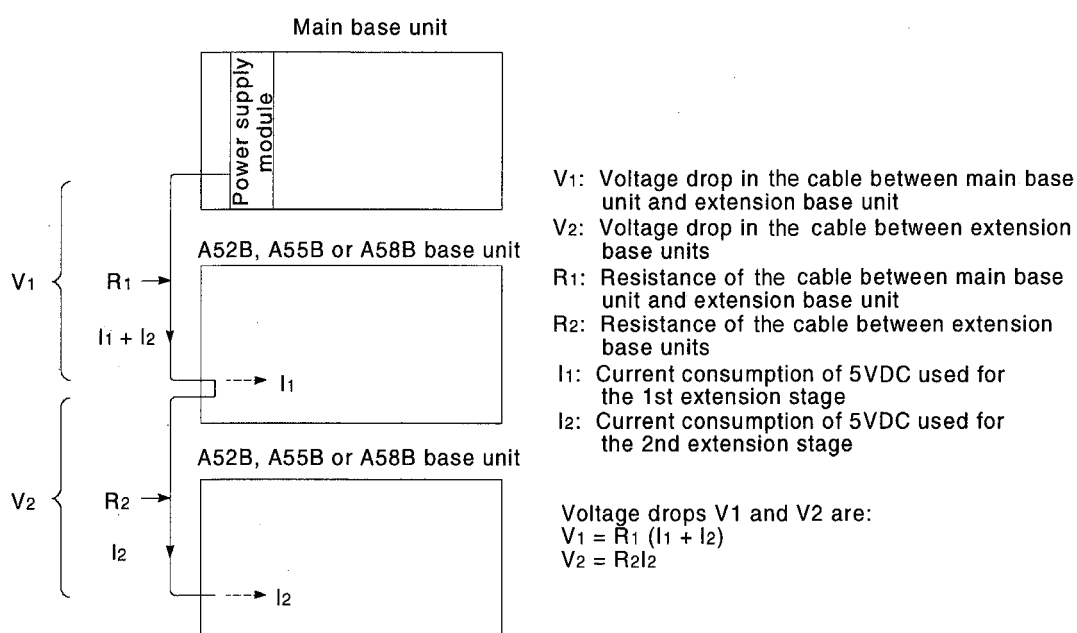
Determine applicability of the A52B, A55B and A58B by the following calculation method.

- (1) Selection condition
 - (a) Voltage of 4.75VDC or more is identified on the receiving end of the base unit.
- (2) Calculation of the voltage on the receiving end
 - (a) The 5VDC output voltage of the power supply module drops to 4.9V.
 - (b) Resistance value of the cable

AC06B.....0.019 Ω

AC12B.....0.028 Ω

AC30B.....0.052 Ω



The voltage of the receiving end on the 2nd extension base is:

$$\text{Voltage on receiving end} = 4.9 - (V1 + V2) > 4.75$$

where the above condition is satisfied by:

$$4.9 - 4.75 \geq V1 + V2$$

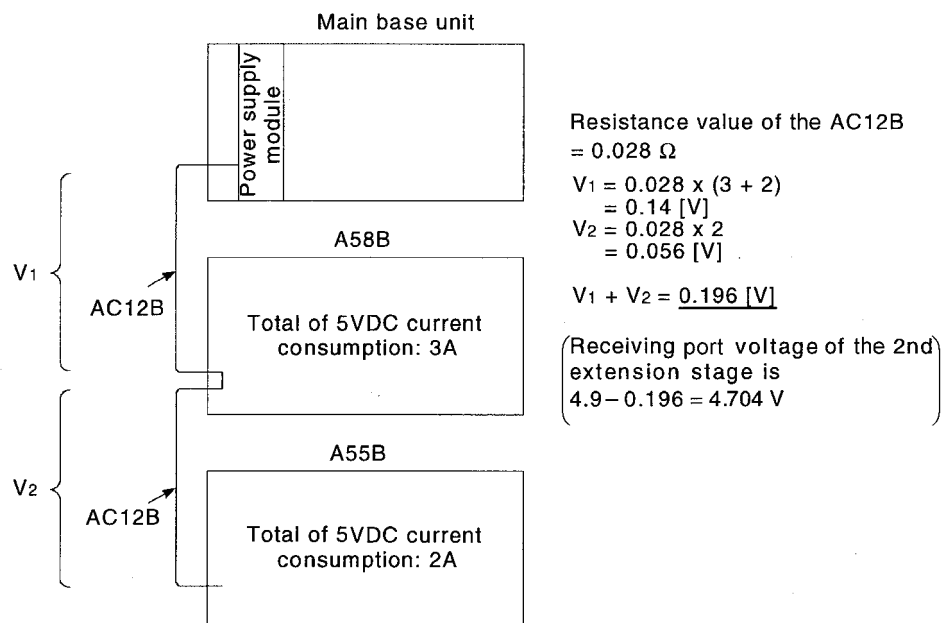
$$0.15 \geq R1(I1 + I2) + R2I2$$

Under the above conditions, the A52B, A55B or A58B can be used as the 2nd extension base.

Therefore, how many A52B, A55B or A58B extension base units can be used and where each of them can be placed is dependant on whether the following condition is satisfied or not.

$$0.15 \geq \text{Total voltage drop up to receiving end}$$

(3) Calculation example



Since the voltage drop is higher than 0.15V, the A55B cannot be used as the 2nd extension base under this condition. In this case, the A55B can be used by changing the cable to AC06B (resistance value = $0.019 \, \Omega$).

$$V_1 = 0.019 \times (3 + 2)$$

$$= 0.095[\text{V}]$$

$$V_2 = 0.019 \times 2$$

$$= 0.038[\text{V}]$$

$$V_1 + V_2 = 0.133[\text{V}]$$

$$\left(\begin{array}{l} \text{Receiving port voltage of the 2nd extension base is:} \\ 4.9 - 0.133 = 4.767\text{V} \end{array} \right)$$

Since the voltage drop is less than 0.15V, the A55B can be used as the 2nd extension base under this condition.

REMARK

When any of the A62B, A65B, A68B is connected between the main base unit and the A52B, A55B, or A58B, calculate a voltage drop by the following.

- Calculate the total resistive value for the extension cables, which are connected from the main base unit to the A52B, A55B, or A58B via the A62B, A65B, or A68B.
- Calculate a 5VDC consumption current for the A52B, A55B, or A58B, which flows thorough the extension cables.

POINT

When using an I/O module or special function module whose internal current consumption is large, mount it on a main base unit or an extension base unit that requires a power supply module (A62B, A65B, A68B).

17.4 Handling Precautions

The handling precautions to be taken from unpacking to mounting a base unit are described below.

The terminal connectors and pin connectors of the base unit are made of resin. Do not drop them or apply heavy impact to them.

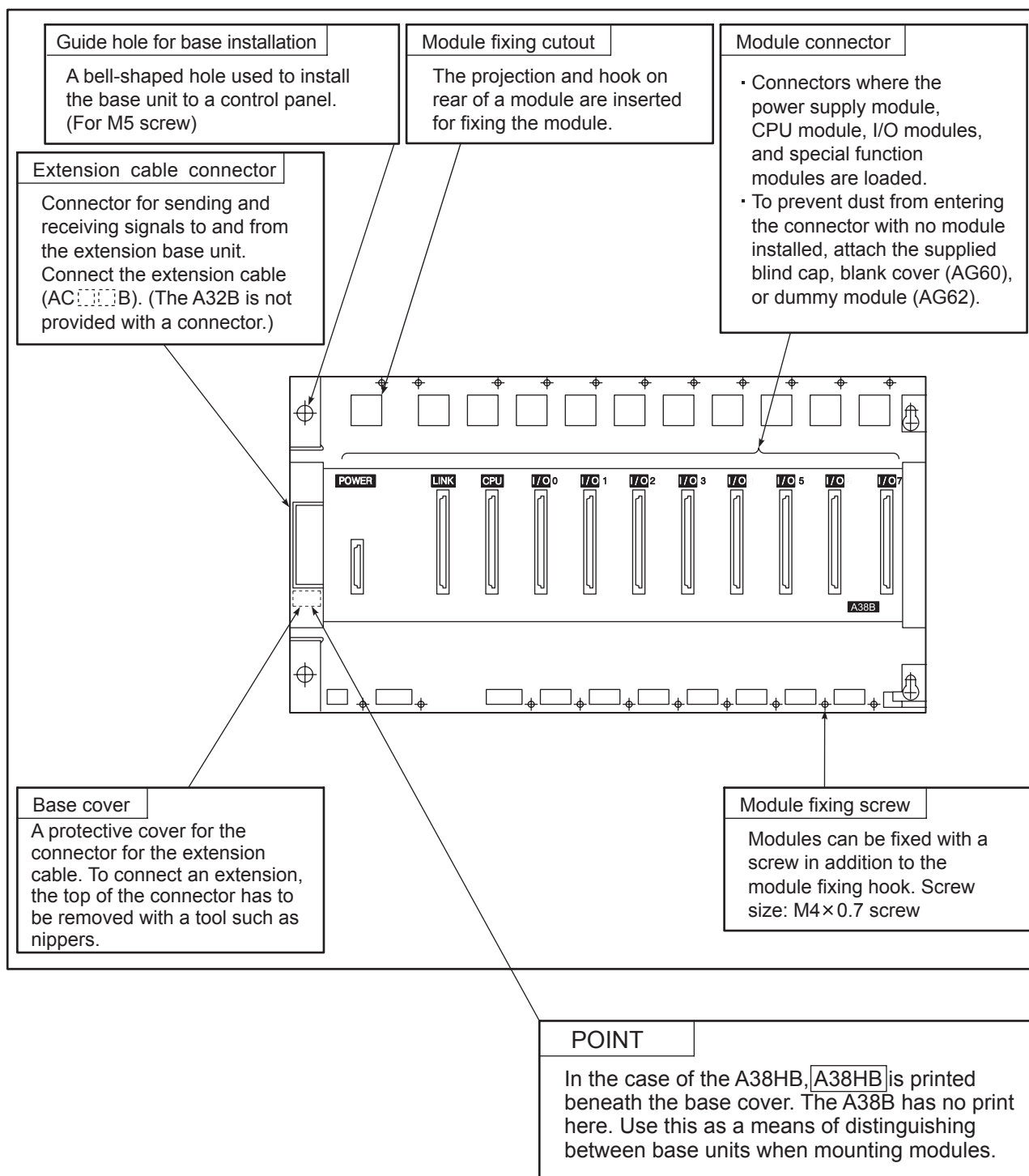
**CAUTION**

- Do not remove the printed-circuit board from the base unit.
Doing so may cause failure, malfunctions, personal injuries and/or a fire.
- Use caution to prevent foreign matter, such as dust or wire chips, from entering the base unit during wiring.
Failure to do so may cause a failure, malfunction or fire.

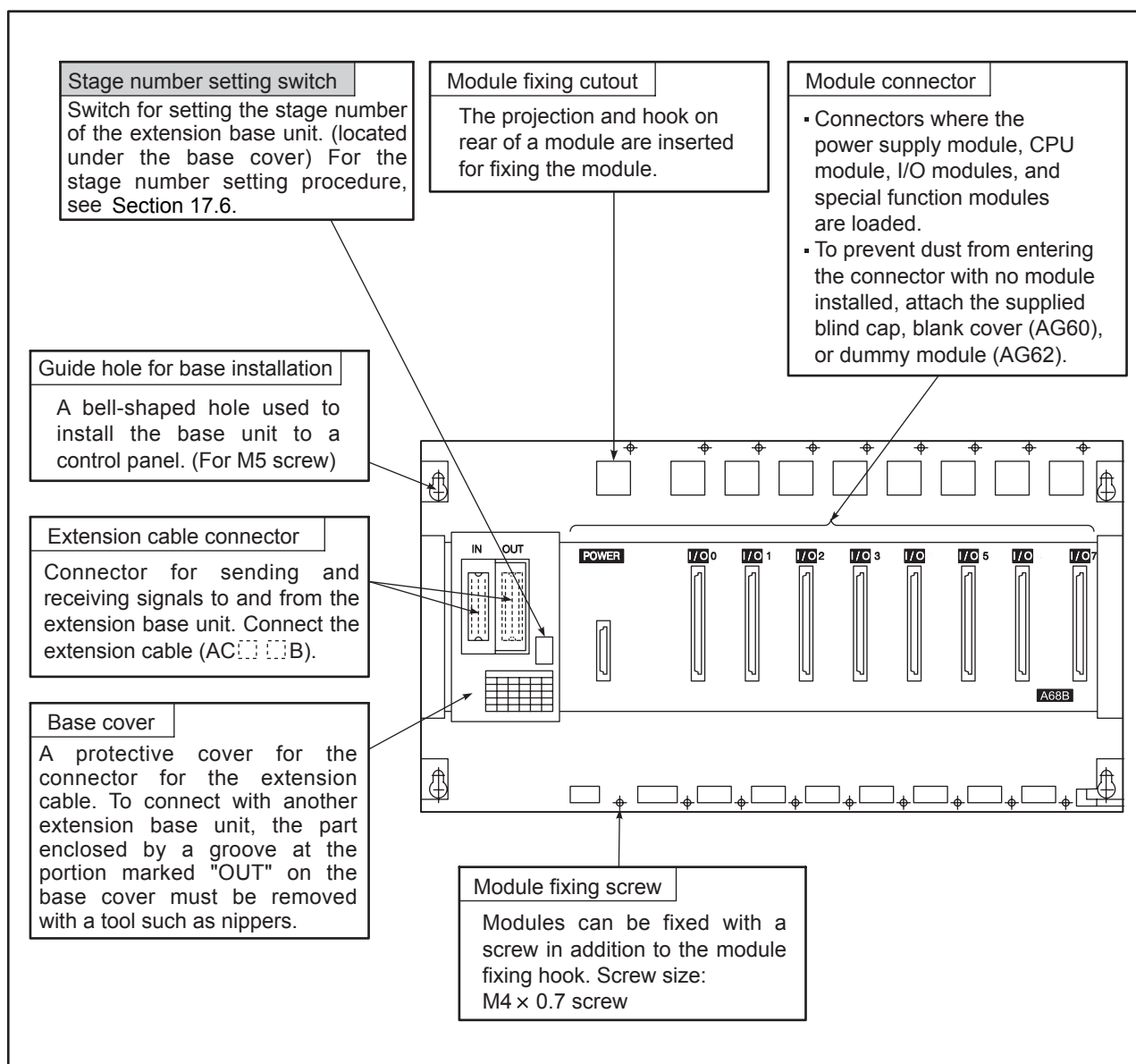
17.5 Part Names

Part names of the base unit are shown here.

(1) Main base units (A32B, A35B, A38B, A38HB, A38HBEU)



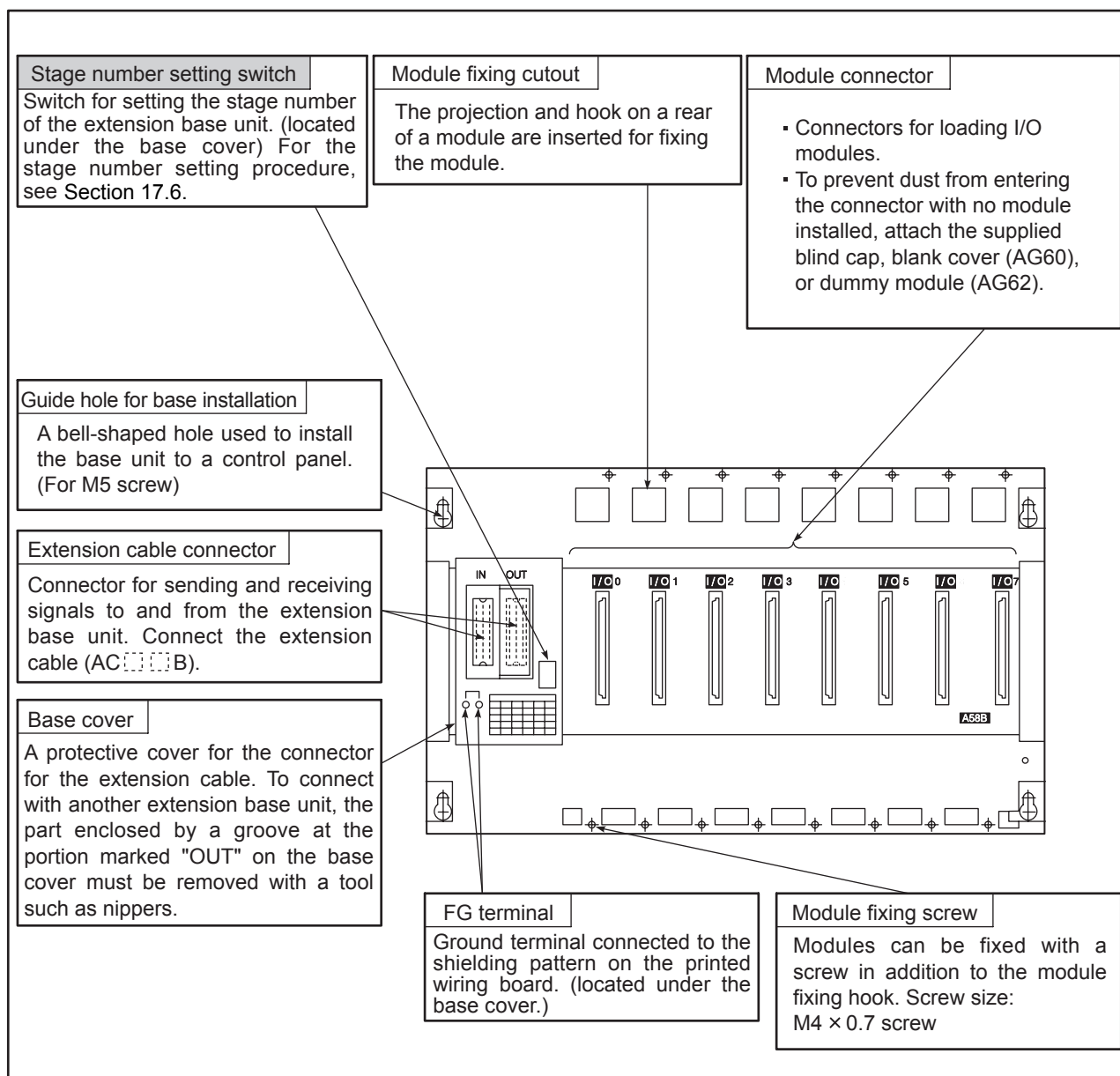
(2) Extension base units (A62B, A65B, A68B)



REMARK

The item indicated by shading  must be set before installing the base unit and starting operation.

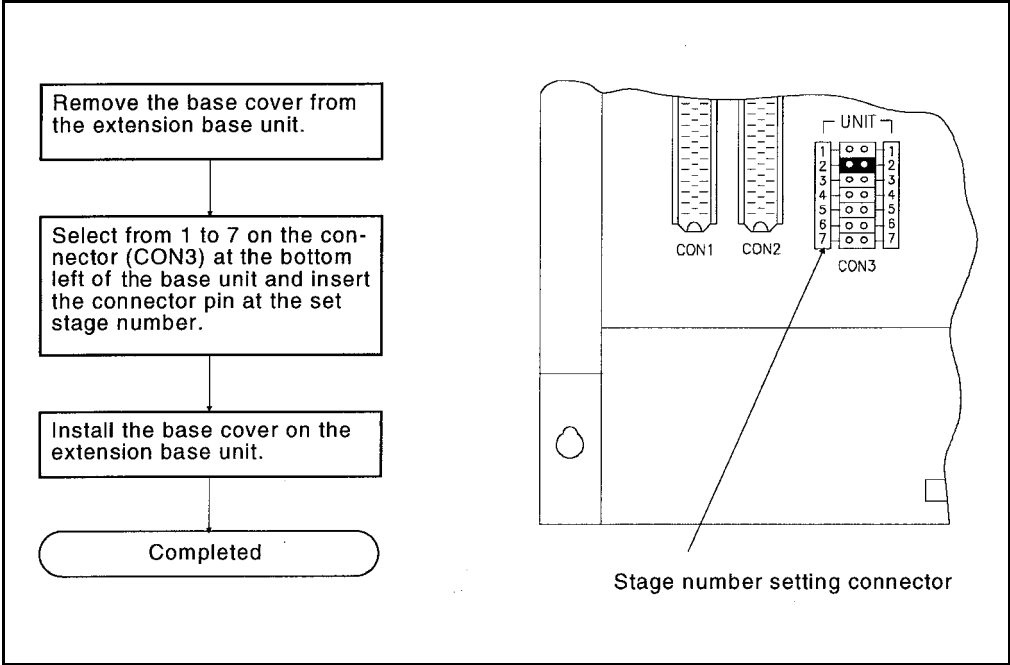
(3) Extension base units (A52B, A55B, A58B)

**REMARK**

The item indicated by shading  must be set before installing the base unit and starting operation.

17.6 Setting of Extension Stage Numbers

This section explains how to set the extension stage number for each of the extension base units used.



Extension base unit stage number setting

	Extension Stage Number Setting						
	1st Stage	2nd Stage	3rd Stage	4th Stage	5th Stage	6th Stage	7th Stage
Setting of the stage number setting connector	 CON3	 CON3	 CON3	 CON3	 CON3	 CON3	 CON3

POINT

With the stage number setting connector (CON3), select one of the 1st to 7th that matches the extension stage number. Multiple settings for the same stage, duplicate stage setting, or no setting is not allowed because it may result in erroneous inputs and/or outputs.

18 MEMORY CARDS AND BATTERIES

This section describes the specifications and handling of the memory cards and batteries that can be used with the QnACPU.

18.1 Memory Card Specifications

The specifications of the memory cards that can be used with QnACPU conform to JEIDA Ver. 4.0.

(1) SRAM type memory cards

Item	Model Name					
	Q1MEM-64S	Q1MEM-128S	Q1MEM-256S	Q1MEM-512S	Q1MEM-1MS	Q1MEM-2MS
SRAM memory capacity before formatting	64k bytes	128k bytes	256k bytes	512k bytes	1M bytes	2M bytes
SRAM memory capacity after formatting	59k bytes	123k bytes	250.5k bytes	506k bytes	1016.5k bytes	2036k bytes
Number of storable files	118	128				256
Insertion/removal limit	5000 times					
External dimensions	85.6mm (3.3inch) × 54mm (2.1inch) × 3.3mm (0.1inch)					
Weight	0.04kg					

(2) SRAM + E²PROM type memory cards

Item		Model Name				
		Q1MEM-64SE	Q1MEM-128SE	Q1MEM-256SE	Q1MEM-512SE	Q1MEM-1MSE
Memory capacity before formatting		32k bytes	64k bytes	128k bytes	256k bytes	512k bytes
	SRAM					
	E ² PROM	32k bytes	64k bytes	128k bytes	256k bytes	512k bytes
Memory capacity after formatting		28.5k bytes	58.5k bytes	122.5k bytes	250k bytes	505.5k bytes
	SRAM					
	E ² PROM	29k bytes	59k bytes	123k bytes	250.5k bytes	506k bytes
Number of storable files		57	117	128		
	SRAM					
	E ² PROM	58	118	128		
Maximum number of writes to E ² PROM		10,000 times				

(2) SRAM + E²PROM type memory cards

Item	Model Name				
	Q1MEM-64SE	Q1MEM-128SE	Q1MEM-256SE	Q1MEM-512SE	Q1MEM-1MSE
Insertion/removal limit	5000 times				
External dimensions	85.6mm (3.3inch) × 54mm (2.1inch) × 3.3mm (0.1inch)				
Weight	0.04kg				

18.2 Handling Memory Cards

(1) Formatting memory cards

All memory cards used with QnACPU must be formatted.

The purchased memory card is not formatted. Use the memory card after formatting with the GPP function.

(a) SRAM+E²PROM type memory card

Format both RAM and ROM.

If installed with only one of them formatted, the QnACPU detects an error (ICM.OPE.ERROR).

For information on how to format SRAM and E²PROM, see the following manual.

- GX Developer Operating Manual
- Type SW□IVD-GPPQ Software package Operating Manual (Online)

(2) Installing the battery in the memory card

The memory card is packaged with a RAM memory backup battery. To use the RAM memory of the memory card, this battery must be installed first.

POINT	
	The battery installed in the CPU module does not back up RAM memories of memory cards. Also, a battery installed in a memory card does not back up the internal RAM of a CPU module.

(3) Switch setting when using a memory card

When using a memory card, turn ON the memory card in/out switch which is close to the connector. If it is set to OFF, the memory card cannot be used.

18.3 Battery Specifications (CPU Module and Memory Card Batteries)

(1) CPU module batteries

Item	Model Name
	A6BAT
Type	Thionyl chloride lithium battery
Initial voltage	3.6VDC
Battery guarantee period	5 years
Total power failure time	Refer to Section 21.3.1
Lithium content	0.48g
Application	Built-in RAM memory backup and power failure compensation
External dimensions	φ 16 × 30mm [0.6 × 1.2 inch]

(2) Memory card batteries

Item	Model Name
	BR2325 or equivalent
Type	BR-type coin cell lithium battery
Initial voltage	3.0VDC
Battery guarantee period	5 years
Total power failure time	Refer to Section 21.3.1
Lithium content	0.05g
Application	Card memory backup and power failure compensation

18.4 Handling Precautions

Handling precautions on memory cards and batteries from unpacking to mounting are listed below.

(1) Memory card

- (a) Do not drop, bend or apply any strong impact to the memory card.
- (b) Do not expose the memory card to water.
- (c) Do not expose the memory card to direct sunlight or leave it near a heat source.
- (d) Be careful to prevent dust from entering the connector.
- (e) Do not store the memory card in high temperature or high humidity areas.
- (f) To protect the memory card from static electricity, always enclose it in a plastic case before transporting or storing.
- (g) Do not touch the terminals of the memory card.



CAUTION

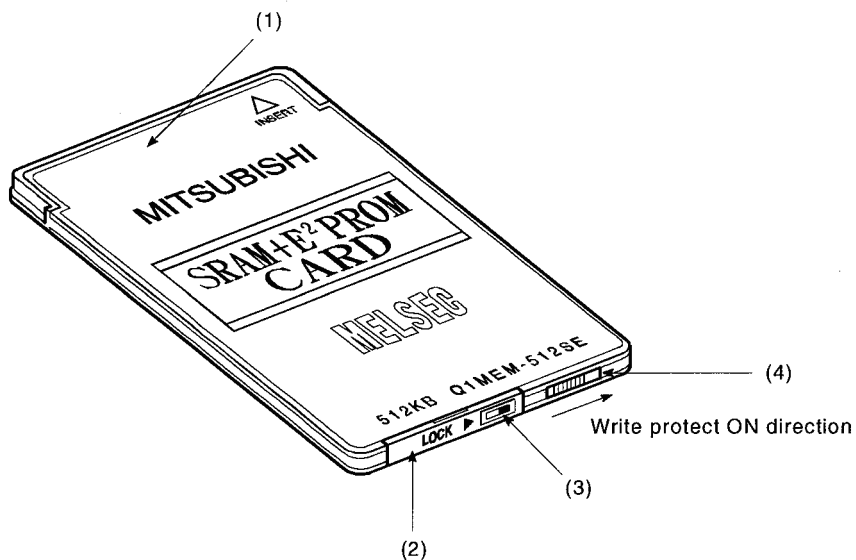
- Insert the memory card and fully press it to the memory card connector. Check for incomplete connection after installing it.
Poor electrical contact may cause malfunctions.

(2) Battery

- (a) Do not short the battery.
- (b) Do not disassemble the battery.
- (c) Do not put it into a fire.
- (d) Do not heat it.
- (e) Do not apply solder to the battery poles.

18.5 Part Names of Memory Card

Part names of the memory card are shown below.

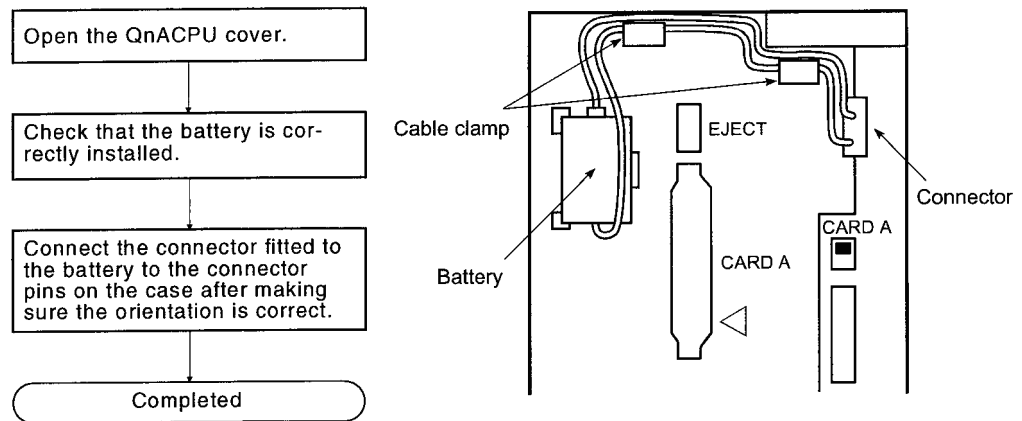


No.	Name	Description	Remark
(1)	Connector	Connects the memory card to the CPU module.	
(2)	Battery holder	Holds a lithium battery that is used to backup RAM data.	*
(3)	Battery holder locking switch	Locks the battery holder to the memory card. (Locked in "LOCK" position.)	
(4)	Write protect switch	Enables or disables writing to the memory. Factory-set to OFF. ON : Data writing disabled OFF : Data writing enabled	*

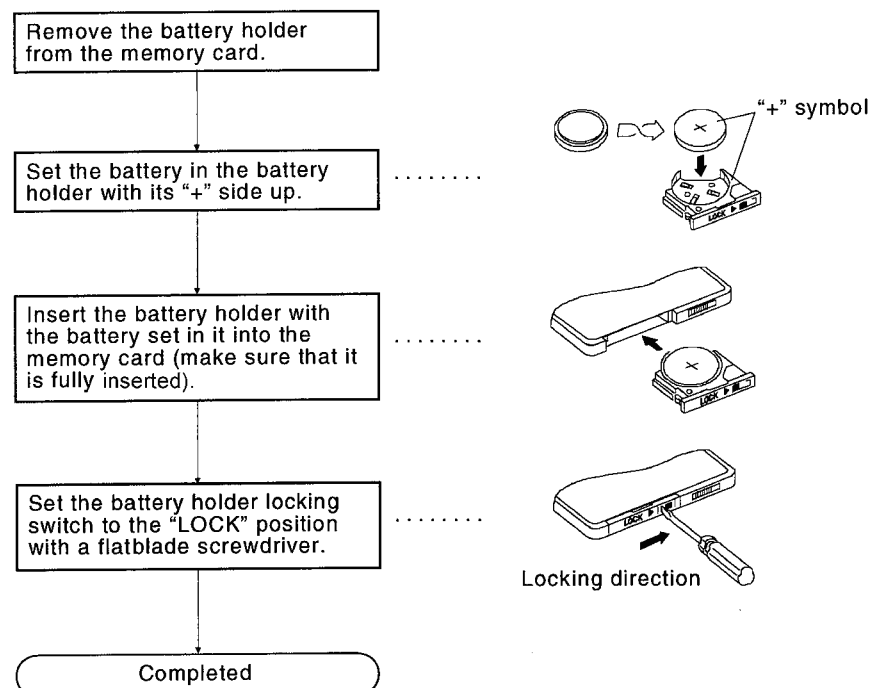
* Must be set before writing a program and starting operation.

18.6 Installing Batteries (CPU Module and Memory Card Batteries)

- (1) Since the CPU module battery is shipped with its battery connector disconnected, connect the connector according to the procedure indicated below.



- (2) Since the memory card battery is removed from the battery holder before shipping, set it in the battery holder before use of the RAM.



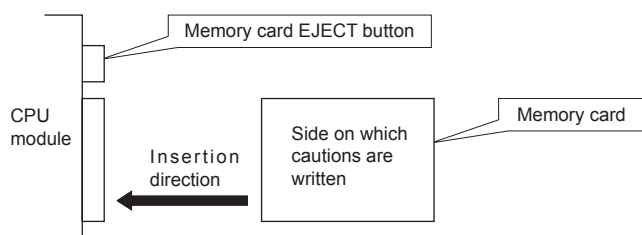
18.7 Installing/Removing a Memory Card

(1) Installing a memory card

When installing a memory card into the CPU module with its power ON, make sure that the orientation of the memory card is correct, then insert it fully until its edge is flush with the face of the EJECT button.

After installing it, set the memory card in/out switch to "ON".

The memory card is operable after the LED on the memory card in/out switch turns ON.

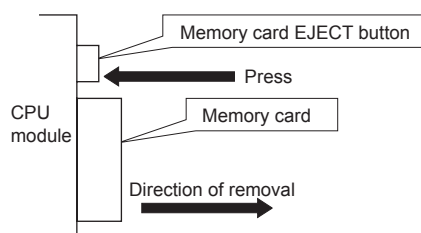
**CAUTION**

- Insert the memory card and fully press it to the memory card connector. After that, check for incomplete insertion. Poor electrical contact may cause malfunctions.

(2) Removing the memory card

Before removing the memory card from the CPU module with its power ON, set the memory card in/out switch to "OFF".

Verify that the LED on the switch has gone OFF. Then, press the memory card EJECT button and remove the memory card.

**POINT**

- (1) When a memory card is installed, the scan time will increase by 10ms at maximum.
The scan time increases only in 1 scan during which the QnACPU performs mount processing.
- (2) If the memory card in/out switch is turned OFF while the system or a program is using the memory card, it may take a while for the LED on the switch to go OFF.
- (3) Installing or removing a memory card with the memory card in/out switch set ON while the power is ON will destroy the contents of the memory card.

- (3) Memory card remove/insert prohibit flag (special relays SM605, SM625)
- Instead of operating the memory card in/out switch, turning ON/OFF special relays SM605 (memory card A) and SM625 (memory card B) can be also used as the card remove/insert prohibit flag. Once removal/insertion is prohibited with the remove/install prohibit flag, it is still disabled even if the memory card in/out switch is set to "ON".
- The relationship between the memory card in/out switch and the memory card remove/insert prohibit flag is shown in the table below.

Memory card remove /insert prohibit flag	Memory card in/out switch	
	ON (Removal/insertion prohibited)	OFF (Removal/insertion permitted)
ON (Removal/insertion prohibited)	Removal/insertion prohibited	Removal/insertion prohibited
OFF (Removal/insertion permitted)	Removal/insertion prohibited	Removal/insertion permitted

19 LOADING AND INSTALLATION

This chapter describes the loading and installation procedures and precautions to obtain the maximum system reliability and performance.

19.1 Fail-Safe Circuit Concept

When the PLC is powered ON or OFF, improper outputs may be generated temporarily depending on the delay time and start-up time differences between the PLC power supply and the external power supply for the control target (especially, DC).

For example, if the external power supply for a DC output module is powered ON and then the PLC is powered ON, the DC output module may generate incorrect outputs temporarily upon the PLC power-ON. To prevent this, it is required to build a circuit by which the PLC is powered on first.

Also, an external power failure or PLC failure may lead to erroneous operation.

In order to eliminate the possibility of a system error and to ensure fail-safe operation, create a circuit (emergency stop circuit, protection circuit, interlock circuit, etc.) outside the PLC for the parts whose faulty operation could cause mechanical damage and/or accidents.

A system design circuit example based on the above is provided later.

**DANGER**

- Create a safety circuit outside the PLC to ensure the whole system will operate safely even if an external power failure or a PLC failure occurs.

Otherwise, incorrect output or malfunction may cause an accident.

- (1) When creating an emergency stop circuit, a protection circuit or an interlock circuit for incompatible actions such as forward/reverse rotation or for damage prevention such as the upper/lower limit setting in positioning, create it outside the PLC.
- (2) When the PLC detects the following error conditions, it stops the operation and turn off all the outputs.
 - The overcurrent or overvoltage protector of the power supply module is activated.
 - The PLC CPU detects an error such as a watchdog timer error by the self-diagnostics function.

In the case of an error undetectable by the PLC CPU, such as an I/O control part error, all the outputs may turn on. In order to make all machines operate safely in such a case, set up a fail-safe circuit or a specific mechanism outside the PLC.

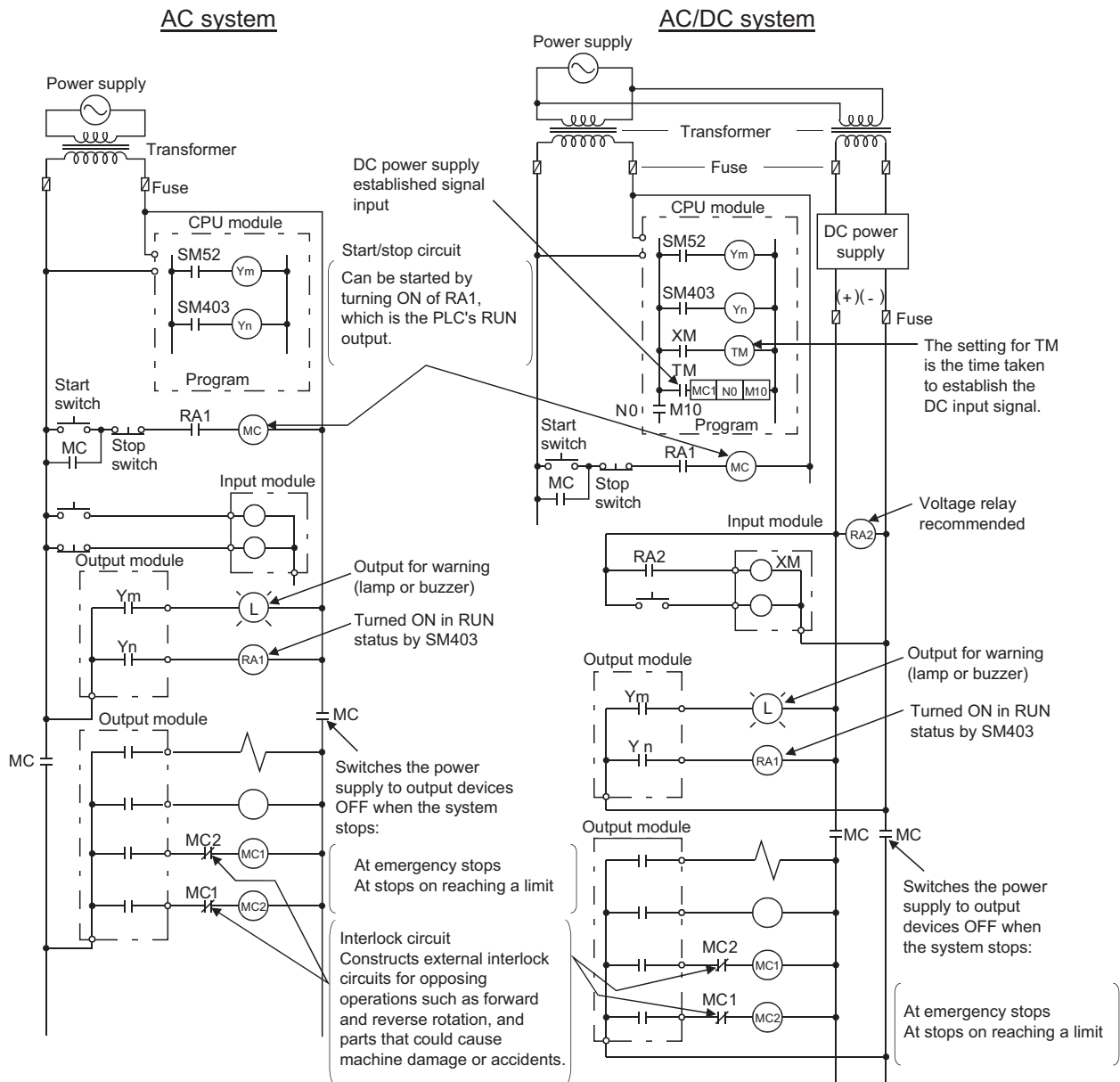
- (3) Depending on the failure of the output module's relay or transistor, the output status may remain ON or OFF incorrectly. For output signals that may lead to a serious accident, create an external monitoring circuit.

- If load current more than the rating or overcurrent due to a short circuit in the load has flowed in the output module for a long time, it may cause a fire and smoke. Provide an external safety device such as a fuse.
- Design a circuit so that the external power will be supplied after power-up of the PLC. Activating the external power supply prior to the PLC may result in an accident due to incorrect output or malfunction.
- For the operation status of each station at a communication error in data link, refer to the respective data link manual.
Otherwise, incorrect output or malfunction may cause an accident.
- When controlling a running PLC (data modification) by connecting a peripheral device to the CPU module or a PC to a special function module, create an interlock circuit on sequence programs so that the whole system functions safely all the time. Also, before performing any other controls (e.g. program modification, operating status change (status control)), read the manual carefully and ensure the safety. In these controls, especially the one from an external device to a PLC in a remote location, some PLC side problem may not be resolved immediately due to failure of data communications.
To prevent this, create an interlock circuit on sequence programs and establish corrective procedures for communication failure between the external device and the PLC CPU.
- When setting up the system, do not allow any empty slot on the base unit. If any slot is left empty, be sure to use a blank cover (AG60) or a dummy module (AG62) for it. When using the extension base unit, A52B, A55B or A58B, attach the included dustproof cover to the module in slot 0. This must be done because some internal parts of the module may be flied during a short circuit test or when an overcurrent or overvoltage is accidentally applied to the external I/O section.

**CAUTION**

- Do not install the control lines or communication cables together with the main circuit or power lines, or bring them close to each other.
Keep a distance of 100mm (3.94inch) or more between them.
Failure to do so may cause malfunctions due to noise.
- If register R outside the allowable range has been read out with the MOV instruction, the file register data will be FFFF_H. Using this as it is may cause malfunctions. Pay attention not to use any out-of-range file register when designing sequence programs. For instruction details, refer to the programming manual.
- When an output module is used to control the lamp load, heater, solenoid valve, etc., a large current (ten times larger than the normal one) may flow at the time that the output status changes from OFF to ON. Take some preventive measures such as replacing the output module with the one of a suitable current rating.

(1) System design circuit example



The procedures used to switch on the power supply are indicated below.

AC system

- 1) Switch the power supply ON.
- 2) Set the CPU module to RUN.
- 3) Switch the start switch ON.
- 4) The output devices are driven in accordance with the program when the magnetic contactor (MC) comes ON.

AC/DC system

- 1) Switch the power supply ON.
- 2) Set the CPU module to RUN.
- 3) Switch RA2 ON when the DC power supply starts.
- 4) Set the timer (TM) to "ON" upon 100% establishment of DC power supply.
(The set value for TM shall be the period from turning "ON" RA2 to 100% establishment of DC power supply. Set 0.5 seconds for it.)
- 5) Switch the start switch ON.
- 6) The output devices are driven in accordance with the program when the magnetic contactor (MC) comes ON.
(When a voltage relay is used for RA2, the timer in the program (TM) is not necessary.)

(2) Fail-safe measures for PLC failure

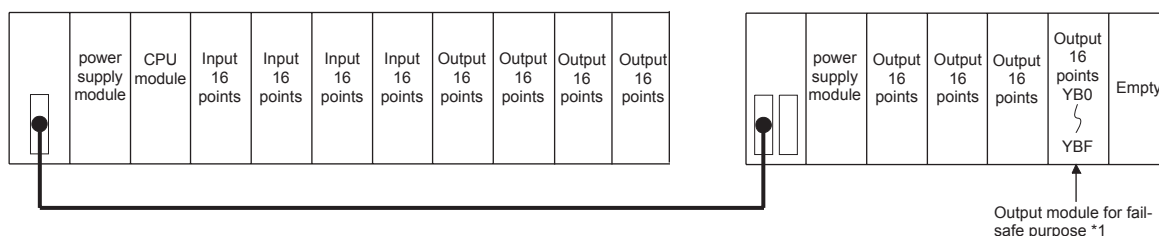
While failure of a CPU module and its memory can be detected by the self-diagnostics function, an error occurred in I/O control area may not be detected by the CPU module.

In such a case, depending on the condition of the failure, all device points could turn ON or OFF resulting in a situation where normal operations of the control target and safety cannot be ensured.

Though Mitsubishi PLCs are manufactured under strict quality control, create a fail-safe circuit outside the PLC to prevent mechanical damage and accidents in the case of a PLC failure occurred due to any cause.

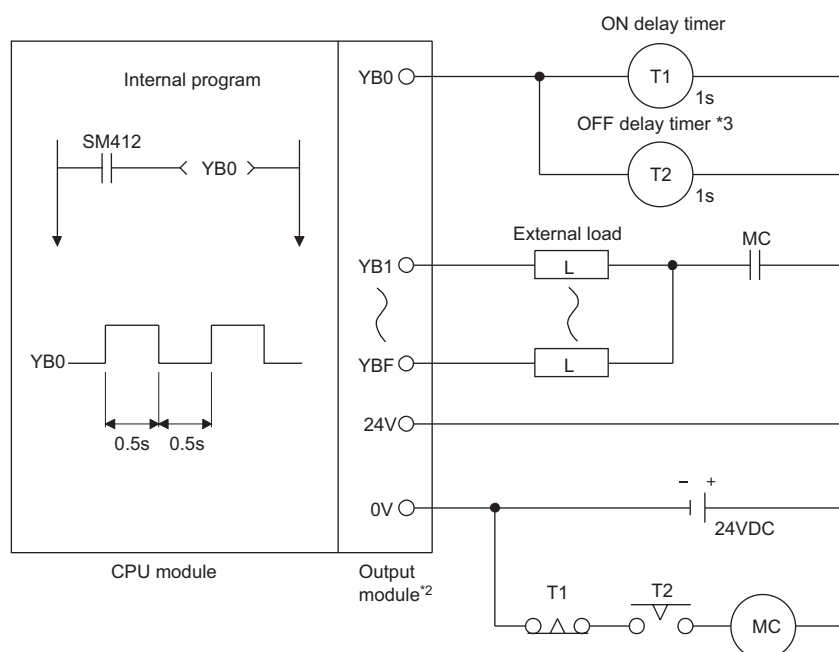
Examples of a system and its fail-safe circuitry are described below:

<System example>



*1 The output module for fail-safe purpose should be mounted on the last slot of the system. (YB0 to YBF in the above system.)

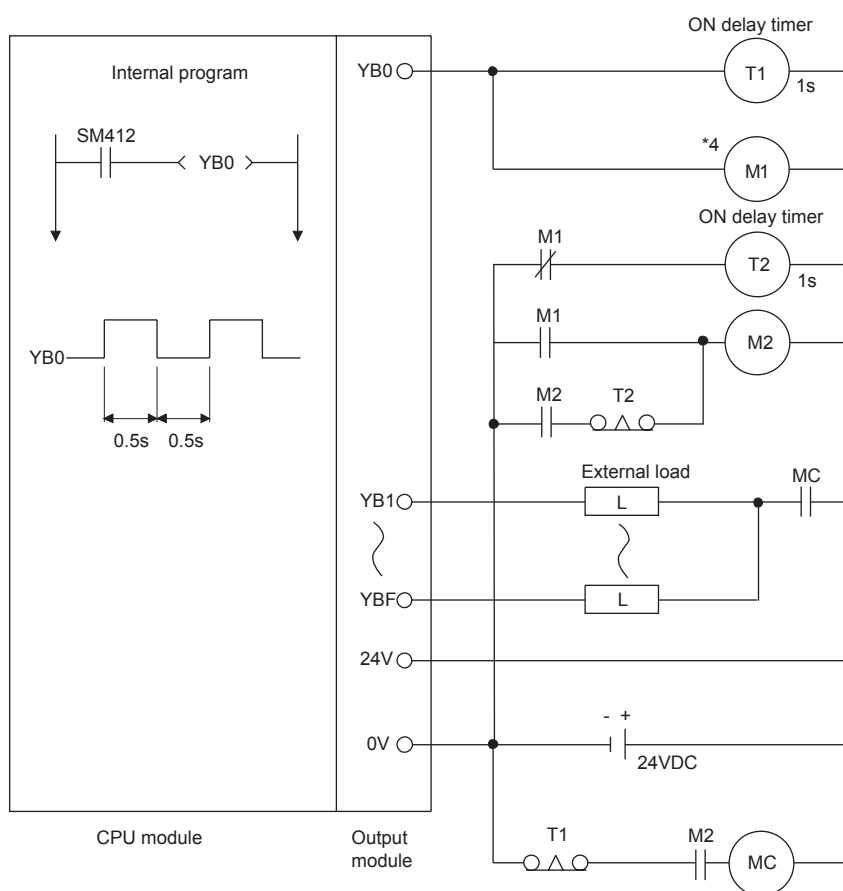
<Fail safe circuit example>



*2 Since YB0 turns ON and OFF alternatively at 0.5 second intervals, use a contactless output module (a transistor is used in the above example).

*3 If an off delay timer (especially miniature timer) is not available, construct a fail-safe circuit using an on delay timer shown on the next page.

When constructing a fail-safe circuit using on delay timers only



*4 Use a solid state relay for the M1 relay.

19.2 Installation Environment

Avoid the following environment when installing a PLC system:

- (1) The ambient temperature may fall outside the range of 0 to 55°C .
- (2) The ambient humidity may fall outside the range of 10 to 90%RH.
- (3) Condensation may occur due to drastic changes in temperature.
- (4) Corrosive gas or flammable gas exists.
- (5) A lot of conductive powdery substance such as dust or iron powder, oil mist, salt, or organic solvent exists.
- (6) A location exposed to direct sunlight.
- (7) Strong electric or magnetic fields may be generated.
- (8) Vibrations and shocks are transmitted directly to the system.

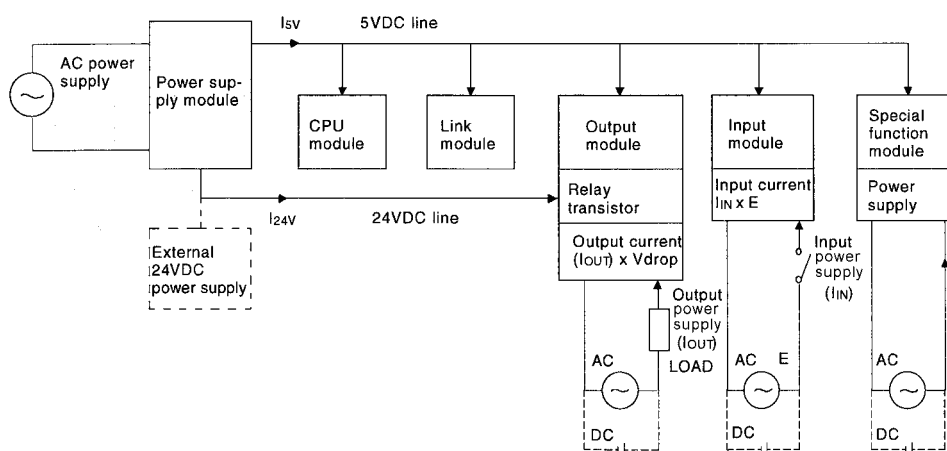
19.3 Calculation of Heat Generated by the PLC

The operating ambient temperature in the panel where the PLC is stored must be kept 55°C or less. For heat dissipation design of the panel, it is necessary to know the average power consumption (heat generation) of the devices and machinery stored inside. In this section, a method to obtain the average power consumption of the PLC system is explained.

Calculate the temperature rise inside the panel from the power consumption.

Average Power Consumption

The power consuming parts of the PLC may be roughly classified into the following blocks:



(1) Power consumption by power supply module

The power conversion efficiency of the power supply module is about 70%, and 30% is consumed as heat generated, thus, 3/7 of the output power is the power consumption. Therefore, the calculation formula is:

$$W_{pw} = \frac{3}{7} \{ (I_{5V} \times 5) + (I_{15V} \times 15) + (I_{24V} \times 24) \} \text{ (W)}$$

I_{5V} : Current consumption of 5VDC logic ladder circuit of each module

I_{15V} : Current consumption of 15VDC external power supply part of special function module

I_{24V} : Average current consumption of 24VDC power supply for output module's internal consumption

(Current consumption equivalent to the points simultaneously ON)

..... Not applicable to a system where 24VDC is supplied externally and a power supply module with no 24VDC output is used.

(2) Total power consumption of 5VDC logic circuits of modules

The 5VDC output circuit power of the power supply module is regarded as the power consumption of each module.

$$W_{5V} = I_{5V} \times 5 \text{ (W)}$$

- (3) Total 24VDC average power consumption of the output module (power consumption equivalent to the points simultaneously ON)

The average 24VDC output circuit power of the power supply module is regarded as the total power consumption of each module.

$$W_{24V} = I_{24V} \times 24 \text{ (W)}$$

- (4) Average power consumption due to output voltage drop of the output modules (power consumption equivalent to the points simultaneously ON)

$$W_{OUT} = I_{OUT} \times V_{drop} \times \text{Output points} \times \text{that are simultaneously ON (W)}$$

I_{OUT} : Output current (actual operating current) (A)

V_{drop} : Voltage dropped across each output load (V)

- (5) Average input power consumption of the input modules (power consumption equivalent to the points simultaneously ON)

$$W_{IN} = I_{IN} \times E \times \text{Input points} \times \text{that are simultaneously ON (W)}$$

I_{IN} : Input current (effective value for AC) (A)

E : Input voltage (actual operating voltage) (V)

- (6) Power consumption of the external power supply part of the special function module

$$W_S = I_{+15V} \times 15 + I_{-15V} \times 15 + I_{24V} \times 24 \text{ (W)}$$

The total of the power consumption values obtained for each block is power consumption of the entire PLC system.

$$W = W_{pw} + W_{5V} + W_{24V} + W_{OUT} + W_{IN} + W_S \text{ (W)}$$

Using this value (W), calculate the amount of heat generation and temperature rise inside the panel.

The calculation formula to obtain the temperature rise inside a panel is shown as:

$$T = \frac{W}{UA} \text{ [}^\circ\text{C]}$$

W : Power consumption of the entire PLC system (the value obtained above)

A : Surface area inside the panel (m^2)

U : When temperature inside panel is kept constant by a fan, etc. 6

When air inside panel is not circulated 4

POINT	
	If the temperature inside the panel can exceed the specified range, it is recommended to install a heat exchanger to the panel to lower the inside temperature. If a ordinary ventilation fan is used, it sucks dust together with the outside air and it may affect the performance of the PLC.

19.4 Installing the Base Units

Precautions on installation of the main base unit and extension base unit are described here.

19.4.1 Installation precautions

Precautions for installing a PLC to a panel, etc. are explained below.

- (1) To allow sufficient air flow and to make module replacement easy, provide a distance of at least 80mm (3.15inch) between the module top and any other structure or part.
- (2) Do not install the PLC vertically or horizontally, because it may affect the ventilation.
- (3) If the base unit is installed to the surface which is not flat or is distorted, an excessive force is applied to the printed-circuit board and it may cause a fault. Be sure to install it to a flat surface.
- (4) Avoid sharing the same panel with any source of vibration such as a large-sized magnetic contactor or no-fuse breaker, and install to a separate panel or away from such devices.
- (5) Provide wiring ducts as necessary.
However, when the clearance from the top or bottom of the PLC is less than that in Fig. 19.1 and Fig. 19.2, pay attention to the following:
 - (a) When installing a duct over the PLC, the height of the duct must be 50mm (1.97inch) or less to allow sufficient air flow.
Place the PLC in the proper position so that the user can press the hook on the top of the module.
Module replacement is not possible if the hook cannot be pressed.
 - (b) When placing a duct under the PLC, take into account the use of optical fiber cables or coaxial cables as well as the minimum bending radius of the cables.
- (6) If any device is placed in front of the PLC (when the PLC is installed on the back of the door), a distance of at least 100mm (3.94inch) must be provided to avoid the influence of radiated noise and heat.
Also, place the base unit at least 50mm (1.97inch) away from any other equipment on the right or left.

19.4.2 Installation

Installation location of the main base unit and the extension base unit is shown below.

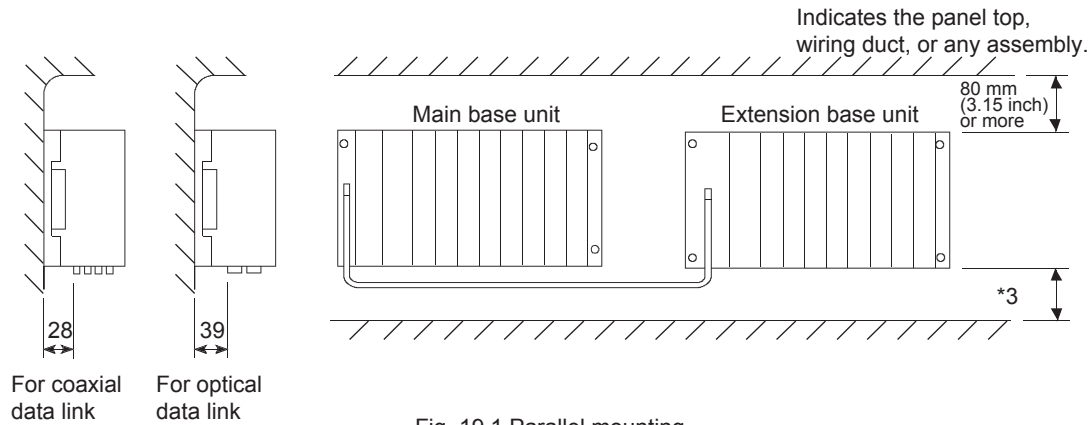


Fig. 19.1 Parallel mounting

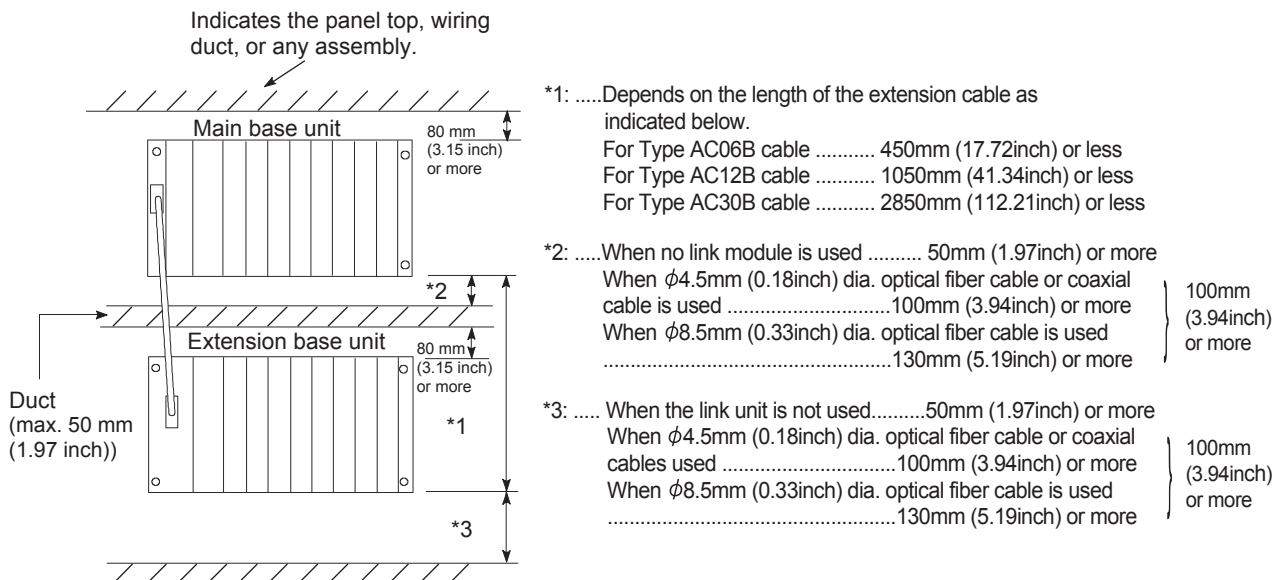


Fig. 19.2 Serial mounting

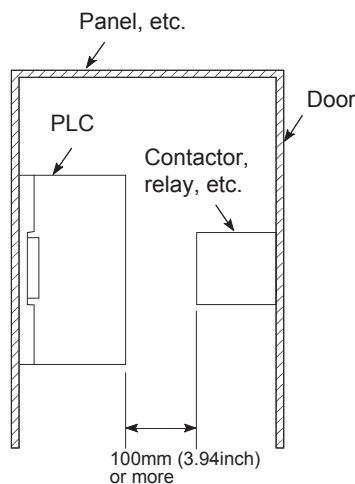


Fig. 19.3 Minimum front clearance with equipment

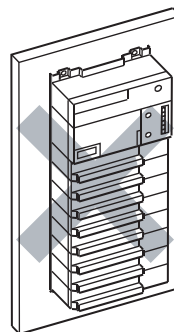


Fig. 19.4 Vertical mounting (Not allowed)

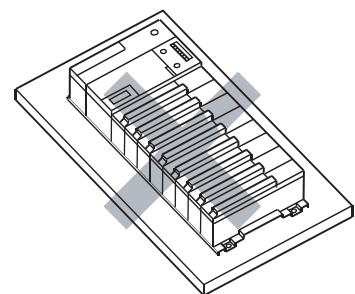


Fig. 19.5 Horizontal mounting (Not allowed)

19.5 Installation and Removal of Modules

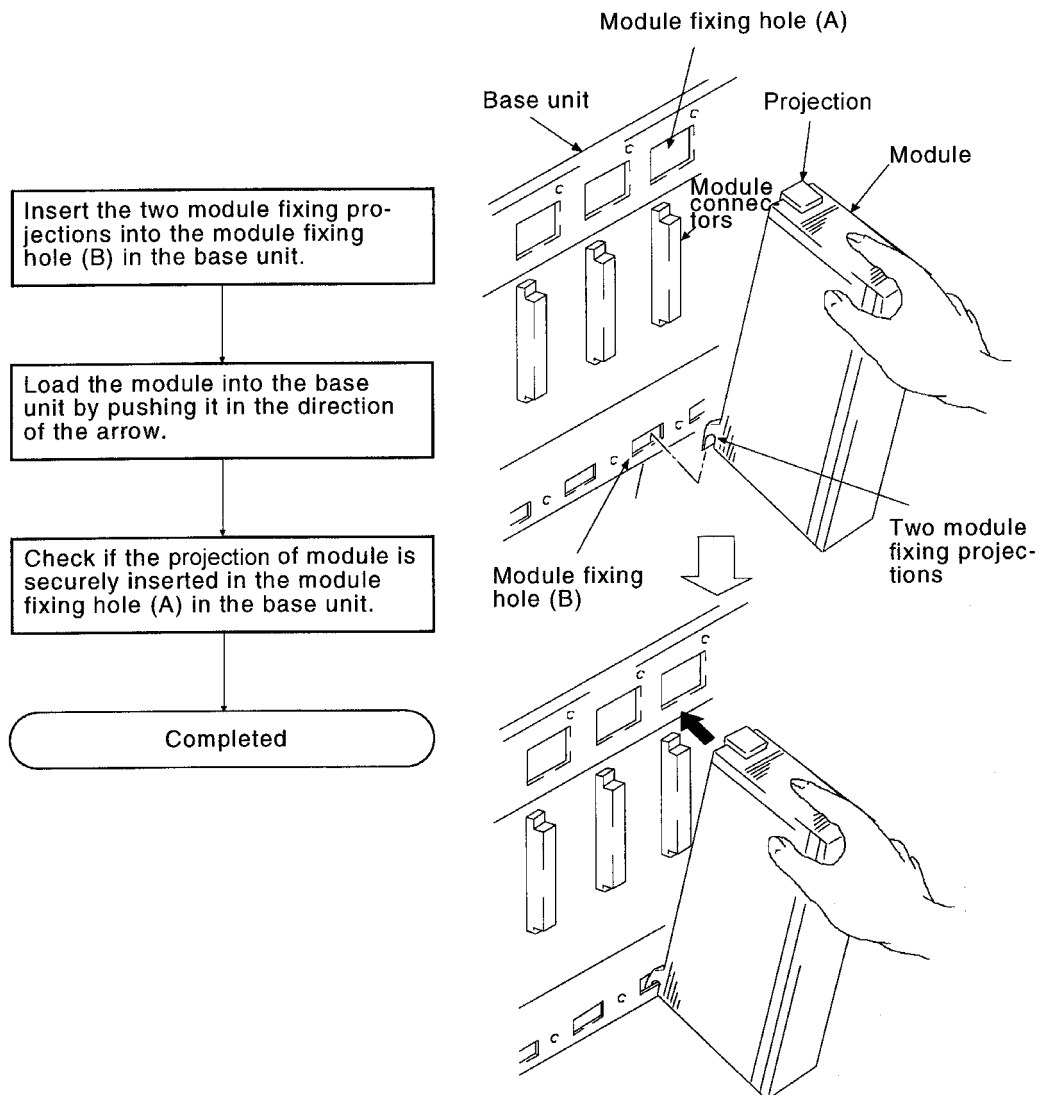
This section explains how to install or remove the power supply module, CPU module, I/O module and special function module, etc. to or from the base unit.

**DANGER**

- Be sure to shut off all phases of the external power supply used by the system before mounting or removing the module.
Failure to do so may damage the module.
- Before energizing and operating the system after installation or wiring, be sure to attach the terminal cover supplied with the product.
Failure to do so may cause an electric shock.

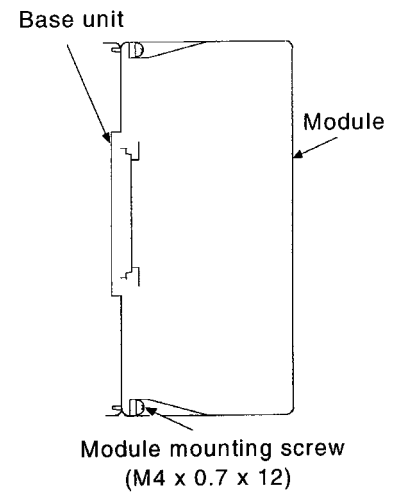
(1) Installing a module

The procedure for mounting a module is described below.



POINT

For use in an environment with particularly large vibrations and/or shocks, fix the module to the base with screws. The applicable screw size is M4(0.16) × 0.7(0.03) × 12mm (0.47 in). Refer to the figure on the right.

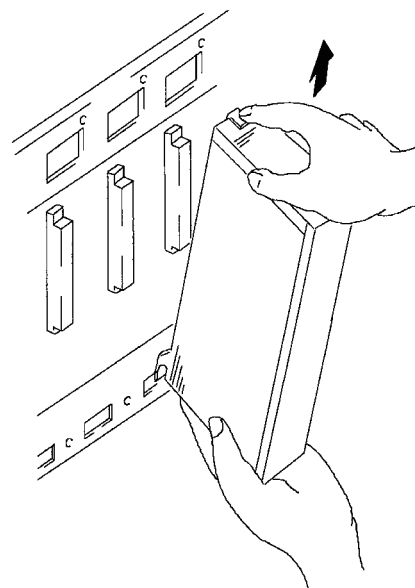
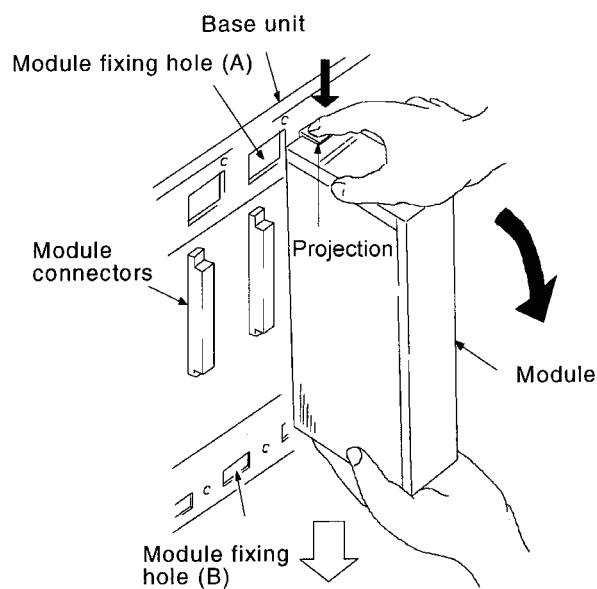
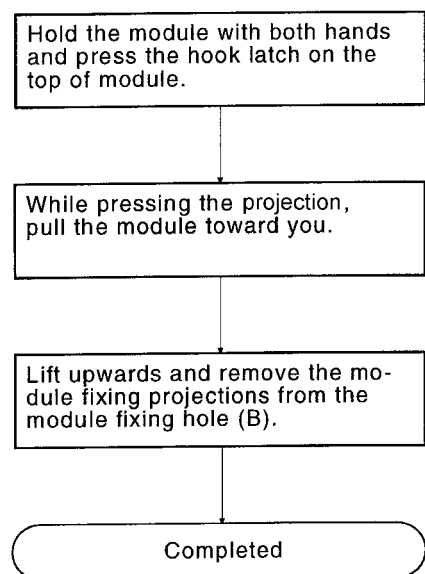


CAUTION

- Insert the module fixing projection into the fixing hole in the base unit to mount the module.
Incorrect installation could result in malfunction, failure, or a drop of the module.
For use in an environment of frequent vibrations, secure the module with screws.
Tighten the screws within the specified torque range.
If the screw is too loose, it may cause a drop of the module, a short circuit or malfunctions.
If too tight, it may cause damage to the screws and/or module, resulting in an accidental drop of the module, short circuit or malfunctions.

(2) Removing a module

The procedure for removing a module is explained here.

**POINT**

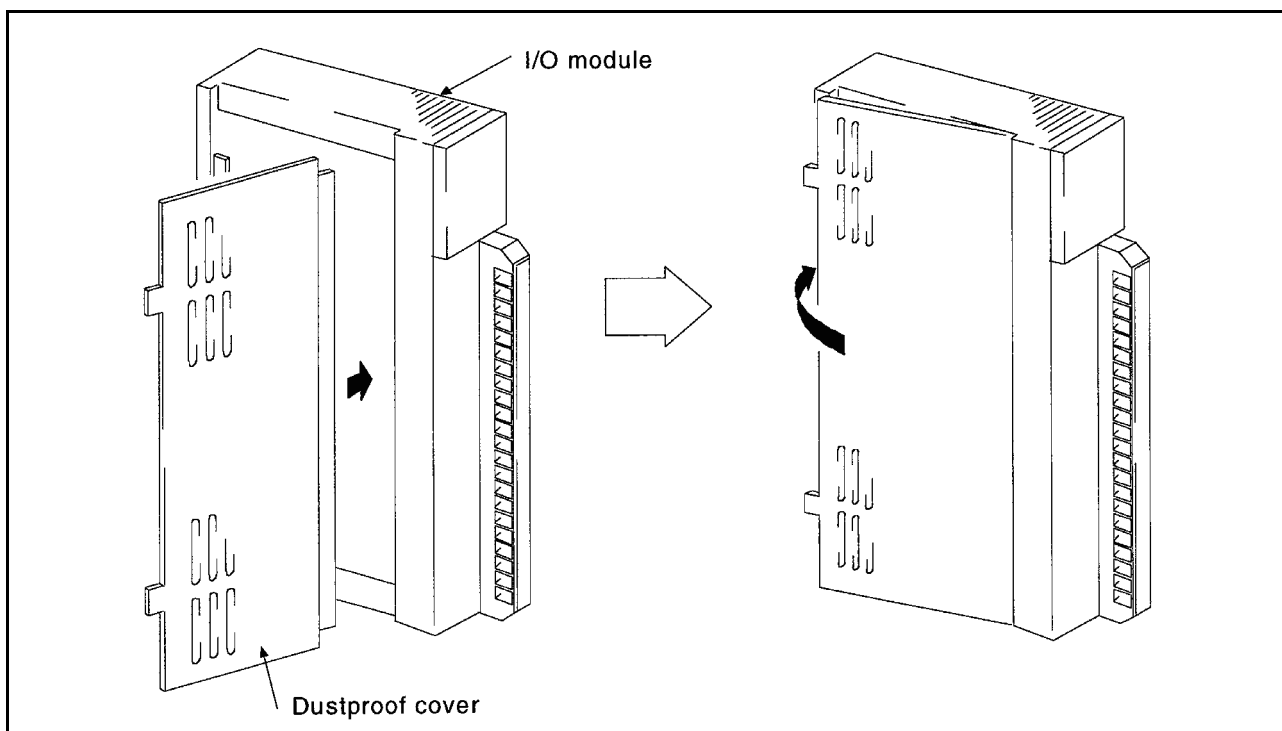
Always disengage the hook from the module fixing hole (A) and then remove the module fixing projection from the module fixing hole (B). An attempt to remove the module forcibly may damage the hook or module fixing projection.

19.6 Installation and Removal of the Dustproof Cover

When using the A52B, A55B or A58B, attach the dustproof cover supplied with the extension base unit to the I/O module on the left end. If no dustproof cover is attached, foreign matter will enter the I/O module, causing a failure.

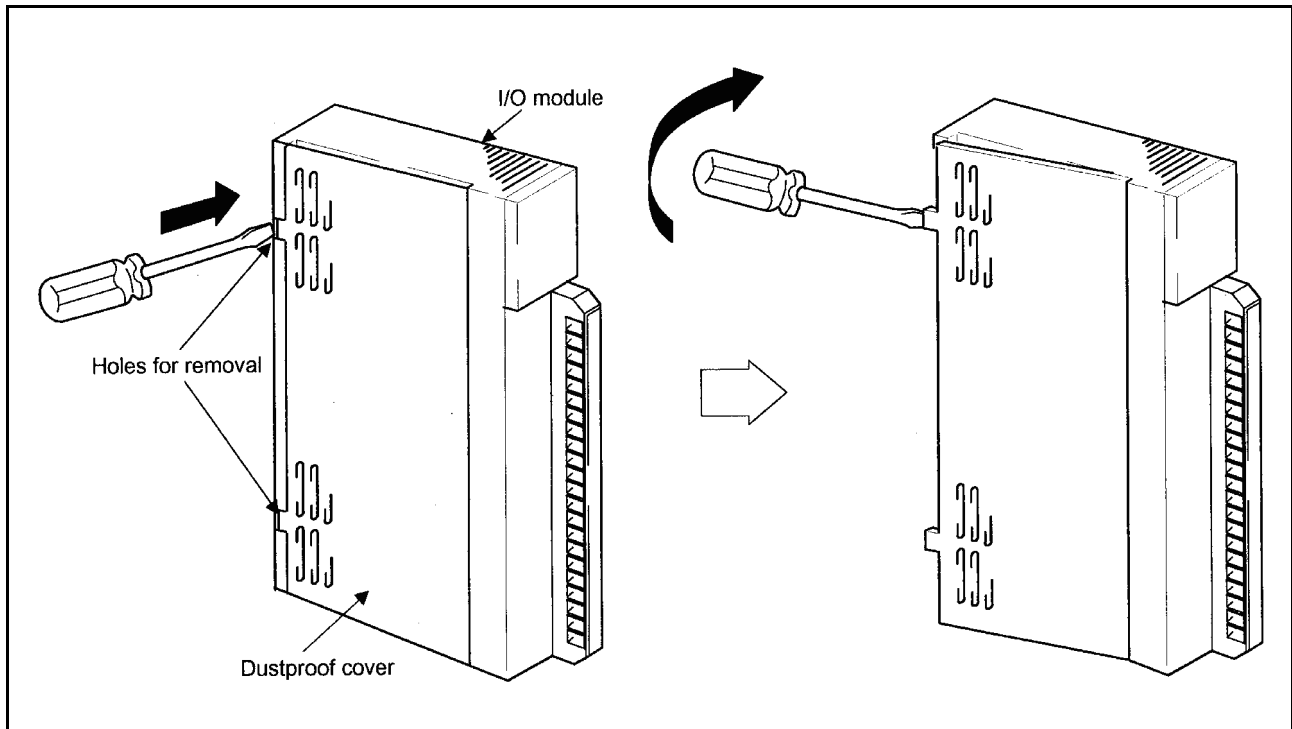
Procedures for installing and removing the dustproof cover are described below.

(1) Installation



Insert the dustproof cover into the connector or terminal-side groove of the I/O module first as shown in the figure, and then push the dustproof cover.

(2) Removal



To remove the dustproof cover from the I/O module, insert the tip of a flat-head screwdriver into the hole as shown in the figure, then pry the tab of the cover out from the hole using the screwdriver.

19.7 Wiring

This section describes details of the wiring that used in systems.

19.7.1 Wiring instructions

Instructions for wiring of power cables or I/O cables are given in this section.

**DANGER**

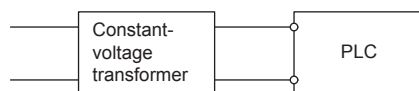
- Be sure to shut off all the phases of the external power supply used by the system before wiring.
Failure to do so may result in an electric shock or damage of the product.
- Before energizing and operating the system after wiring, be sure to attach the terminal cover supplied with the product.
Failure to do so may cause an electric shock.

**CAUTION**

- Ground the FG and LG terminals correctly.
Failure to do so may cause an electric shock or malfunctions.
- Wire the module correctly after confirming the rated voltage and terminal layout.
Connecting a power supply of a different voltage rating or incorrect wiring may cause a fire or failure.
- Do not connect multiple power supply modules to one module in parallel.
The power supply modules may be heated, resulting in a fire or failure.
- Press, crimp or properly solder the connector for external connection with the specified tool.
Incomplete connection may cause a short circuit, fire or malfunctions.
- Tighten terminal screws within the specified torque range.
If the screw is too loose, it may cause a short circuit, fire or malfunctions
If too tight, it may damage the screw and/or the module, resulting in a drop of the module , a short circuit or malfunctions.
- Carefully prevent foreign matter such as dust or wire chips from entering the module.
Failure to do so may cause a fire, failure or malfunctions.
- Install our PLC in a control panel for use.
Wire the main power supply to the power supply module installed in a control panel through a distribution terminal block.
Furthermore, the wiring and replacement of a power supply module have to be performed by a maintenance worker who acquainted with shock protection.
(For the wiring methods, refer to Section 19.7.)

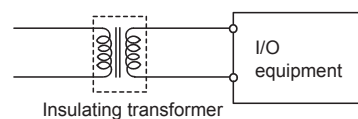
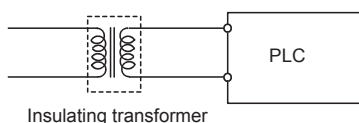
(1) Wiring the power supply

- (a) When voltage fluctuates outside the specified value range, connect a constant-voltage transformer.



- (b) Use a power supply which generates minimal noise between wires and between the PLC and ground.

If excessive noise is generated, connect an isolating transformer.



- (c) When using a power transformer or an isolating transformer to reduce the voltage from 200VAC to 100VAC, its capacity must be equal to or greater than the corresponding value shown in the following table.

Power Supply Module	Transformer Capacity
A61P, A61PN	160VA × n
A61PEU	130VA × n
A62P, A62PEU	155VA × n
A65P	110VA × n
A66P	95VA × n

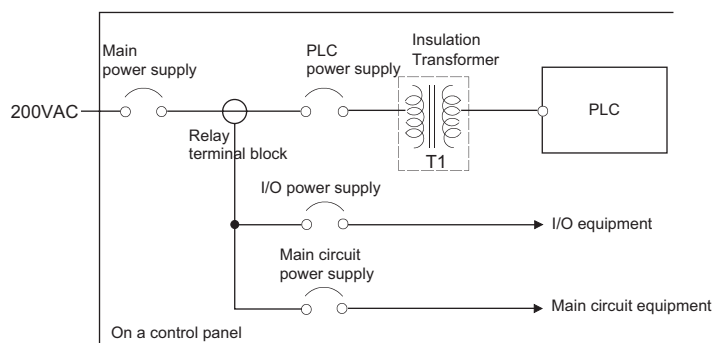
n: Stands for the number of power supply modules.

- (d) Separate the PLC's power supply line from the lines for I/O devices and power devices as shown below.

When there is much noise, connect an isolating transformer.

- (e) Taking rated current or inrush current into consideration when wiring the power supply, be sure to connect a breaker or an external fuse that have proper blown and detection.

When using a single PLC, a 10A breaker or an external fuse are recommended for wiring protection.



REMARK

As a safety measure, provide a switch for turning on/off the power to each module and equipment to allow "online I/O module replacement".

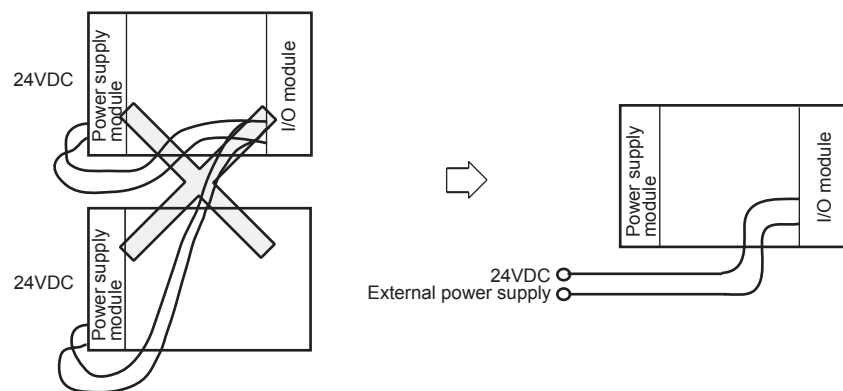
- (f) Precautions for using 24VDC output of the A62P, A62PEU, A65P or A66P power supply module



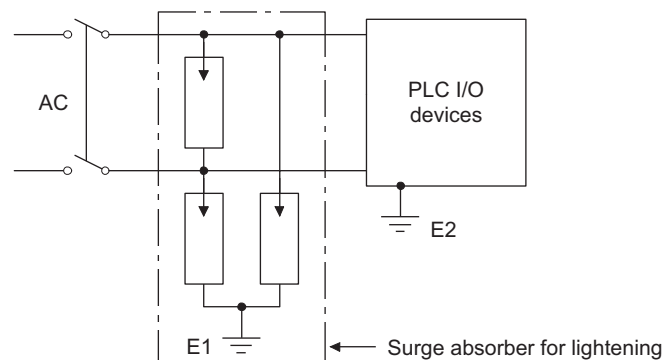
CAUTION

- Do not connect multiple power supply modules to one module in parallel. The power supply modules may be heated, resulting in a fire or failure.

If the 24VDC output power from a single power supply module is insufficient, supply it from the external 24VDC power supply.



- (g) Twist the 100VAC, 200VAC or 24VDC wires as tightly as possible, and use the minimum length to make connection between modules.
Also, use a thick wire (max. 2 mm²) to minimize voltage drop.
- (h) Do not install 100VAC and 24VDC wires together with main circuit wires (high voltage and large current) or I/O signal lines (including common line). Provide a distance of 100mm (3.94inch) or more between them if possible.
- (i) As a measure against lightning surges, connect a lightning surge absorber as shown below.



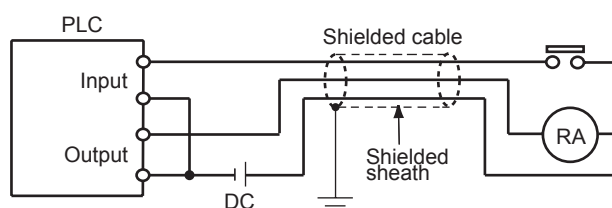
POINT
(1) Ground the lightning surge absorber (E1) and the PLC (E2) separately from each other. (2) Select a lightning surge absorber whose voltage does not exceed the maximum allowable circuit voltage even when line voltage reaches the maximum.

(2) Wiring I/O equipment

**CAUTION**

- Do not install the control lines or communication cables together with the main circuit or power lines, or bring them close to each other. Keep a distance of 100mm (3.94inch) or more between them. Failure to do so may cause malfunctions due to noise.

- (a) The applicable wire size for a terminal block connector is 0.75 to 2mm². It is recommended to use wire of 0.75mm² for easy use.
- (b) Run the input line and output line away from each other.
- (c) Separate the I/O signal lines (including common line) at least 100mm (3.94inch) away from the main circuit line carrying high voltage and large current.
- (d) If it is not possible, use a batch shielding cable and ground it on the PLC side. However, ground it on the opposite side in some cases.



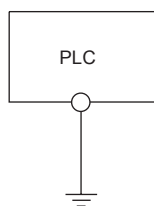
- (e) When ducts are used for wiring, securely ground them.
- (f) Separate the 24VDC I/O cables from the 100VAC and 200VAC cables.
- (g) In a long distance wiring of 200m (656.2ft.) or longer, leak current due to capacitance may cause failure.
- (h) As protective measures against lightning surges, separate the AC wiring from the DC wiring and connect a lightning surge absorber as shown in (1) (i). Failure to do so increases the risk of I/O equipment failure due to lightning.

(3) Grounding

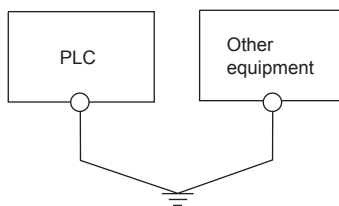
**CAUTION**

- Always ground the FG and LG terminals to the protective ground conductor. Failure to do so may cause an electric shock or malfunctions.

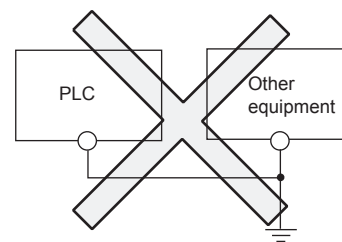
- Carry out the independent grounding if possible.
- If independent grounding is impossible, carry out the shared grounding (2) as shown below.



(1) Independent grounding ... Best



(2) Joint grounding ... Good

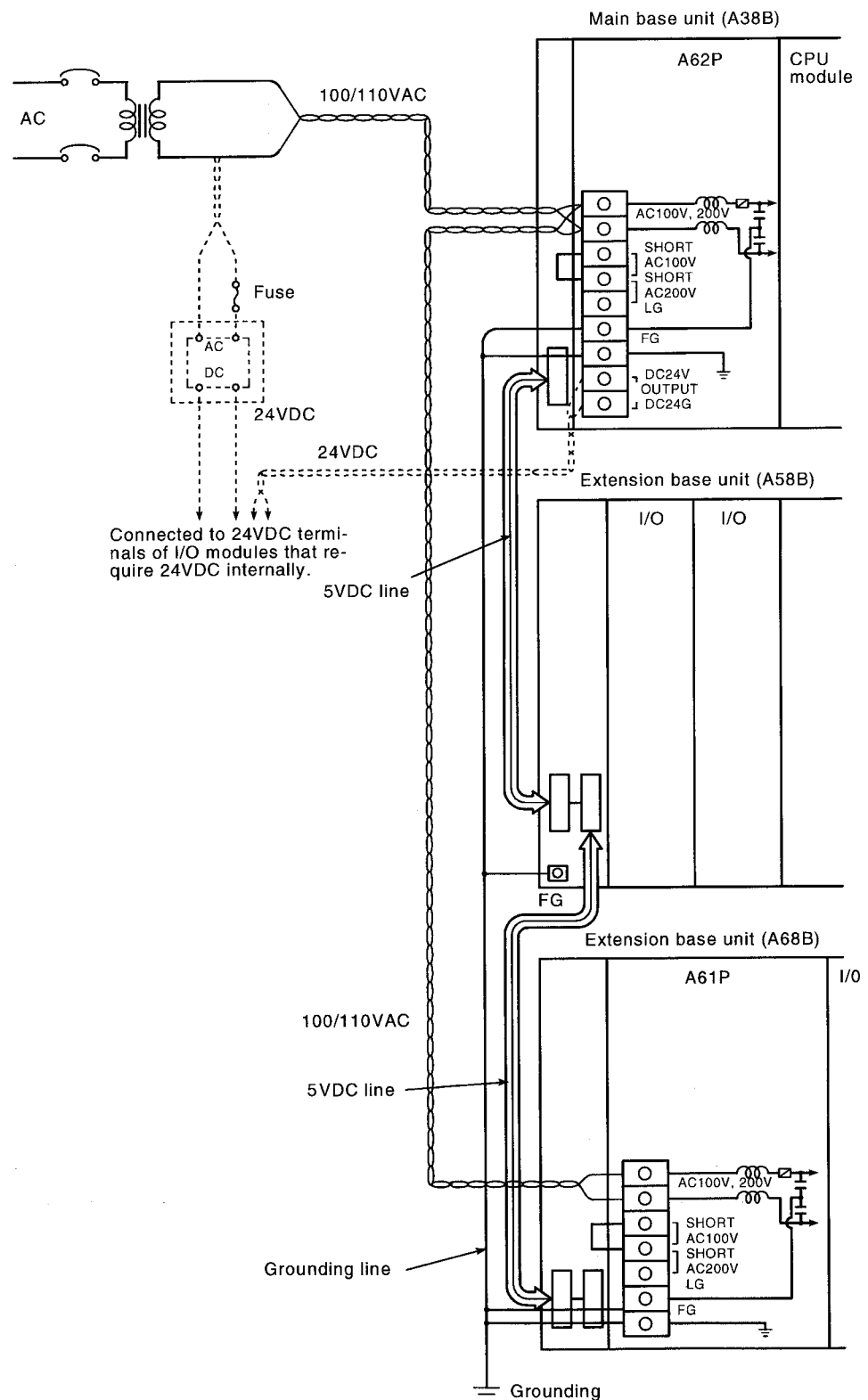


(3) Joint grounding ... Not allowed

- Use the cable of 2mm^2 or more for grounding.
Set the grounding point closer to the PLC to make the grounding cable short as possible.
- If any malfunction occurs due to grounding, disconnect either or both of the LG and FG terminals of the base unit from the ground.

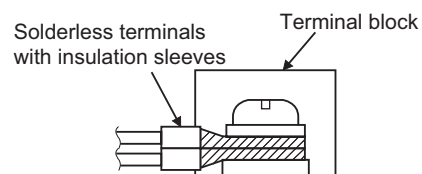
19.7.2 Wiring to module terminals

This section provides an example for wiring power cables and ground wires to the main and extension bases.



POINT

- (1) Use the thickest possible (max. 2 mm² (14 AWG)) wires for the 100/200 VAC and 24 VDC power cables. Be sure to twist these wires starting at the connection terminals. For wiring a terminal block, be sure to use a solderless terminal. To prevent short-circuit due to loosening screws, use the solderless terminals with insulation sleeves of 0.8 mm (0.03 inch) or less thick. The number of the solderless terminals to be connected for one terminal block are limited to 2



- (2) When connection is made between the LG and FG terminals, be sure to ground the wire.
When it is not grounded with LG and FG terminals connected, it will be susceptible to noise.
Note that each LG terminal has half the potential of the input voltage; you might get an electric shock if you touch it.

19.8 Precautions When Connecting Uninterruptible Power Supply Module (UPS)

When connecting a PLC system to an uninterruptible power supply (UPS), pay attention to the following.

Use an on-line or line interactive UPS (with voltage distortion of 5% or less.)

When using an off-line system UPS, use the F series UPS manufactured by Mitsubishi Electric (serial No. P or later). Example: FW-F10-03.K/0.5K

Do not use any off-line system UPS other than the F series.

20 EMC AND LOW VOLTAGE DIRECTIVES

The products sold in the European countries have been required by law to comply with the EMC and Low Voltage Directives of the EU Directives since 1996 and 1997, respectively. The manufacturers must confirm by self-declaration that their products meet the requirements of these directives, and put the CE mark on the products.

20.1 Requirements for Compliance with EMC Directives

The EMC Directives specifies emission and immunity criteria and requires the products to meet both of them, i.e., not to emit excessive electromagnetic interference (emission): to be immune to electromagnetic interference outside (immunity). Guidelines for complying the machinery including MELSEC-QnA series PLC with the EMC Directives are provided in Section 20.1.1 to Section 20.1.7 below.

The guidelines are created based on the requirements of the regulations and relevant standards, however, they do not guarantee that the machinery constructed according to them will comply with the Directives. Therefore, manufacturers must finally determine how to make it comply and how it is compliant with the EMC Directives.

20.1.1 EMC standards

Standards related to the EMC directives are described below.

Specifications	Test Item	Test Description	Standard Values
EN61000-6-4 (2001)	EN55011 ^{*2} Radiated noise	Measure the emission released by the product.	30 M-230 M Hz QP : 30dB μ V/m (30m measurement) ^{*1} 230 M-1000 M Hz QP : 30dB μ V/m (30m measurement) ^{*1}
	EN55011 ^{*2} Conduction noise	Measure the emission released by the product to the power line.	150 K-500k Hz QP: 79 dB, Mean : 66 dB ^{*1} 500 K-30M Hz QP : 73 dB, Mean: 60 dB ^{*1}
EN61131-2/A12 (2000)	EN61000-4-2 ^{*2} Static electricity immunity	Immunity test by applying static electricity to the module enclosure.	4kV contact discharge 8kV air discharge
	EN61000-4-4 ^{*2} First transient burst noise	Immunity test by applying burst noise to the power line and signal line.	2kV power line 1kV signal line
	EN61000-4-12 ^{*2} Damped oscillatory wave	Immunity test in which damped oscillatory waves are applied to power line.	1kV
	EN61000-4-3 ^{*2} Radiated electromagnetic field	Immunity test in which electric fields are applied to the product.	10V/m, 26-1000MHz
EN61000-6-2 (2001)	EN61000-4-6 ^{*2} Conduction noise	Immunity test in which electromagnetic fields are induced to power cables and signal line.	10V, 0.15-80MHz

^{*1} QP: Quasi-peak value, Mean: Average value

^{*2} The PLC is an open type device (device installed to another device) and must be installed in a conductive control panel. The tests for the corresponding items were performed while the PLC was installed inside the control panel.

20.1.2 Installation inside the control panel

The PLC is open equipment and must be installed within a control panel for use.* This is effective not only for ensuring safety but also for shielding electromagnetic noise generated from the PLC.

* Each network remote station also needs to be installed inside the control panel.
However, waterproof type remote stations can be installed outside the control panel.

- (1) Control panel
 - (a) Use a conductive control panel.
 - (b) When fixing the top or base plate with bolts, mask the fixing area when painting so that an electrical contact can be made.
 - (c) To ensure an electrical contact with the control panel, mask the bolt areas of the inner plates when painting to allow conductivity over the widest possible area.
 - (d) Ground the control panel with a thick wire so that a low impedance can be ensured even at high frequencies.
 - (e) Holes made in the control panel must be 10cm (3.94inch) diameter or less. If the diameter is more than 10cm (3.94inch), radio waves can be leaked.
- (2) Connection of power cable and ground wires

Handle the power cables and ground wires as described below.

 - (a) Provide a grounding point near the power supply module. Ground the power supply module's LG and FG terminals (LG : Line Ground, FG : Frame Ground) with the thickest and shortest wire possible. (The wire length must be 30cm (11.18inch) or shorter.)As the LG and FG terminals release the noise generated in the PLC to the ground, the lowest possible impedance must be ensured. The ground wires also need to be short as they are used to release noise. Because the wire itself carries large noise, short wiring prevents it from acting as an antenna.
 - (b) Twist the ground wire led from the grounding point with the power cable. By doing this, noise from the power cable can be released to the ground. If a filter is attached to the power cable, however, this twisting may not be needed.

20.1.3 Cables

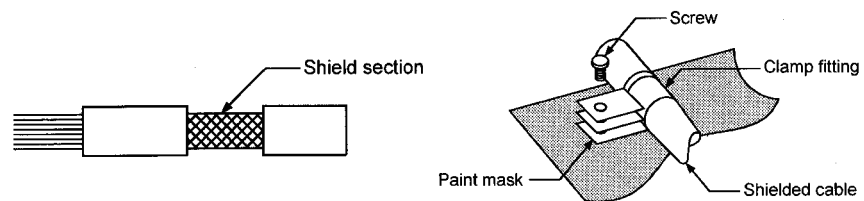
The cables running from the control panel contain a high frequency noise component, and outside the control panel, they release noise acting as antennas. Always use shielded cables when cables connected to I/O modules and/or special modules are to be brought out from the control panel.

Attaching ferrite cores is not required except some CPU types, however, using ferrite cores can restrain noise emanated via cables.

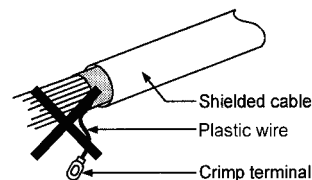
Using shielded cables also increase noise resistance. The signal lines (including common line) of the PLC, which are connected to I/O modules and/or special modules, have noise resistance compliant with EN61131-2/A12(2000) in the condition that shielded cables are to be used. If shielded cables are not used, or if grounding of shielded cables is not correct, the noise resistance will be less than the specified value.

(1) Grounding of shielded cables

- (a) Shielding must be done close to the control panel. Otherwise, electromagnetic induction from the cable after the grounding point will generate high frequency noise.
- (b) Partly remove the outer sheath of the shielded cable so that it can be contact with the widest possible area of the control panel. A clamp may also be used as shown in the figure below. In this case, cover the control panel's inner surface which will come in contact with the clamp when painting.

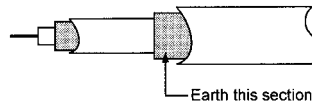


Note) Grounding a shield cable by soldering a wire to the shield section as illustrated below is not recommended. The high frequency impedance will increase and the shield will be ineffective.



(2) MELSECNET (II) and MELSECNET/10 modules

- (a) Use double-shielded coaxial cables (MITSUBISHI CABLE INDUSTRIES, LTD.: 5C-2V-CCY) for the MELSECNET modules (such as AJ71AR21, AJ71QBR11) which uses coaxial cables. Radiated noise in the range of 30 MHz or higher can be suppressed by using double-shielded coaxial cables. Ground the double-shielded coaxial cable by connecting its outer shield to the ground.



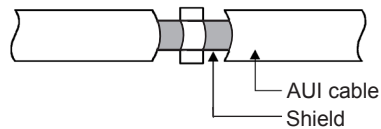
Refer to (1) for grounding of the shield.

- (b) Always attach a ferrite core to the double-shielded coaxial cable connected to the MELSECNET module. In addition, position the ferrite core on each cable near the outlet of the control panel. The ZCAT3035 ferrite core (TDK) is recommended.

(3) Ethernet module

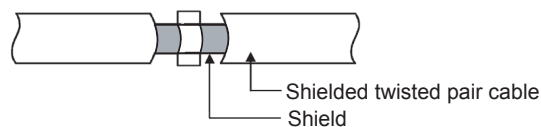
Precautions to be followed when AUI cables^{*1}, twisted pair cables and coaxial cables are used are described below.

- (a) Be sure to ground the AUI cables connected to the 10BASE5 connectors. Because the AUI cable is of the shielded type, as shown in the figure below, partly remove the outer sheath, and ground the exposed shield section to the widest possible surface.



Refer to (1) for the grounding of the shield.

- (b) Use shielded twisted pair cables as the twisted pair cables^{*1} connected to the 10BASE-T connectors. Partly strip the outer sheath of the shielded twisted pair cable, and ground the exposed shield section to the widest possible area as shown below.

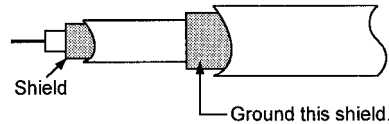


Refer to (1) for the grounding of the shield.

^{*1} Make sure to attach a ferrite core to the cable.

As a ferrite core, the ZCAT2035 manufactured by TDK is recommended.

- (c) Always use double-shielded coaxial cables as the coaxial cables^{*2} connected to the 10BASE2 connectors. Ground the double-shielded coaxial cable by connecting its outer shield to the ground.



Refer to (1) for the grounding of the shield.

- ^{*2} Make sure to attach a ferrite core to the cable.
As a ferrite core, ZCAT2035 manufactured by TDK is recommended.

Ethernet is the registered trademark of XEROX, Co.,LTD

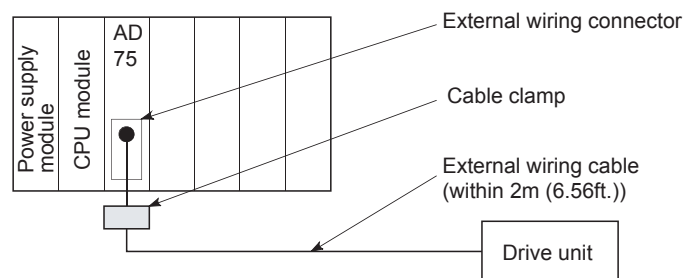
- (4) I/O signal cables and other communication cables
Always ground the I/O signal lines (including common line) and other communication cables (RS-232-C, RS-422, etc.) in the same manner as described in (1) if they are brought out of the control panel.

- (5) Positioning modules

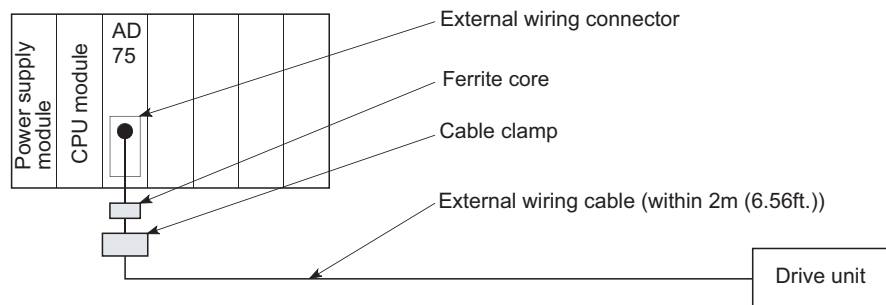
Precautions for configuring machinery compliant with the EMC Directives using the AD75P□-S3 are described below.

- (a) When using a cable of 2m (6.56ft.) or less

- Ground the shield section of the external wiring cable with a cable clamp.
(Ground the shield at the closest location to the AD75 external wiring connector.)
- Connect the external wiring cable to a drive unit or an external device in the shortest distance.
- Install the drive unit in the same panel.



- (b) When connecting a cable longer than 2m (6.56ft.), but not exceeding 10m (32.81ft.)
- Ground the shield section of the external wiring cable with a cable clamp.
(Ground the shield at the closest location to the AD75 external wiring connector.)
 - Install a ferrite core.
 - Connect the external wiring cable to a drive unit or an external device in the shortest distance.

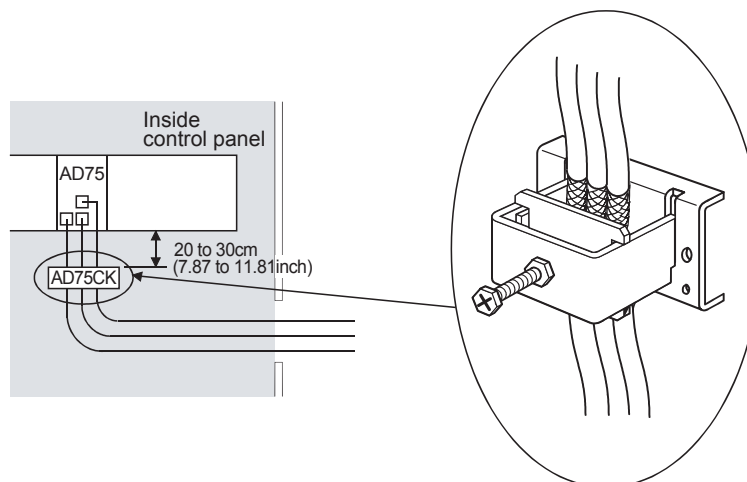


- (c) Models and required quantities of the ferrite core and cable clamp

- Cable clamp
Model: AD75CK (Manufactured by Mitsubishi Electric)
- Ferrite core
Model: ZCAT3035-1330 (TDK ferrite core)
Contact: TDK Corporation
- Required quantity

Cable length	Optional part	Required quantity		
		1 axis	2 axes	3 axes
2m (6.56ft.) or less	AD75CK	1	1	1
2m (6.6ft.) to 10m (32.8ft.)	AD75CK	1	1	1
	ZCAT3035-1330	1	2	3

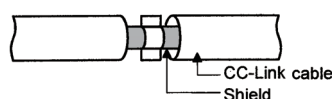
(d) Cable clamp position



(6) CC-Link module

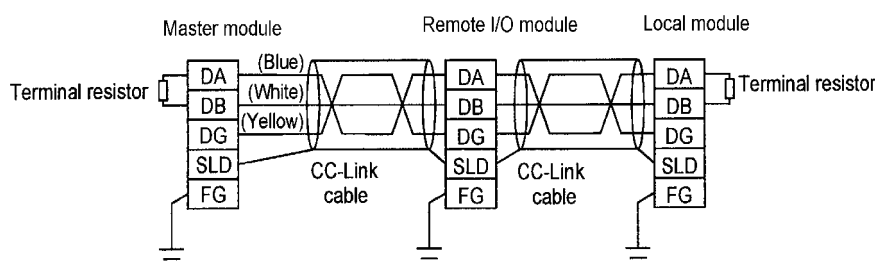
- (a) Be sure to ground the shield of the cable that is connected to a CC-Link module close to the exit of the control panel or to any of CC-Link stations within 30cm (11.81inch) from the module or stations.

The CC-Link dedicated cables are shielded cables. As shown in the illustration below, remove a part of the outer sheath and ground it to the widest possible area.



- (b) Always use the specified CC-Link dedicated cable.
 (c) Connect the CC-Link module and each CC-Link station to the FG line inside the control panel with the FG terminals as shown below.

[Simplified diagram]



- (d) Power line connecting to the external power supply terminal (compliant with I/O power port of CE standard) should be 30m (98.43 ft.) or less.
 Power line connecting to module power supply terminal (compliant with main power port of CE standard) should be 10m (32.81 ft.) or less.
- (e) A power line connecting to the analog input of the following modules should be 30cm or less.
- AJ65BT-64RD3
 - AJ65BT-64RD4
 - AJ65BT-68TD

20.1.4 Power supply module

The precautions required for each power supply module are described below. Always observe the items noted as precautions.

Model	Precautions
A61P, A62P	Use not allowed
A63P	Use a CE-compliant 24VDC power supply in the control panel.
A61PN, A61PEU, A62PEU	Make sure to short and ground the LG and FG terminals.

20.1.5 Base unit

The following table lists the base units that can be used for compliance with the EMC directives.

Type	Model	Applicability
Main Base Unit	A38HBEU	Applicable
	A3□B, A38HB	N/A
Extension Base Unit	A5□B, A6□B	Applicable

20.1.6 Ferrite core

Use of ferrite cores is effective in reducing conduction noise in the band of about 10MHz and radiated noise of 30 to 100MHz.

It is recommended to attach ferrite cores when the shield of the shielded cable coming out of control panel does not work effectively, or when emission of the conduction noise from the power supply line has to be suppressed.*1 The ferrite cores used in our tests are TDK's ZCAT3035.

It should be noted that the ferrite cores should be fitted to the cables in the position immediately before they are pulled out of the enclosure. If the fitting position is improper, the ferrite will not produce any effect.

*1 To comply with CE(EN61131-2/A12), make sure to attach 2 or more ferrite cores to the power supply line.

The position should be as close to the power supply module as possible.

• Ferrite core

Model: ZCAT2235-1030A (TDK ferrite core)

Contact: TDK Corporation

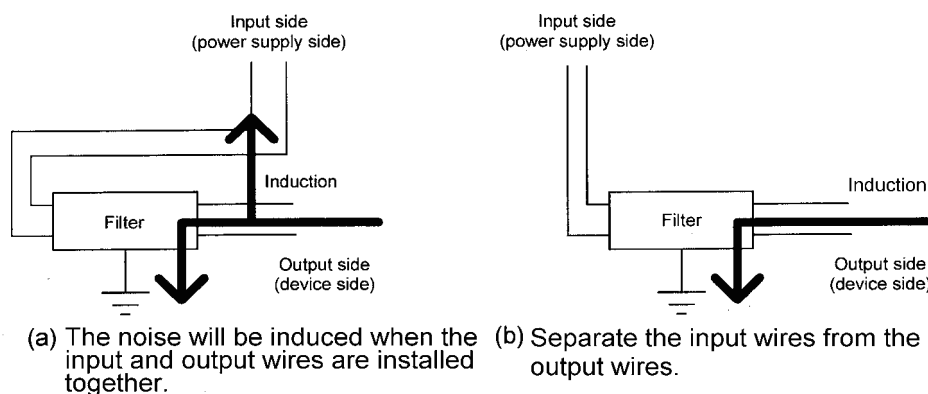
20.1.7 Noise filter (power supply line filter)

A noise filter is a component which has an effect on conducted noise. With the exception of A61PEU, A62PEU and A63P, it is not required to fit the noise filter to the power supply line, but fitting it can further suppress noise. (The noise filter has the effect of reducing conducted noise of 10 M Hz or less.) Use any of the following noise filters (double π type filters) or equivalent.

Model name	FN343-3/01	FN660-6/06	ZHC2203-11
Manufacturer	SCHAFFNER	SCHAFFNER	TDK
Rated current	3A	6A	3A
Rated voltage	250V		

The precautions required when installing a noise filter are described below.

- (1) Do not bundle the wires on the input side and output side of the noise filter. When bundled, the output side noise will be induced into the input side wires from which noise has been filtered out.



- (2) Ground the noise filter ground terminal to the control panel with the shortest wire possible (approx. 10cm (3.94inch)).

20.2 Requirements for Compliance with Low Voltage Directives

The Low Voltage Directives apply to the electrical equipment operating from 50 to 1000VAC or 75 to 1500VDC; the manufacturer must ensure the safety of the equipment. Sections 20.2.1 to 20.2.7 provide precautions on installation and wiring of the MELSEC-QnA series PLC to conform to The Low Voltage Directives.

The descriptions are made based on the requirements and standards of the latest regulation. However, they do not guarantee that any machinery produced according to the contents of this manual is compliant with the above directives. Therefore, manufacturers must finally determine how to make it comply it and how it is compliant with the low voltage directives.

20.2.1 Standard applied for MELSEC-QnA series PLC

The standard applied for MELSEC-QnA series PLC is EN61010-1 safety of devices used in measurement, control, or laboratories.

For the modules which operate with the rated voltage of 50 VAC/75 VDC or above, we have developed new models that conform to the above standard.

For the modules which operate with the rated voltage less than 50 VAC or 75 VDC, conventional models can be used, because the low voltage directives do not apply to them.

20.2.2 Precautions when using the QnA series PLC

Module selection

(1) Power supply module

Since a power supply module with the rated input voltage of 100/200VAC has a potentially hazardous voltage area (42.4V or more at the peak), select a model in which reinforced insulation is provided between the primary and secondary sides. For those of 24VDC rated input, conventional models can be used.

(2) I/O module

Since an I/O module with the rated input voltage of 100/200VAC has a potentially hazardous voltage area, select a model in which reinforced insulation is provided between the primary and secondary sides. For those of 24VDC rated input, conventional models can be used.

(3) CPU module, memory card, base unit

Conventional models can be used for these modules, because they only have a 5VDC circuit inside.

(4) Special function module

Conventional models can be used for the special function modules including analog modules, network modules, and positioning modules, because their rated voltage is 24 V DC or lower.

(5) Display

Use the CE-marked product.

20.2.3 Power supply

The insulation specification of the power supply module was designed assuming installation category II. Be sure to use the installation category II power supply to the PLC. The installation category indicates the durability level against surge voltage generated by a thunderbolt. Category I has the lowest durability; and category IV has the highest durability.

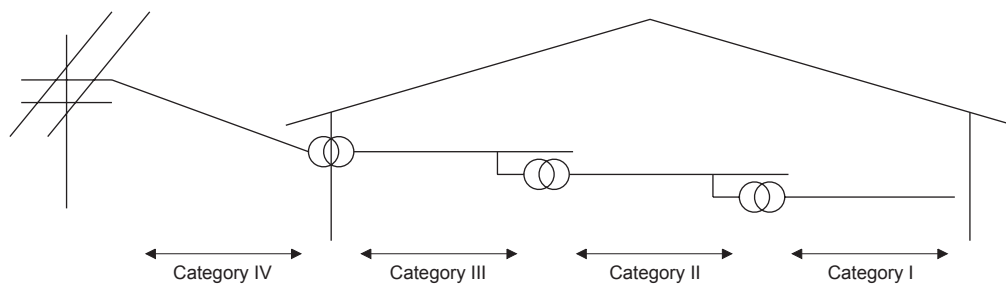


Fig. 20.1 Installation category

Category II indicates a power supply whose voltage has been reduced by two or more levels of isolating transformers from the public power distribution.

20.2.4 Control panel

Because the PLC is an open type device (a device designed to be stored within another device), be sure to use it inside the control panel.*

* Also, each network remote station needs to be installed inside the control panel. However, the waterproof type remote station can be installed outside the control panel.

(1) Shock protection

To prevent personnel such as operators who are not familiar with electricity from electric shocks, the control panel must be handled as follows:

- (a) Lock the control panel so that only the qualified personnel can open it.
- (b) Provide a mechanism so that opening the control panel will automatically stop the power supply.
- (c) For electric shock protection, use IP20 or greater control panel.

(2) Dustproof and waterproof features

The control panel also has the dustproof and waterproof functions. Insufficient dustproof and waterproof features lower the insulation withstand voltage, resulting in insulation destruction. As our PLCs are designed assuming the pollution level 2, use them in an environment of pollution level 2 or lower.

Pollution level 1: An environment where the air is dry and conductive dust does not exist.

Pollution level 2: An environment where conductive dust does not usually exist, however, temporary conductivity may occasionally occur due to accumulated dust. Generally, this is the level for the inside of the IP54-equivalent control panel in a control room or on a shop floor.

Pollution level 3: An environment where conductive dust exists and conductivity may be generated due to accumulated dust. An environment for a typical factory floor.

Pollution level 4: Continuous conductivity may occur due to rain, snow, etc. An outdoor environment.

As shown above, the PLC can meet pollution level 2 when stored in a control panel equivalent to IP54.

20.2.5 Module installation

(1) Installing modules contiguously

The left side face of each QnA series I/O module is open. When installing I/O modules to the base, do not allow any empty slots between modules. If a slot to the left of a 100/200VAC module is left empty, the circuit board containing the hazardous voltage circuit is exposed. When a slot needs to be left open, be sure to install the blank module (AG60).

When using the A5□B expansion base with no power supply, attach the included cover to the side of the leftmost module.

20.2.6 Grounding

There are two kinds of ground terminals as shown below. Either ground terminal must be used grounded.

Be sure to perform protective grounding to ensure the safety.

Protective grounding (⏏): Ensures the safety of the PLC and improves the noise resistance.

Functional grounding (⏏): Improves the noise resistance.

20.2.7 External wiring

(1) Module power supply and external power supply

For the remote module which requires 24VDC as module power supply, the 5/12/24/48VDC I/O module, and the special function module which requires the external power supply, use the 5/12/24/48VDC circuit which is doubly insulated from the hazardous voltage circuit or use the power supply whose insulation is reinforced.

(2) External devices

When a device with a hazardous voltage circuit is externally connected to the PLC, use a model whose circuit section of the interface to the PLC is intensively insulated from the hazardous voltage circuit.

(3) Reinforced insulation

Reinforced insulation refers to the insulation with the dielectric withstand voltage shown in Table 1.

Reinforced Insulation Withstand Voltage (Installation Category II, source : IEC664)

Rated voltage of hazardous voltage area	Surge withstand voltage (1.2/50 μ s)
150VAC or less	2500V
300VAC or less	4000V

21 MAINTENANCE AND INSPECTION

In order to use the PLC always in good condition, conducting daily and periodical maintenance/inspection on the following items are strongly recommended.

21.1 Daily Inspection

Daily inspection items recommended are shown in Table 21.1.

Table 21.1 Daily inspection

Item	Check item		Content of inspection	Judgement	Action
1	Installation condition of the base unit		Confirm if installation screws are not loose or cover is not detached.	It is installed securely.	Retighten the screw.
2	Installation condition of the I/O modules		Check if the module is not disengaged and if the hook is securely engaged.	The hook should be securely engaged and the module should be positively mounted.	Securely engage the hook.
3	Connection conditions		Loosening of terminal screw.	No loosening.	Retighten the terminal screw.
			Proximity of solderless terminals.	There is an appropriate distance.	Correct the distance.
			Connector areas of extension cable.	No loosening at connectors.	Retighten the connector fixing screw.
4	LEDs on the main module	Power supply module POWER LED	Confirm it is ON.	The LED is ON. (Faulty if it is OFF.)	Refer to Section 22.2.2.
		CPU module "RUN" LED	Confirm it is ON in the "RUN" state.	The LED is ON. (Faulty if it is OFF.)	Refer to Section 22.2.3. Section 22.2.4.
		CPU module "ERROR" LED	Check that the LED is OFF.	OFF (Faulty if it is ON or flickering.)	Refer to Section 22.2.5.
		CPU module "BAT. ARM" LED	Check that the LED is OFF.	OFF (Faulty if it is ON.)	Refer to Section 22.2.7.
		Input module LED	Confirm if it correctly turns on and off.	The LED is ON when input is ON, and OFF when input is OFF. (Faulty other than the above.)	Refer to Section 22.2.8.
		Output module LED	Confirm if it correctly turns on and off.	The LED is ON when output is ON, and OFF when output is OFF. (Faulty other than the above.)	Refer to Section 22.2.8.

REMARK

If an I/O module has to be replaced when the system is running, use the "online I/O module replacement" function.

21.2 Periodic Inspection

Inspection on items shown below should be conducted once or twice every six months to a year. Conduct the inspection when the equipment is moved or modified, or wiring is changed.

Table 21.2 Periodic inspection

Item	Check item		Check method	Judgement	Action
1	Ambient environment	Ambient temperature	Measure with temperature and humidity gauge.	0 to 55°C	When used in a panel, temperature inside the panel is the ambient temperature.
		Ambient humidity		10 to 90%RH	
		Atmosphere	Measure presence of corrosive gases.	There is no corrosive gas present.	
2	Line voltage check		100/200VAC, 24VDC, 110VDC Measure voltage across 100/200VAC terminals.	85 to 132VAC	Change the power supply.
				170 to 264VAC	
				15.6 to 31.2VDC	
				85 to 140VDC	
3	Fuse		Check if the fuse is blown.	(Preventive maintenance)	Even if a fuse has not blown, the element may have deteriorated due to inrush current, and the fuse should therefore be changed at regular intervals.
4	Installation condition	Loosening, backlash	Test by moving the module.	Must be installed solidly.	Retighten the screw. For CPU module, I/O module, and power supply modules check all connections.
		Adhesion of dirt or foreign matters	Visual inspection	No adhesion.	Remove and clean.
5	Connection conditions	Loosening of terminal screw	Retighten with a screwdriver.	No loosening.	Retighten.
		Proximity of solderless terminals	Visual inspection	There is an appropriate distance.	Correct the distance.
		Loosening of connector	Visual inspection	No loosening.	Retighten the connector fixing screw.
6	Battery		Confirm SM51 or SM52 is OFF with a peripheral device in the monitoring mode.	(Preventive maintenance)	Even when there is no low-battery display, replace if specified life is exceeded.

**DANGER**

- Be sure to shut off all phases of the external power supply used by the system before cleaning or retightening the terminal screws or module mounting screws. Failure to do so may result in an electric shock.
If they are too loose, it may cause a short circuit or malfunctions.
If too tight, it may cause damage to the screws and/or module, resulting in an accidental drop of the module, short circuit or malfunctions.

21.3 Battery Replacement

Special relay SM51 or SM52 is turned ON when voltage of the battery for backing up programs and power failure compensation function drops. Even though programs and contents of power failure compensation function are not erased immediately when these special relays become ON, the contents could be erased if the ON-status of the special relay fails to be recognized. Replace the battery before the total latch time after special relay SM51 turns ON reaches the stipulated time.

POINT	
	SM51 is a battery voltage drop alarm, and it remains ON once turning it ON even if the battery voltage returns to normal.
	SM52 is a battery voltage drop alarm, and after turning ON, it goes OFF when the battery voltage returns to normal.
	After SM51 and SM52 have turned ON, immediately replace the battery.

SM51 and SM52 will turn ON if there is a voltage drop in the battery of any of the following: the built-in RAM, memory card A, or memory card B.

In order to determine which of these memory's battery has sustained the voltage drop, check the contents of special relay SD51 and SD52.

When the voltage of any memory's battery drops, the bit in SD51 and SD52 that corresponds to each memory turns ON.

SD51, SD52 bit No.	Corresponding memory
Bit 0	Built-in RAM
Bit 1, 2	Memory card A
Bit 3, 4	Memory card B

POINTS				
The relationship of back up between the status of the batteries installed in the CPU module and memory cards is explained below. The following two points are applied. 1) The battery installed in the CPU module does not back up the RAM memories of the memory cards. 2) The batteries installed in the memory cards do not back up the built-in RAM of the CPU module.				
AC power supply for CPU module	CPU module battery	Memory card battery	CPU module memory	Memory card memory
ON	ON	ON	○	○
		OFF	○	○
	OFF	ON	○	○
		OFF	○	○
OFF	ON	ON	○	○
		OFF	○	×
	OFF	ON	×	○
		OFF	×	×

○ : Back up is possible.
 × : Back up is not possible.

The battery life guideline and the replacement procedures are explained on the following pages.

21.3.1 Battery life

(1) Battery life of CPU module

The CPU module battery life differs depending on the CPU model. The life for each CPU model is shown in Table 21.3.

Table 21.3 CPU module battery life

CPU module model name	Battery life (Total power failure time) [hr]		
	Guaranteed value (MIN)	Actual value (TYP)	After SM51 is turned ON
Q2ACPU	1800	14500	48
Q2ACPU-S1	1150	10700	27
Q3ACPU	4000	18000	113
Q4ACPU	1750	6200	44

* Actual value indicates a rough average value and guaranteed value indicates the minimum value.

POINT
(1) Switch batteries regularly in case that battery hours (total power failure time) exceed guaranteed values. (2) When the battery hours (total power failure time) may exceed the guaranteed value, take the following measures. Perform ROM operation to protect a program in case that the battery dies at PLC power supply OFF. After SM51 (Battery low) turns ON, back up a program and data within the specified time shown in the Table 21.3.

(2) Battery life of memory card

The battery life of memory card differs depending on the memory capacity. The life for each memory is shown in Table 21.4.

Table 21.4 Battery lives of memory cards

Memory card model name	Battery life (Total power failure time) [hr]		
	Guaranteed value (MIN)	Actual value (TYP)	After SM51 is turned ON
Q1MEM-64S	5256	23652	8
Q1MEM-128S	2628	12264	6
Q1MEM-256S	5256	23652	8
Q1MEM-512S	2628	12264	6
Q1MEM-1MS	7008	23652	6
Q1MEM-2MS	2628	12264	6
Q1MEM-64SE	5256	23652	8
Q1MEM-128SE	5256	23652	8
Q1MEM-256SE	5256	23652	8
Q1MEM-512SE	5256	23652	8
Q1MEM-1MSE	2628	12264	6

* Actual value indicates a rough average value and guaranteed value indicates the minimum value.

The guide for preventive maintenance is as follows.

- 1) Replace in 4 to 5 years even when the total power failure time is less than the guaranteed value shown in the table above.
- 2) Replace when the total power failure time exceeds the guaranteed value shown in the table above and the SM51 is ON.

21.3.2 Battery replacement procedure

**DANGER**

- Properly connect batteries.

Do not charge, disassemble, heat or throw them into the fire and do not make them short-circuited and soldered.

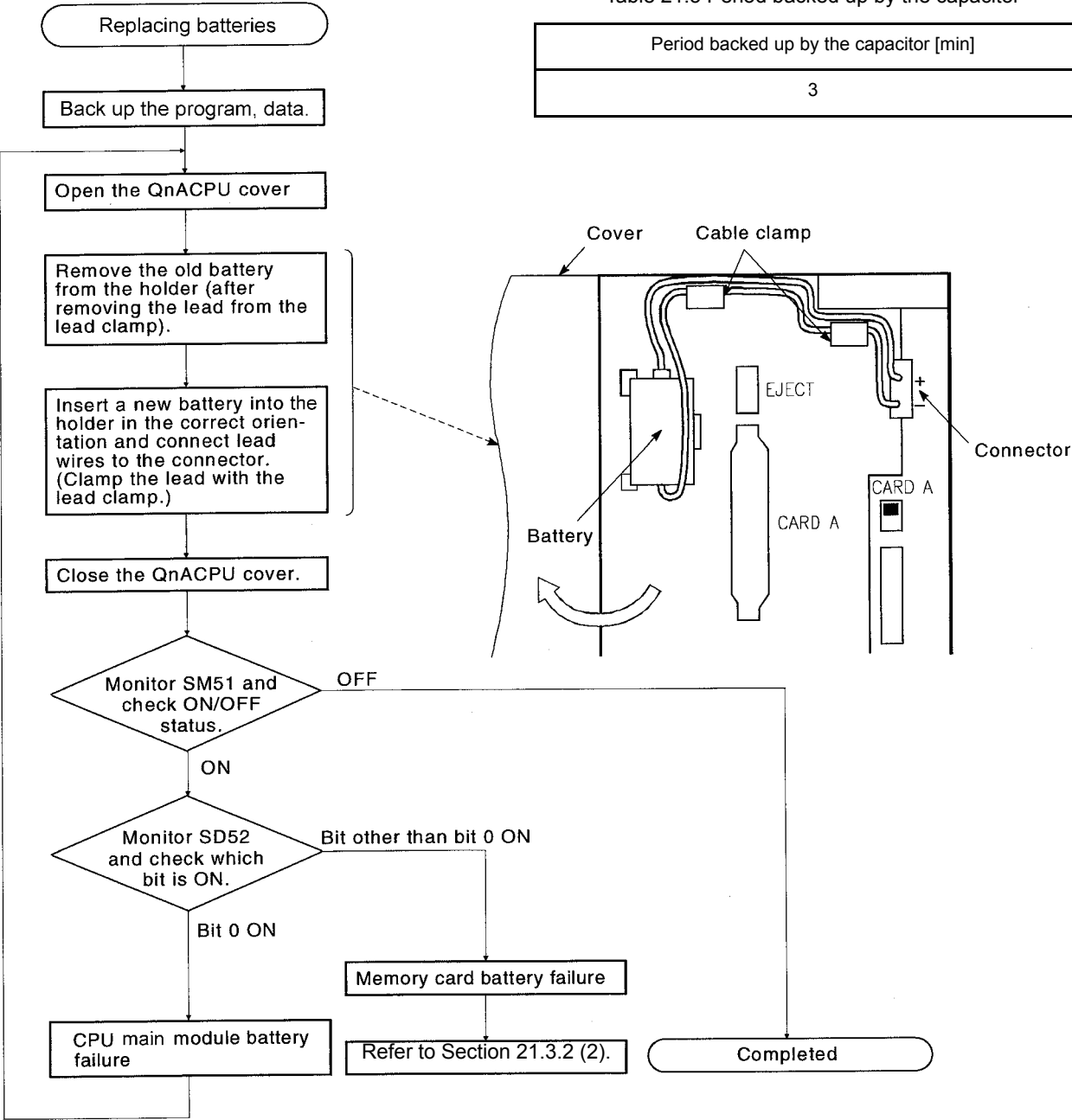
Incorrect battery handling may cause personal injuries or a fire due to exothermic heat, burst and/or ignition.

(1) CPU module battery replacement procedure

Replace the battery of a CPU module according to the following procedure when life of the battery is over. Even when the battery is removed, memory is backed up by the capacitor for a while. However, if replacement takes longer than the guaranteed value shown in the following table, the content of the memory may be erased, so replace the battery quickly. Even if the PLC power is ON, the battery of the CPU module can be replaced. In this case, the memory contents are backed up by the power supply voltage from the power supply module.

Table 21.5 Period backed up by the capacitor

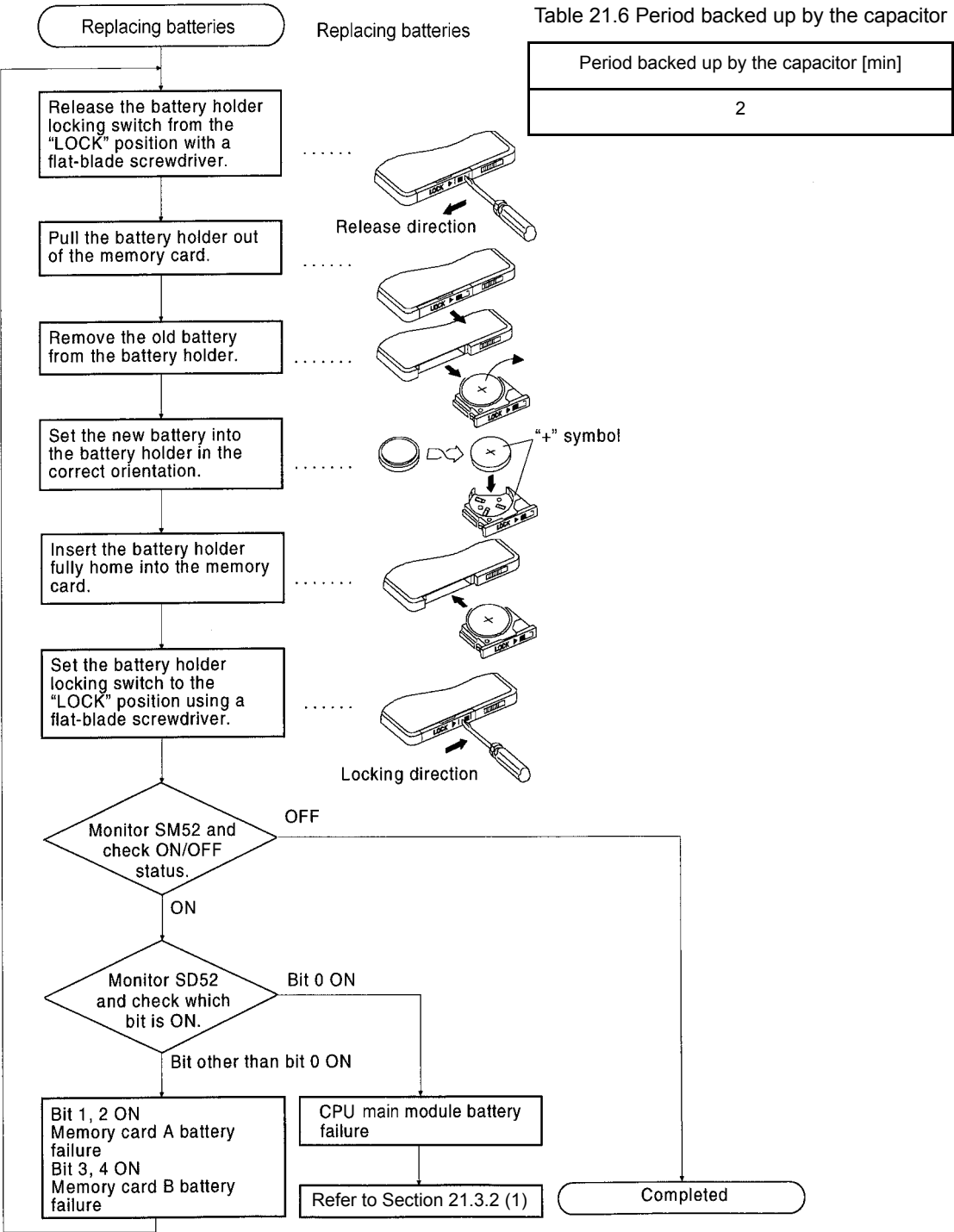
Period backed up by the capacitor [min]
3



(2) Memory card battery replacement procedure

Replace the memory card battery according to the following procedure when the life is over. Even if the battery is removed, the memory card memory is backed up by a capacitor so that the battery can be replaced while the memory card is out of the CPU module.

However, if the time taken to replace the battery exceeds the guaranteed value indicated in Table 21.6 below, the contents of the memory may be lost. Therefore, change the battery as quickly as possible. While the PLC power is ON, the battery can be replaced without removing the memory card in the CPU module. In this case, the memory contents are backed up by the power supply voltage from the power supply module.



21.4 Fuse Replacement

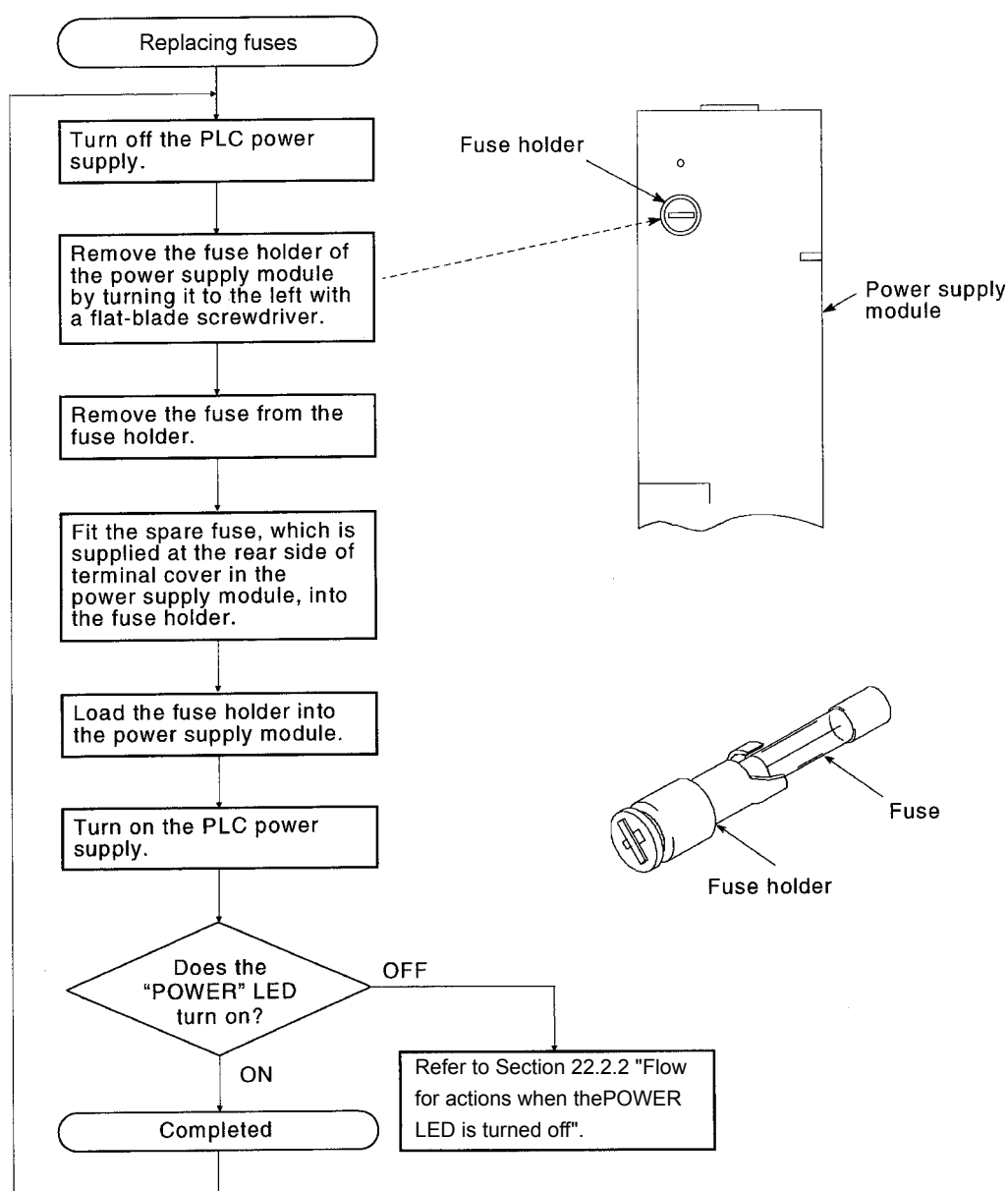
Even if a fuse has not blown, the element may have deteriorated due to inrush current, and the fuse should therefore be changed at regular intervals.

**CAUTION**

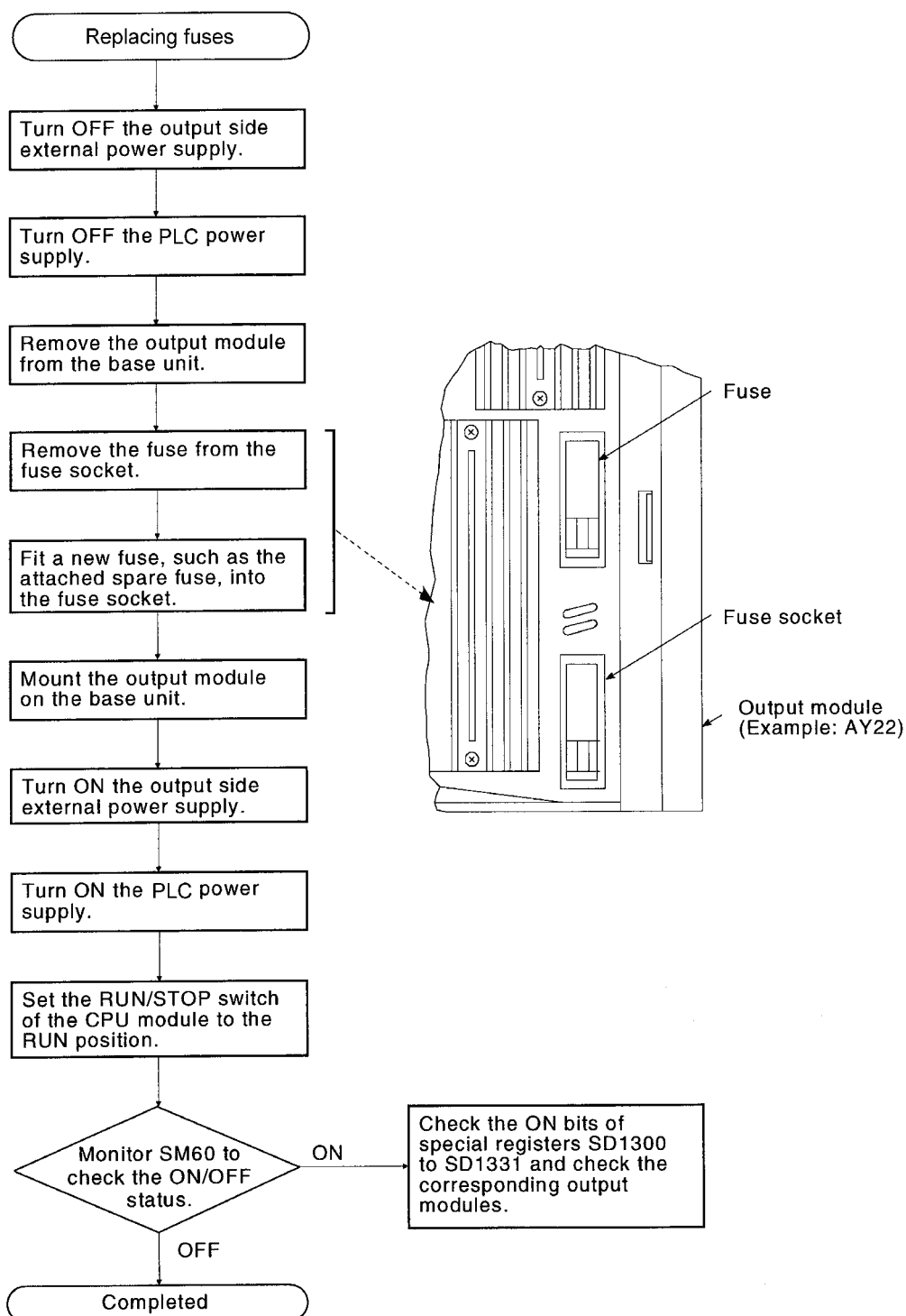
- When replacing the fuse, use a fuse specified by the manufacturer.
Using the one for the high-rated current or an electric wire may cause a fire.

21.4.1 Replacement of the fuse for a power supply module

The procedure for replacing the fuse is as follows.



21.4.2 Replacement of the fuse for an output module



21.5 When Reoperating a PLC After Storing it with a Battery Unconnected

When reoperating after a battery is uncounted and the PLC is stored, the memory contents of a CPU module and memory card may be undefined.

Therefore, when resuming the operation, clear the CPU module memory and format the memory in the CPU module by peripheral device.

After doing so, write the memory contents backed up before saving to each memory.

The relationship between the backed-up memory and the batteries is explained below.

Memory			Battery	
			A6BAT installed in a CPU module	Battery incorporates a memory card
CPU module	Built-in RAM		○	×
	Device*		○	×
Memory card	SRAM type		×	○
	SRAM + E ² PROM type	SRAM	×	○
		E ² PROM	– (Battery back up is not required.)	

○: Battery is backed up. ×: Battery is not backed up.

*As for device memory, also clear the latch range.

Before resuming the operation, clear/format the memory for which a battery is backed up in the table above with a peripheral device.

For memory clear/format operations, refer to the following manuals.

- Type SW□ IVD-GPPQ GPP Software package Operating Manual (Online)
- GX Developer Operating Manual

POINT
(1) Make sure to back up each memory contents before storing the PLC. When a PLC power supply is ON or CPU module reset is cancelled, a CPU module reviews the status of data below, and initializes all the data if detecting an error. ▪ RAM data in built-in RAM ▪ Breakdown history ▪ Latch data (Latch relay (L), latch setting range device set in a parameter), special relay SM900 to SM999, special register SD900 to SD999) ▪ Sampling trace data

21.6 When a PLC is Reoperated After Stored with the Battery Over the Battery Life

If a battery exceeded its guaranteed life is stored and reoperated, the memory contents of CPU module and memory card may be undefined.

Therefore, when resuming the operation, clear the CPU module memory and format the memory in the CPU module by peripheral device.

After doing so, write the memory contents backed up before saving to each memory.

The relationship between the backed-up memory and the batteries is explained below.

Memory			Battery	
			A6BAT installed in a CPU module	Battery incorporates a memory card
CPU module	Built-in RAM		○	×
	Device*		○	×
Memory card	SRAM type		×	○
	SRAM + E2PROM type	SRAM	×	○
		E2PROM	– (Battery back up is not required.)	

○: Battery is backed up. ×: Battery is not backed up.

*As for device memory, also clear the latch range.

Before resuming the operation, clear/format the memory for which a battery is backed up in the table above with a peripheral device.

For memory clear/format operations, refer to the following manuals.

- Type SW□ IVD-GPPQ GPP Software package Operating Manual (Online)
- GX Developer Operating Manual

POINT
(1) Make sure to back up each memory contents before storing a PLC. (2) When a PLC power supply is ON or CPU module reset is cancelled, a CPU module reviews the status of data below, and initializes all the data if detecting an error. ▪ RAM data in built-in RAM ▪ Breakdown history ▪ Latch data (Latch relay (L), latch setting range device set in a parameter), special relay SM900 to SM999, special register SD900 to SD999) ▪ Sampling trace data

22 TROUBLESHOOTING

The description, cause determination, and corrective actions of each error which may occur during system usage are described.

22.1 Fundamentals of Troubleshooting

Besides using obviously highly-reliable devices to increase system reliability, it is an important point to quickly start up the system again when an error occurs. In order to quickly start up the system, find the cause of the problem and resolve it. There are the following three basic points to be aware of when performing troubleshooting.

(1) Visual confirmation

Confirm the following points:

- 1) Machine operation (stop status and operation status)
- 2) Power supply ON/OFF
- 3) I/O equipment status
- 4) Wiring status (I/O wires and cable)
- 5) Display status of each display indicator (POWER LED, RUN LED, ERROR LED, I/O LED, etc.)
- 6) Status of each setting switch (extension base, power failure compensation, etc.)

After confirming 1) to 6), connect a peripheral device and observe the operation status of the PLC and program contents.

(2) Error confirmation

Observe how the error changes by performing the following operations:

- 1) Set the RUN/STOP key switch to "STOP".
- 2) Reset using the RUN/STOP key switch.
- 3) Turn ON/OFF the power supply.

(3) Narrow down the range

By performing the (1) and (2) above, assume the faulty area in the following:

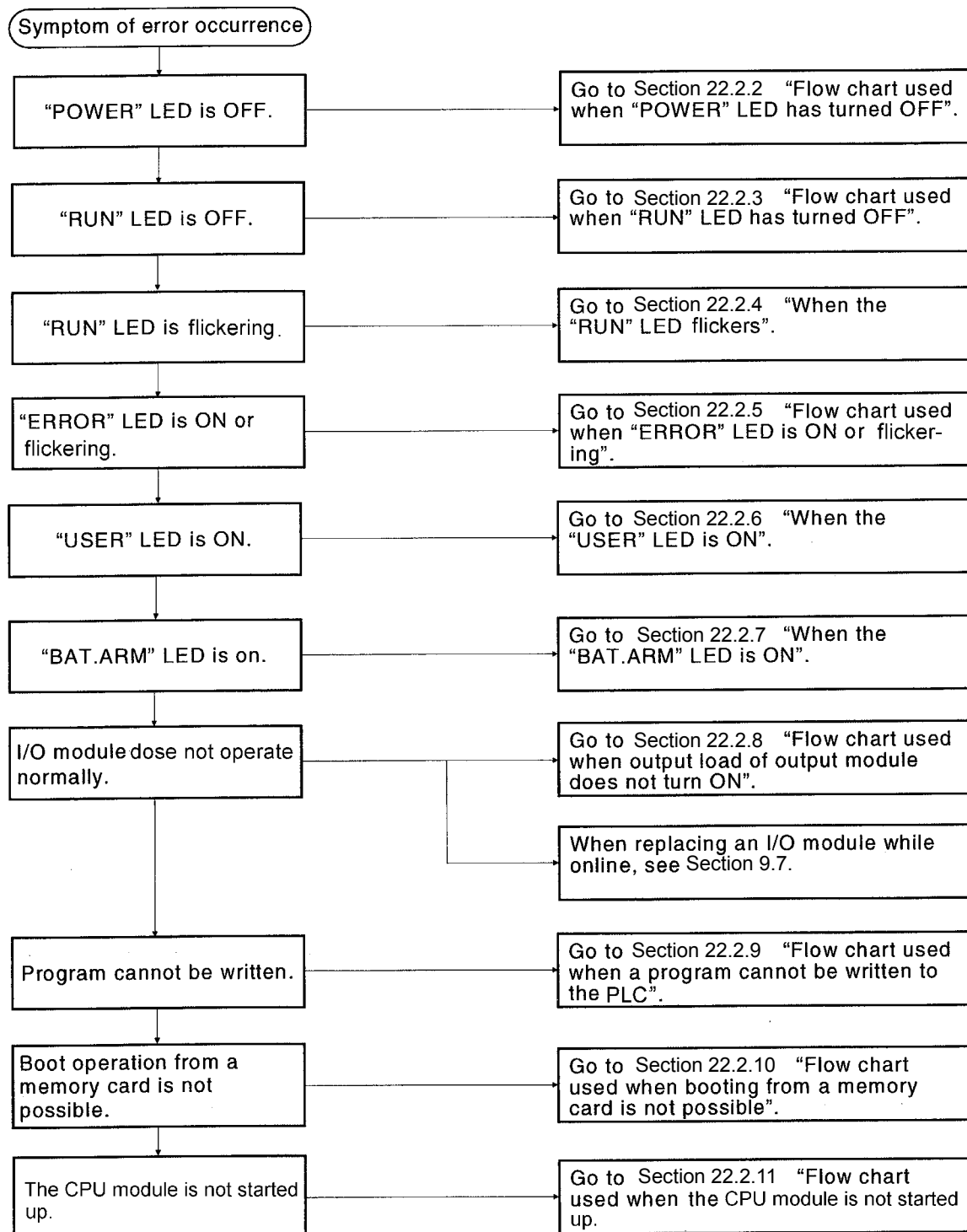
- 1) PLC or external?
- 2) I/O module or others?
- 3) Sequence program?

22.2 Troubleshooting

The error definition determination method, error definition corresponding to the error code, and corrective actions are described.

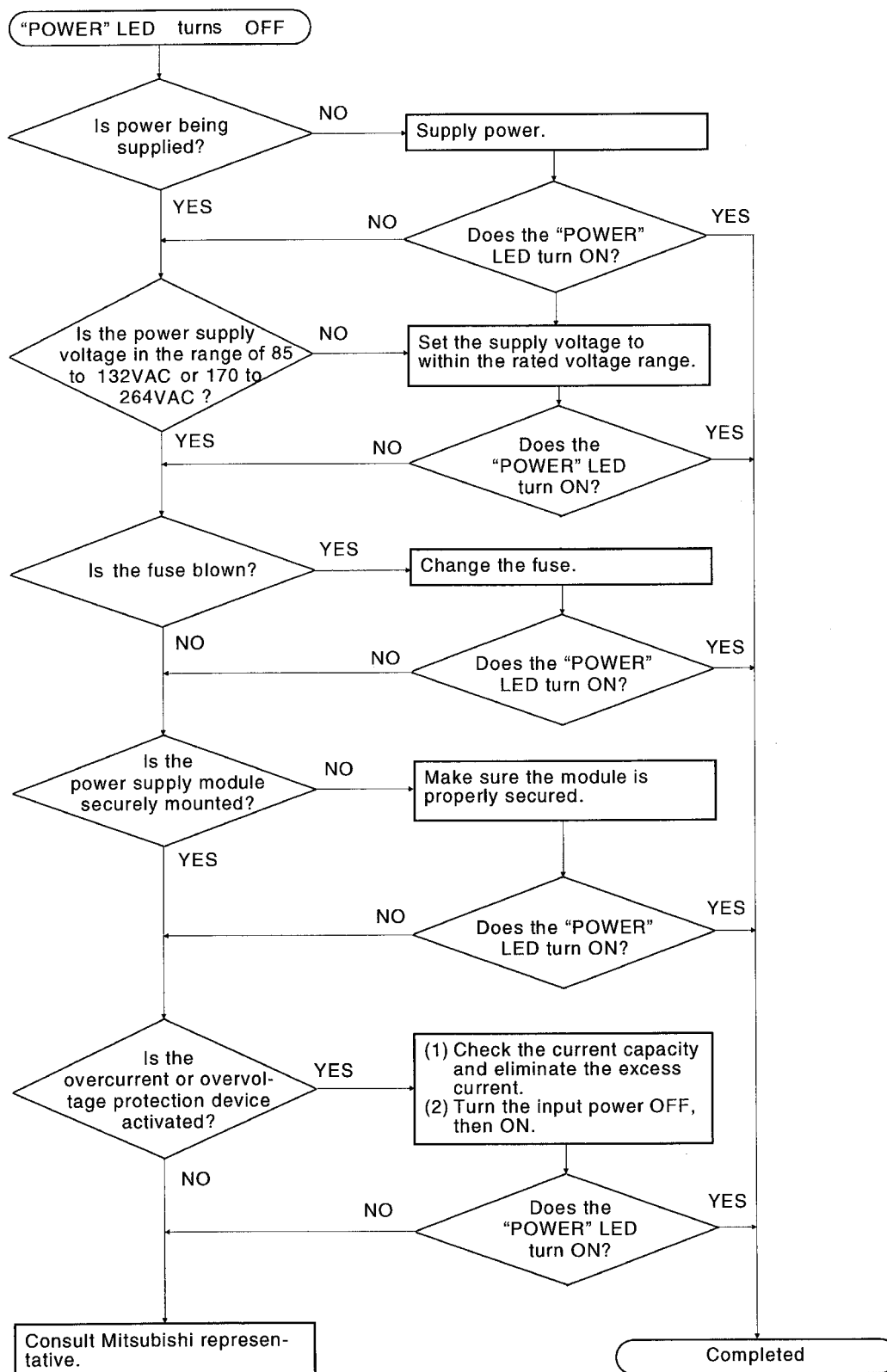
22.2.1 Troubleshooting flowchart

The error definitions are described by events.



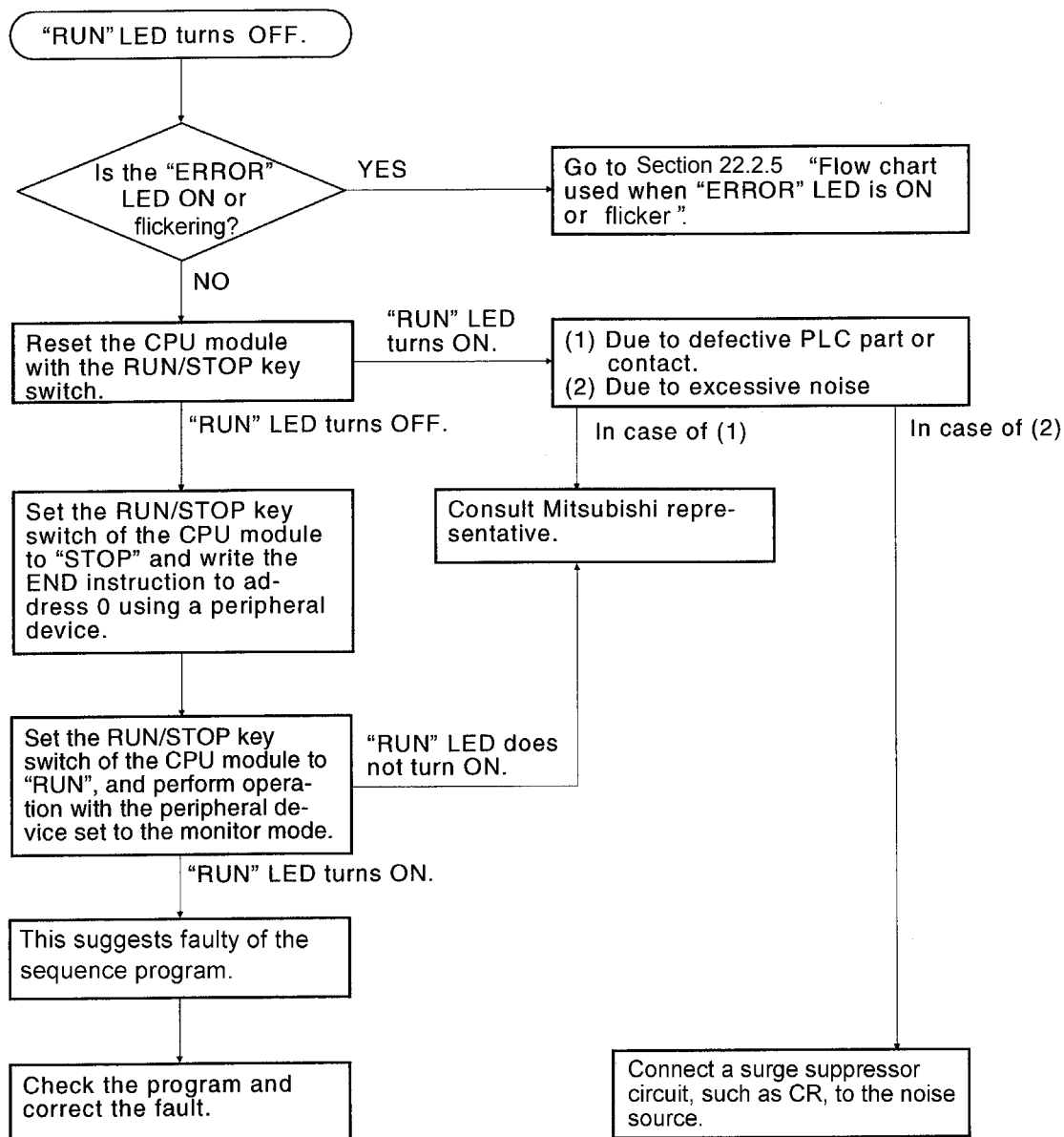
22.2.2 Flow for actions when the "POWER" LED is turned OFF

The flow when the PLC power is ON or when the "POWER" LED of the power supply module is ON during operation is described.



22.2.3 Flow for actions when the "RUN" LED is turned OFF

The flow when the "POWER" LED of the CPU module turns OFF during operation is described.



22.2.4 When the "RUN" LED is flashing

Flashing of the "RUN" LED of a CPU module is described below.

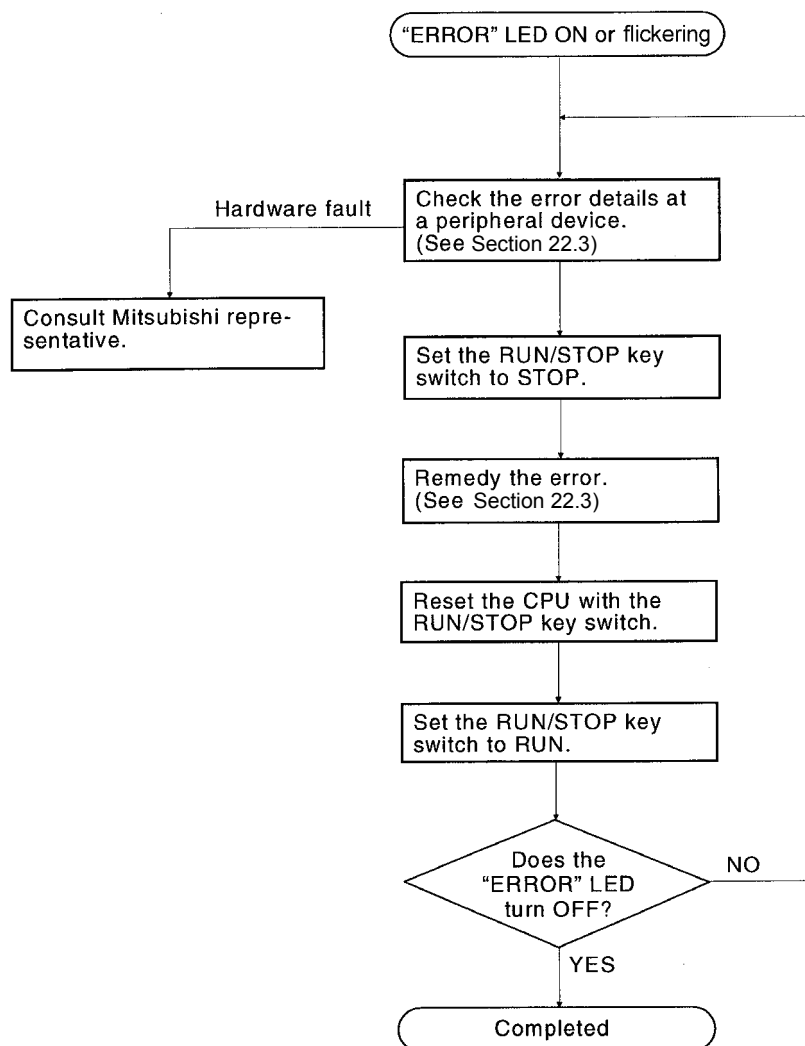
With the QnACPU, when the RUN/STOP key switch is turned from STOP to RUN after writing a program in the STOP state, the "RUN" LED flashes. Then, no CPU module error occurs, but the operation stops.

To set the CPU module to RUN, either turn the RUN/STOP key switch to STOP then RUN again, or reset the CPU module using the key switch. The "RUN" LED turns ON.

With the Q3ACPU and Q4ACPU, the message "PRG.CHECK!!" is displayed on the LED indicator on the front panel of the CPU module.

22.2.5 Flow for actions when the "ERROR LED" is turned ON/flashing

The flow when the PLC power is ON, when the operation is started or when the "ERROR" LED of the CPU module is ON/blinking during operation is described. Note that in the case of the Q3ACPU and Q4ACPU, an error message is displayed in the LED indicator on the front panel. Check and correct the error following an error code list. Section 22.3.3.



22.2.6 When the "USER" LED is turned ON

The case when the "USER" LED of the CPU module is turned ON is described.

With the QnACPU, the "USER" LED comes ON when an error is detected by the CHK instruction, or when an annunciator (F), turns ON.

When the "USER" LED is turned ON, monitor SM62 and SM80 of the special relay in the peripheral device monitor mode.

After monitoring and removing the cause, the "USER" LED can be turned OFF by resetting the RUN/STOP key switch or performing the LEDR instruction.

- When SM62 is ON
With the annunciator (F) ON, the "USER" LED is ON.
Check the error cause with SD62 to SD79.
- When SM80 is ON
With execution of the CHK instruction, the "USER" LED is ON.
Check the error cause with SD80.

After checking the error cause, remove the cause.

The "USER" LED can be turned OFF by either of the following operations.

- Resetting the system with the RUN/STOP key switch
- Execution of the LEDR instruction with the sequence program

REMARK

When the RUN/STOP key switch is turned to "L.CLR" several times in a latch clear operation, the "USER" LED flashes to indicate that latch clear processing is in progress.

(With Q3ACPU and Q4ACPU, the message "L.CLR RDY" is displayed in the LED indicator on the front panel of the CPU module.)

When the RUN/STOP key switch is turned once more to "L.CLR" while the "USER" LED is flashing, the "USER" LED goes OFF and latch clear processing is ended.

22.2.7 When the "BAT.ARM" LED is turned ON

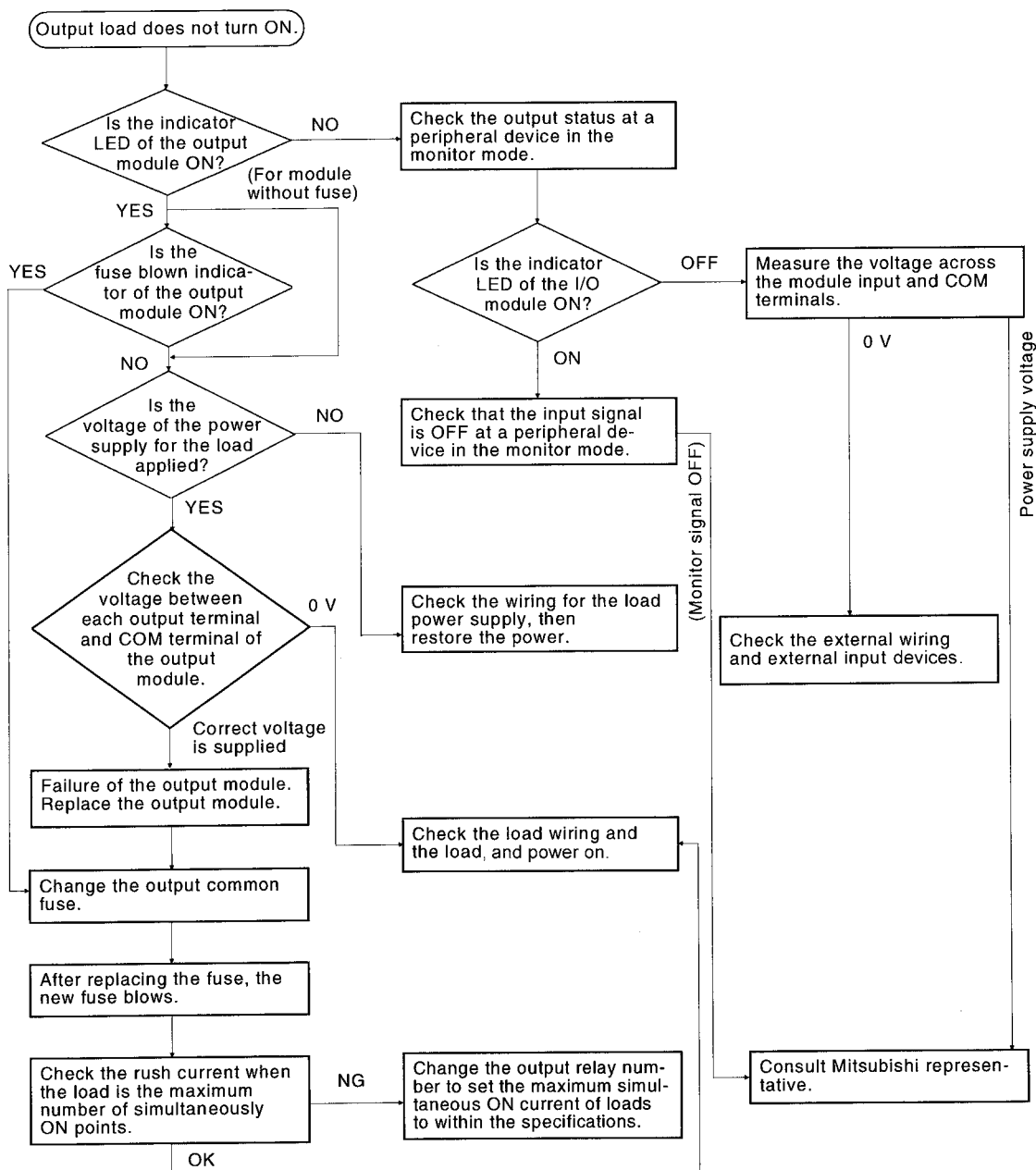
The case when the "BAT.ARM" LED of the CPU module is turned ON is described.

With the QnACPU, the "BAT.ARM" LED turns ON when the voltage of the battery for a CPU module or a memory card drops.

When the "BAT.ARM" LED turns ON, monitor the special relays (SM51 and SM52) and special registers (SD51 and SD52) in the peripheral device monitor mode, and check if there has been a voltage drop at either of the battery for a CPU module or a memory card. After monitoring and replacing the battery by a new one, the "BAT.ALM" LED can be turned OFF by resetting the RUN/STOP key switch or performing the LEDR instruction. With the Q3ACPU and Q4ACPU, a message is displayed in the LED indicator on the front panel of the CPU module.

22.2.8 Flow for actions when the output module's output load does not turn ON

The flow when the output load of the output module is not turned ON during operation is described.

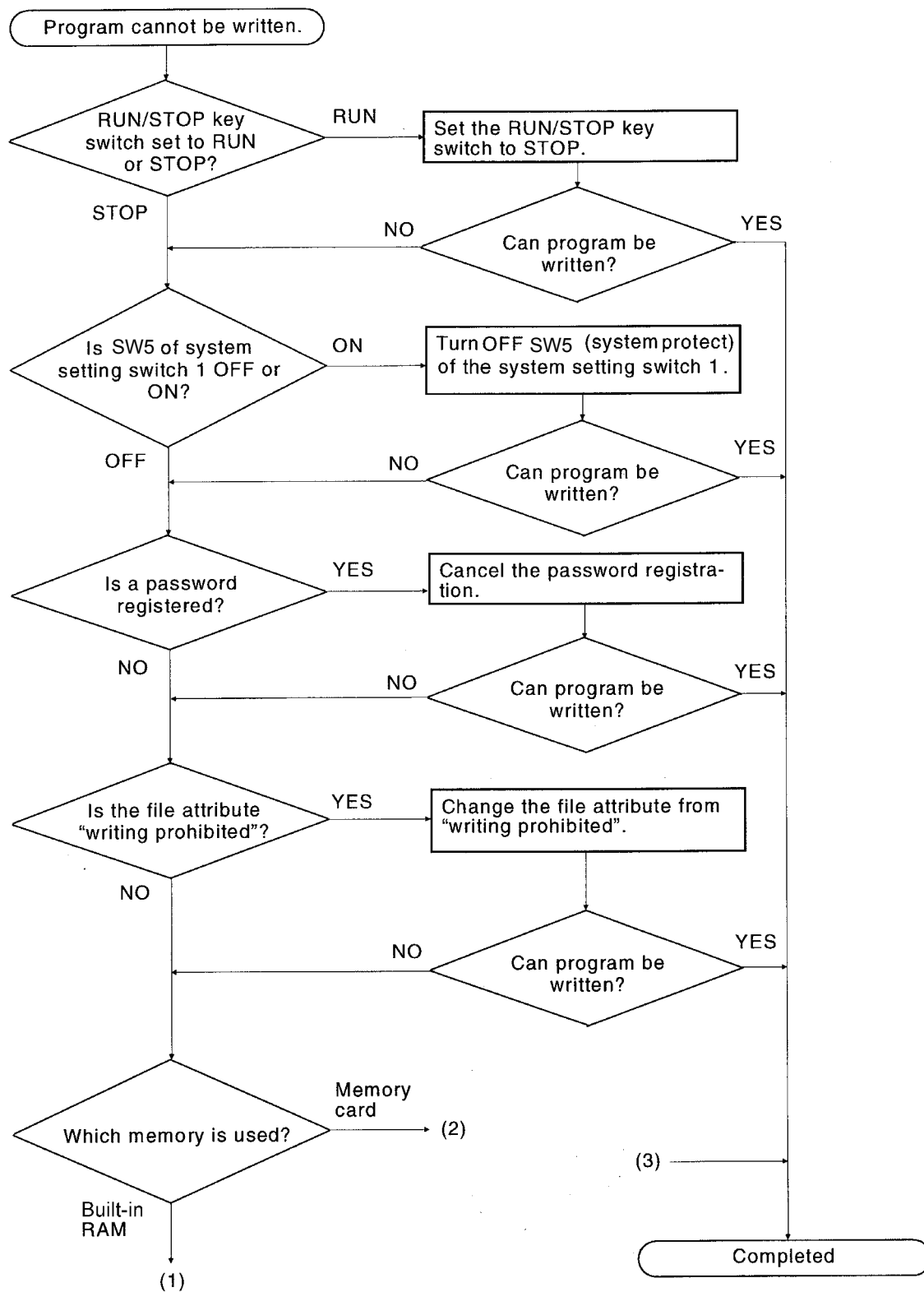


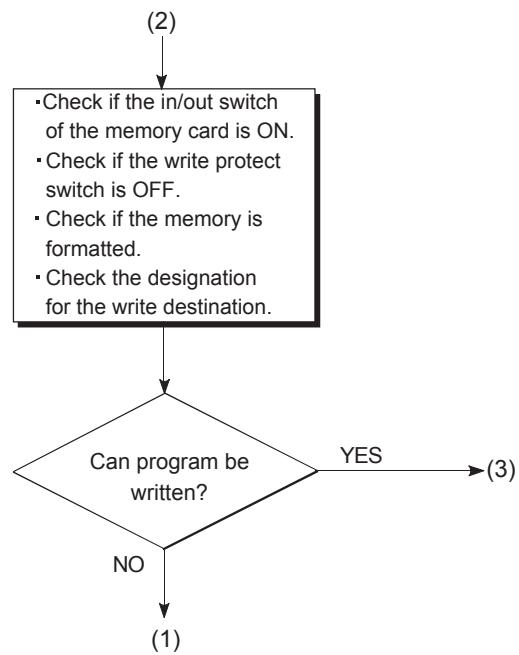
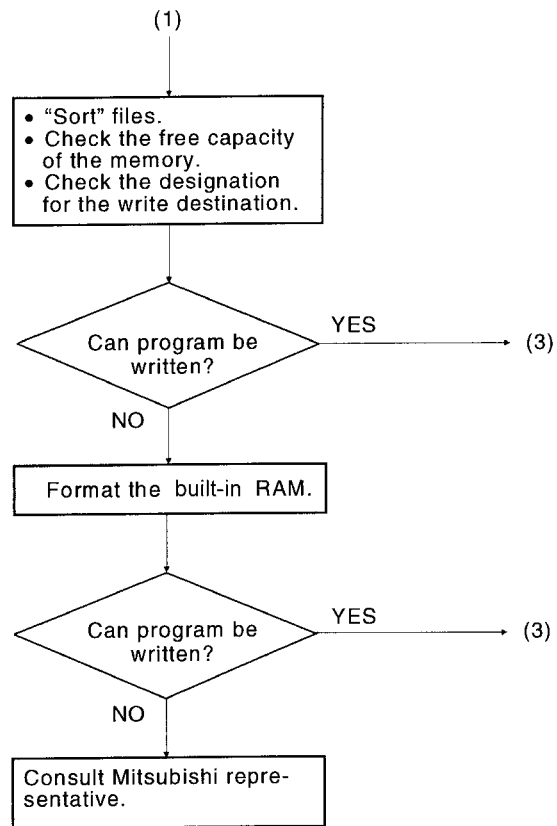
POINT

For problems when the input signal does not turn off or output load does not turn off, perform troubleshooting by referring to the fault examples for the I/O modules in Section 22.5.

22.2.9 Flow for actions when the program cannot be written

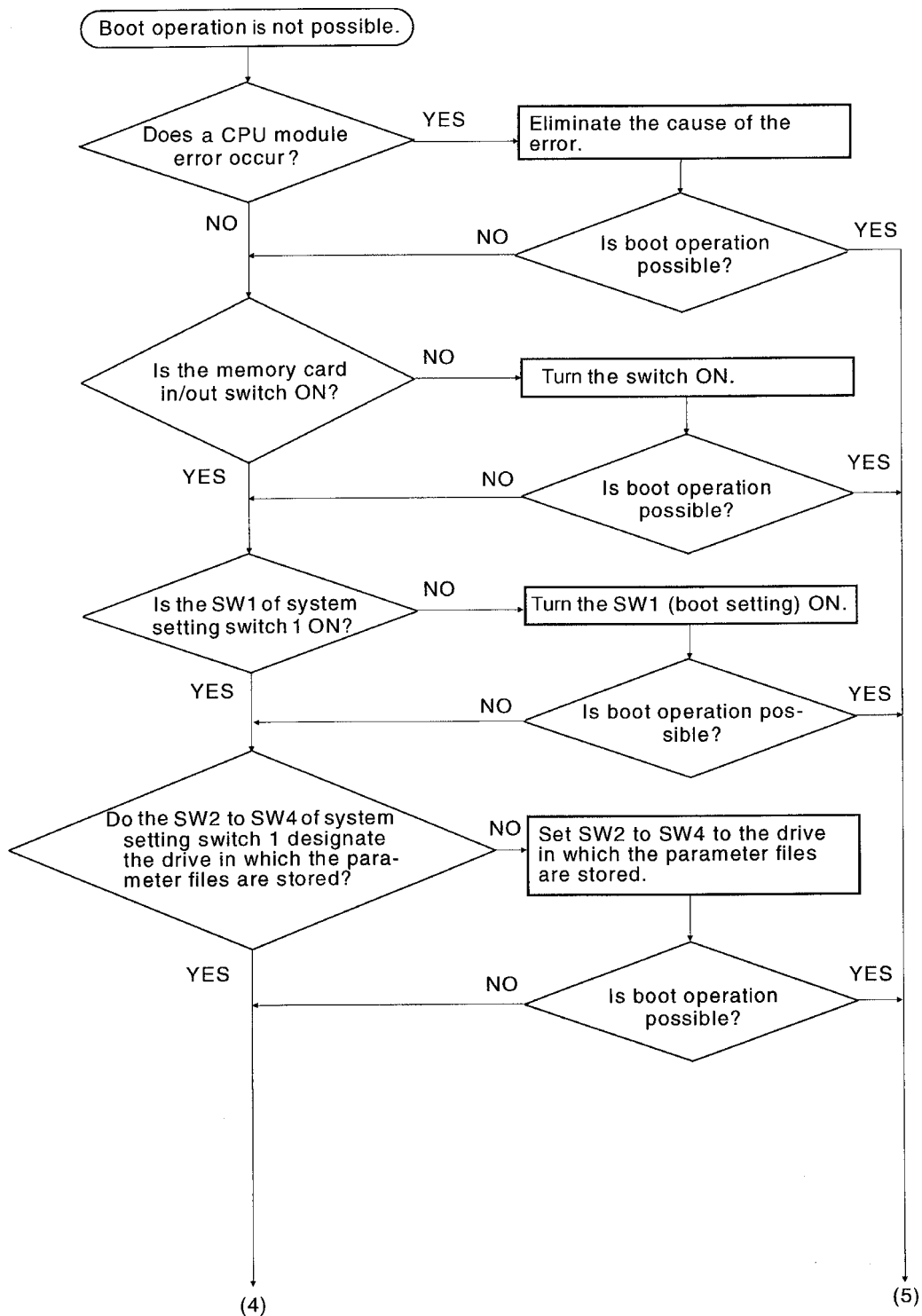
The flow when a program cannot be written to the CPU module is described.

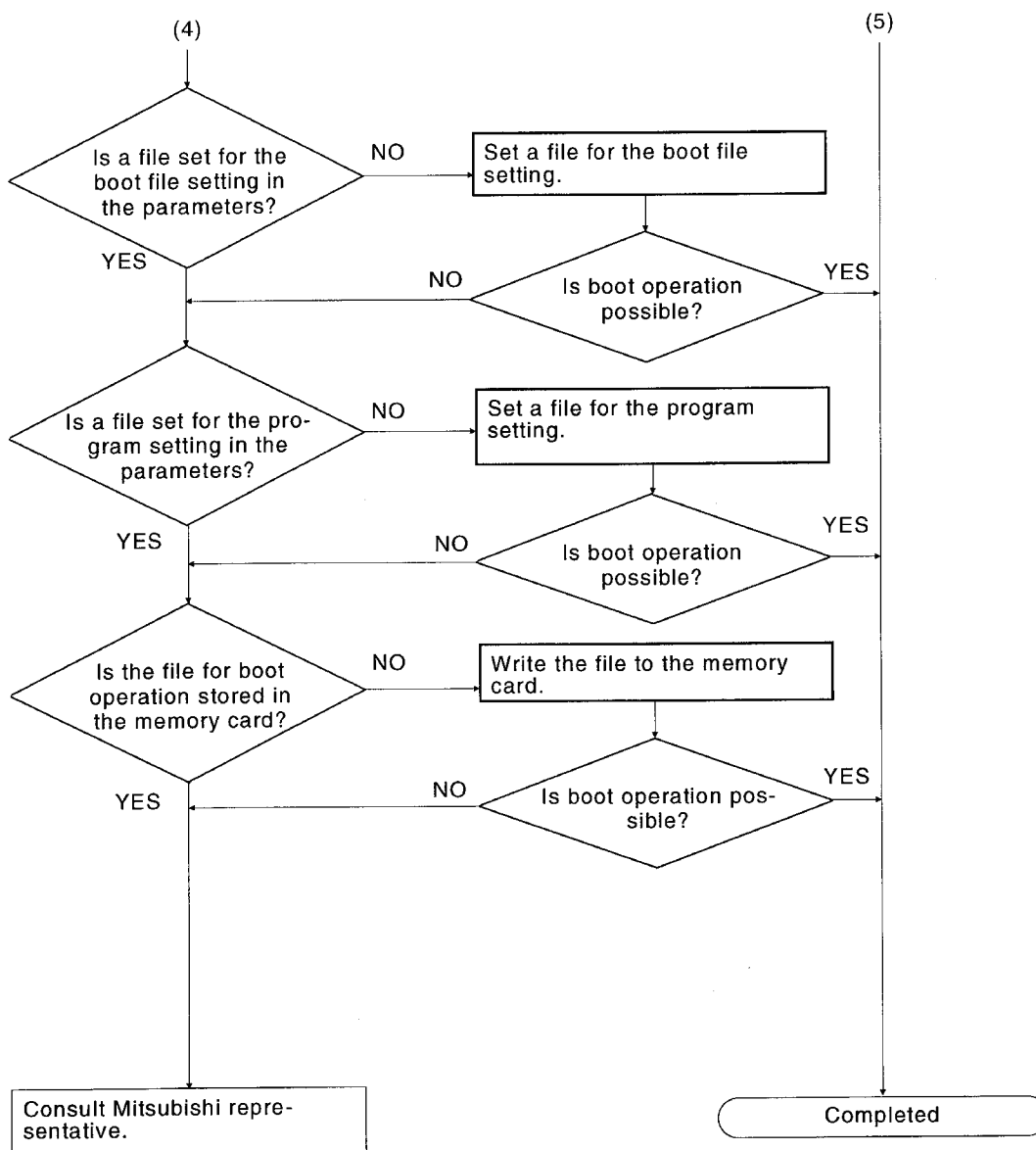




22.2.10 Flow for actions when booting from a memory card is not possible

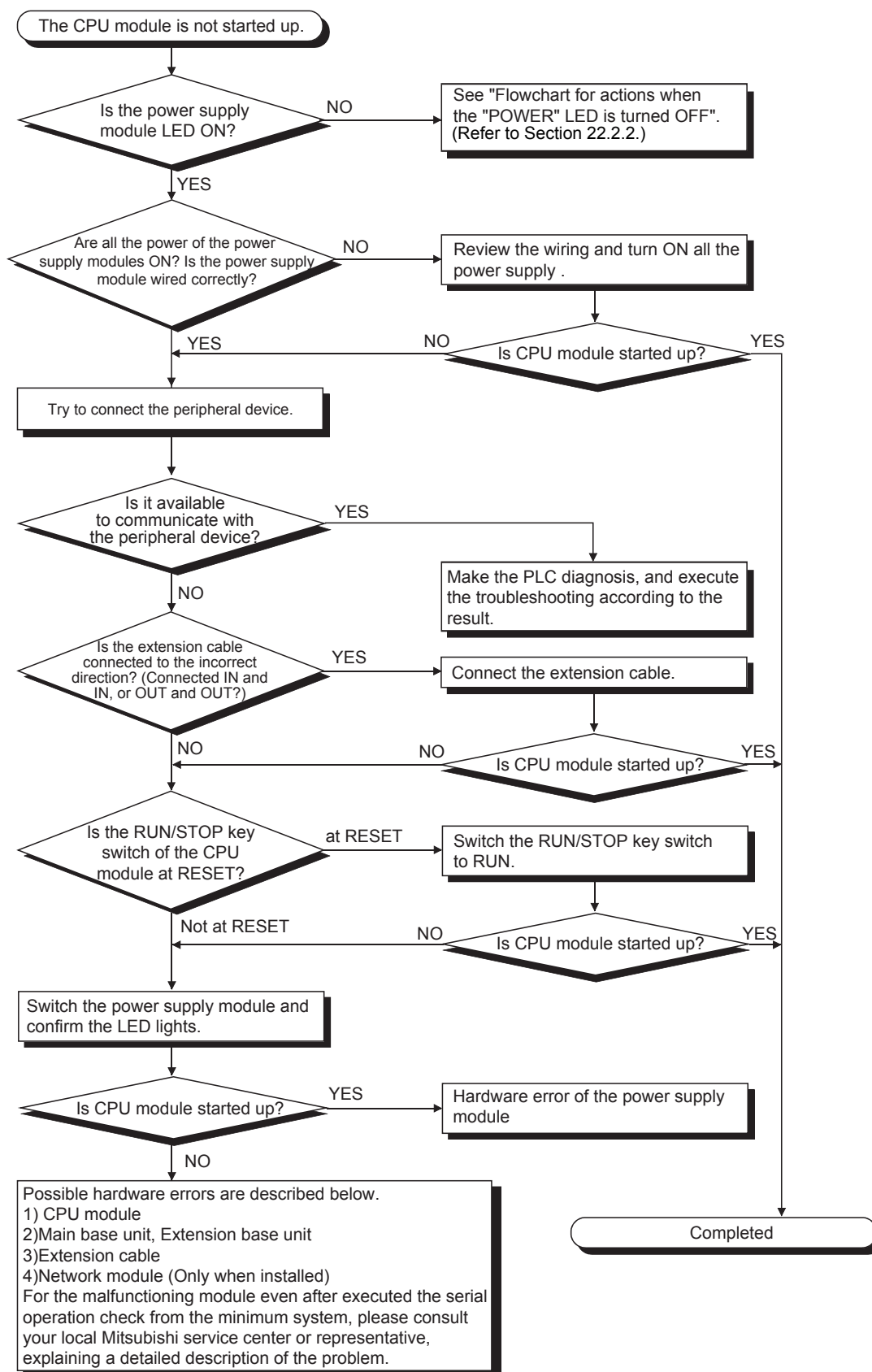
The flow when the CPU module cannot be booted from a memory card is described.





22.2.11 Flow chart used when the CPU module is not started up

The following shows the flow when the CPU module is not started up.



MEMO

[illegible]

22.3 Error Code List

When an error occurs at PLC power ON, on switching to the RUN status, or during the RUN status, the self-diagnostics function displays the error content (by LED indication, or message display on an LED indicator), and stores the error information at a special relay (SM) and special register (SD).

If an error occurs on a data communication request from peripheral devices, a special function module and the network system to the CPU module, error codes (4000H to 4FFFH) are returned to the request source.

QnACPU errors and corrective actions are described in this section.

(1) How to read the error code lists

The following shows the way of reading the error code lists from Section 22.3.3 (1000 to 1999) to Section 22.3.9 (7000 to 10000).

(a) Error code, common information, and individual information

Alphanumeric characters in the parentheses of the titles indicate the special register numbers where the individual information is stored.

(b) Compatible CPUs

○	: Compatible with all the QnACPU and QCPU.
QCPU	: Compatible with all the Q series CPU module.
Q00J/Q00/Q01	: Compatible with the Basic model QCPU.
Qn(H)	: Compatible with the High Performance model QCPU.
QnPH	: Compatible with the process CPU.
QnPRH	: Compatible with the redundant CPU.
QnA	: Compatible with the QnA series and Q2ASCPU series.
Rem	: Compatible with the MELSECNET/H remote I/O module.
Each CPU module	: Compatible with the listed CPU module. (Example: Q4AR, Q2AS)

22.3.1 Error Codes

There are errors that is detected by the self-diagnostics function of the CPU module, and that is detected while communicating with the CPU module.

The table below shows the link between the type of error detection, the point of error detection and the error codes.

Error Detection Type	Error Detection Point	Error Code	Reference for Error Contents
Detection by the self-diagnostics function of the CPU module	CPU module	1000 to 10000 ^{*1}	Section 22.3.3 to Section 22.3.9
Detection while communicating with the CPU module	CPU module	4000H to 4FFFH	Appendix 5
	Serial communication	7000H to 7FFFH	Serial Communication Module User's Manual
	CC-Link module	B000H to BFFFH	CC-Link System Master/Local Module User's Manual
	Ethernet module	C000H to CFFFH	Ethernet Interface Module User's Manual
	MELSECNET/10 network module	F000H to FFFFH	QnA/Q4AR MELSECNET/10 Network System Reference Manual

^{*1} The error codes of the CPU module are categorizes according to minor errors, moderate errors and major errors.

Minor error: Errors that CPU module such as a battery error continues the operation (Error code: 1300 to 10000)

Moderate error: Errors that CPU module such as a WDT error stops the operation (Error code: 1300 to 10000)

Minor error: Errors that CPU module such as a RAM error stops the operation (Error code: 1000 to 1299)

"The error that the QnACPU continues operation" and "the error that QnACPU stops operation" are determined by "CPU operation status" of the error code list.

22.3.2 Procedure to read an error code

When an error occurs, error codes and error messages can be read with the peripheral devices.

For details on the setting method for each function, refer to the GX Developer Operating Manual or SW□IVD-GPPQ Operating Manual (Offline).

22.3.3 Error code list (1000 to 1999)

The following shows the error messages from the error code 1000 to 1999, the contents and causes of the errors, and the corrective actions for the errors.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1000	MAIN CPU DOWN	—	—	Off	Flicker	Stop	Always	
1001								
1002								
1003								
1004								
1005								
1006								
1007								
1008								
1009								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALAM LED is displayed at BATTERY ERROR.

Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
1000	Runaway or failure of CPU module or failure of main CPU • Malfunctioning due to noise or other reason • Hardware fault	• Take noise reduction measures. • Reset the CPU module and RUN it again. If the same error is displayed again, this suggests a CPU module hardware fault. (Contact your local Mitsubishi representative.)	○
1001			Q00J/Q00/Q01
1002			Qn(H)
1003			QnPH
1004			QnPRH
			QnU
1005			Q00J/Q00/Q01
			Qn(H)
			QnPH
1006			QnPRH
			QnU
1007			Qn(H)
1008			QnPH
			QnPRH
1009	• A failure is detected on the power supply module, CPU module, main base unit, extension base unit or extension cable. • When using the redundant base unit, the redundant power supply module failure in both systems and/or the redundant base unit failure are detected.	Reset the CPU module and RUN it again. If the same error is detected again, it is considered that the power supply module, CPU module, main base unit, extension base unit or extension cable is faulty. (Contact your local Mitsubishi representative.)	Q00J/Q00/ Q01 ^{*4} Qn(H) ^{*6} QnPH QnPRH QnU

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1010	END NOT EXECUTE	—	—	Off	Flicker	Stop	When an END instruction executed	
1020	SFCP. END ERROR	—	—	Off	Flicker	Stop	When SFC program is executed	
1035	MAIN CPU DOWN	—	—	Off	Flicker	Stop	Always	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALM LED is displayed at BATTERY ERROR.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	1010	Entire program was executed without the execution of an END instruction. - When the END instruction is executed it is read as another instruction code, e.g. due to noise. - The END instruction has been changed to another instruction code somehow.	- Take noise reduction measures. - Reset the CPU module and RUN it again. If the same error is displayed again, this suggests a CPU module hardware fault. (Contact your local Mitsubishi representative.)	○
	1020	The SFC program cannot be normally terminated due to noise or other reason. - The SFC program cannot be normally terminated due to noise or any similar cause. - The SFC program cannot be normally terminated for any other reason.		Q00J/Q00/ Q01 ^{*4} QnPH QnU
	1035	Runaway or error of the CPU module was detected. - Malfunction due to noise etc. - Hardware failure	- Take measures against noise. - Reset the CPU module and run it again. If the same error is displayed again, the CPU module has hardware failure. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	QnU

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1101	RAM ERROR	—	—	Off	Flicker	Stop	At power ON/ At reset/ When an END instruction executed	
1102							At power ON/ At reset/ When an END instruction executed	
1103							At power ON/ At reset	
							At power ON/ At reset/ When an END instruction executed	
1104	RAM ERROR	—	—	Off	Flicker	Stop	At power ON/ At reset	
1105								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALM LED is displayed at BATTERY ERROR.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	1101	The sequence program storing built-in RAM/program memory in the CPU module is faulty.	- Take noise reduction measures. - Reset the CPU module and RUN it again. If the same error is displayed again, this suggests a CPU module hardware fault. (Contact your local Mitsubishi representative.)	○
	1102	The work area RAM in the CPU module is faulty.	- Take noise reduction measures. - Reset the CPU module and RUN it again. If the same error is displayed again, this suggests a CPU module hardware fault. (Contact your local Mitsubishi representative.)	○
	1103	The device memory in the CPU module is faulty.	- Take noise reduction measures. - When indexing is performed, check the value of index register to see if it is within the device range. - Reset the CPU module and RUN it again. If the same error is displayed again, this suggests a CPU module hardware fault. (Contact your local Mitsubishi representative.)	○
		- The device memory in the CPU module is faulty. - The device out of range is accessed due to indexing, and the device for system is overwritten.		Qn(H) ^{*8} QnPH ^{*8} QnPRH ^{*9}
	1104	The address RAM in the CPU module is faulty.	- Take noise reduction measures. - Reset the CPU module and RUN it again. If the same error is displayed again, this suggests a CPU module hardware fault. (Contact your local Mitsubishi representative.)	○
	1105	The system RAM in the CPU module is faulty.		Q4AR
		The CPU memory in the CPU module is faulty.		Q00J/Q00/Q01 QnU
		The CPU shared memory in the CPU module is faulty.		Qn(H) ^{*4} QnPH QnPRH QnU

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1106	RAM ERROR	—	—	Off	Flicker	Stop	STOP→RUN/ When an END instruction executed	
1107	RAM ERROR	—	—	Off	Flicker	Stop	At power ON/ At reset	
1108								
1109							Always	
1110	TRK. CIR. ERROR	—	—	Off	Flicker	Stop	At power ON/ At reset	
1111		—	—	Off	Flicker	Stop		

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALM LED is displayed at BATTERY ERROR.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	1106	The battery is dead. The program memory in the CPU module is faulty.	• Check the battery to see if it is dead or not. If dead, replace the battery. • Take noise reduction measures. • Format the program memory, write all files to the PLC, then reset the CPU module, and RUN it again. If the same error is displayed again, the possible cause is a CPU module hardware fault. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	Qn(H) QnPH*7 QnPRH
	1107	The work area RAM in the CPU module is faulty.	This suggests a CPU module hardware fault. (Contact your local Mitsubishi representative.)	QnPRH
	1108			Qn(H)*8 QnPH*8 QnPRH*9
	1109			
	1110	A fault was detected by the initial check of the tracking hardware.		QnPRH
	1111	A tracking hardware fault was detected.		

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1112	TRK. CIR. ERROR	—	—	Off	Flicker	Stop	During running	
1113								
1115	TRK. CIR. ERROR	—	—	Off	Flicker	Stop	At power ON/ At reset	
1116	TRK. CIR. ERROR	—	—	Off	Flicker	Stop	During running	
1150	RAM ERROR	—	—	Off	Flicker	Stop	At power ON/ At reset	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALM LED is displayed at BATTERY ERROR.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	1112	A tracking hardware fault was detected during running. • The tracking cable was disconnected and reinserted without the standby system being powered off or reset.	- Start after checking that the tracking cable is connected. - If the same error is displayed again, the cause is the hardware fault of the tracking cable or CPU module. (Please contact your local Mitsubishi representative, explaining a detailed description of the problem.) - Confirm the redundant system startup procedure, and execute a startup again. For details, refer to the QnPRHCPU User's Manual (Redundant System).	QnPRH
	1113	• The tracking cable is not secured by the connector fixing screws. • The error occurred at a startup since the redundant system startup procedure was not followed.		
	1115	A fault was detected by the initial check of the tracking hardware.	This suggests a CPU module hardware fault. (Contact your nearest Mitsubishi representative.)	
	1116	A tracking hardware fault was detected during running. • The tracking cable was disconnected and reinserted without the standby system being powered off or reset. • The tracking cable is not secured by the connector fixing screws. • The error occurred at a startup since the redundant system startup procedure was not followed.	- Start after checking that the tracking cable is connected. - If the same error is displayed again, the cause is the hardware fault of the tracking cable or CPU module. (Please contact your local Mitsubishi representative, explaining a detailed description of the problem.) - Confirm the redundant system startup procedure, and execute a startup again. For details, refer to the QnPRHCPU User's Manual (Redundant System).	
	1150	The memory of the CPU module in the Multiple CPU high speed transmission area is faulty.	- Take noise reduction measures. - Reset the CPU module and RUN it again. If the same error is displayed again, the CPU module has hardware failure. Contact your local Mitsubishi representative, explaining a detailed description of the problem.	QnU*10

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1160	RAM ERROR	—	—	Off	Flicker	Stop	At program execution	
1161							At program execution	
1162							At power ON/ At reset	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALM LED is displayed at BATTERY ERROR.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	1160	The program memory in the CPU module is overwritten.	• Take noise reduction measures. • Format the program memory, write all files to the PLC, then reset the CPU module, and RUN it again. If the same error is displayed again, the CPU module has hardware failure. Contact your local Mitsubishi representative, explaining a detailed description of the problem.	QnU
	1161	The data of the device memory built in the CPU module is overwritten.	• Take noise reduction measures. If the same error is displayed again, the CPU module has hardware failure. Contact your local Mitsubishi representative, explaining a detailed description of the problem.	
	1162	The error of the data held by the battery in the CPU module is detected. (It occurs when the automatic format is not set.)	• Take noise reduction measures. • Change the CPU main body or SRAM card battery. If the same error is displayed again, the CPU module has hardware failure. Contact your local Mitsubishi representative, explaining a detailed description of the problem.	

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1200	OPE. CIRCUIT ERR.	—	—	Off	Flicker	Stop	At power ON/ At reset	
1201								
1202								
1203	OPE. CIRCUIT ERR.	—	—	Off	Flicker	Stop	When an END instruction executed	
1204								
1205								
1206	OPE. CIRCUIT ERR.	—	—	Off	Flicker	Stop	When instruction executed	
1300	FUSE BREAK OFF	Module No. (Slot No.) [For Remote I/O network] Network No./ Station No.	—	Off/ On	Flicker/ On	Stop/ Continue ^{*1}	Always	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALARM LED is displayed at BATTERY ERROR.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	1200	The operation circuit for index modification in the CPU module does not operate normally.	This suggests a CPU module hardware fault. (Contact your local Mitsubishi representative.)	○
	1201	The hardware (logic) in the CPU module does not operate normally.		
	1202	The operation circuit for sequence processing in the CPU module does not operate normally.		
	1203	The operation circuit for index modification in the CPU module does not operate normally.		Q4AR QnPRH
	1204	The hardware (logic) in the CPU module does not operate normally.		
	1205	The operation circuit for sequence processing in the CPU module does not operate normally.		
	1206	The DSP operation circuit in the CPU module does not operate normally.		Q4AR
1300		There is an output module with a blown fuse.	• Check FUSE. LED of the output modules and replace the module whose LED is lit. (The module with a blown fuse can also be identified using GX Developer. Check the special registers SD1300 to SD1331 to see if the bit corresponding to the module is "1".) • When a GOT is bus-connected to the main base unit or extension base unit, check the connection status of the extension cable and the earth status of the GOT.	Qn(H) QnPH QnPRH QnU Rem
		There is an output module with a blown fuse.	Check ERR. LED of the output modules and replace the module whose LED is lit. (The module with a blown fuse can also be identified using GX Developer. Check the special registers SD130 to SD137 to see if the bit corresponding to the module is "1".)	Q00J/Q00/Q01

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1300	FUSE BREAK OFF	Module No. (Slot No.) [For Remote I/O network] Network No./ Station No.	—	Off/ On	Flicker/ On	Stop/ Continue ^{*1}	Always	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALM LED is displayed at BATTERY ERROR.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
1300		There is an output module with a blown fuse.	• Check ERR. LED of the output modules and replace the fuse of the module whose LED is lit. • Read the common information of the error using the peripheral device and replace the fuse at the output module corresponding to the numerical value (module No.) reading. Alternatively, monitor special registers SD1300 to SD1331 with the peripheral device and change the fuse of the output module whose bit has a value of "1". • When a GOT is bus-connected to the main base unit or extension base unit, check the connection status of the extension cable and the grounding status of the GOT.	QnA Q4AR
		• There is an output module with a blown fuse. • External power supply for output load is turned off or disconnected.	• Check ERR. LED of the output modules and replace the module whose LED is lit. • Read the common information of the error using the peripheral device and replace the fuse at the output module corresponding to the numerical value (module No.) reading. Alternatively, monitor special registers SD1300 to SD1331 with the peripheral device and change the fuse of the output module whose bit has a value of "1". • Check whether the external power supply for output load is ON or OFF. • When a GOT is bus-connected to the main base unit or extension base unit, check the connection status of the extension cable and the earth status of the GOT.	Q2AS

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1310	I/O INT. ERROR	—	—	Off	Flicker	Stop	During interrupt	
1311								
1401	SP. UNIT DOWN	Module No. (Slot No.)	—	Off/ On	Flicker/ On	Stop/ Continue ^{*2}	At power ON/ At reset/When intelligent function module is accessed	
				Off	Flicker	Stop ^{*2}	At power ON/ At reset	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALARM LED is displayed at BATTERY ERROR.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	1310	An interruption has occurred although there is no interrupt module.	Any of the mounted modules is experiencing a hardware fault. Therefore, check the mounted modules and change the faulty module. (Contact your local Mitsubishi representative.)	○
	1311	An interrupt request from other than the interrupt module was detected.	Take action so that an interrupt will not be issued from other than the interrupt module.	Q00J/Q00/ Q01 ^{*4} QnU
		An interrupt request from the module where interrupt pointer setting has not been made in the PLC parameter dialog box was detected.	• Correct the interrupt pointer setting in the PLC system setting of the PLC parameter dialog box. • Take measures so that an interrupt is not issued from the module where the interrupt pointer setting in the PLC system setting of the PLC parameter dialog box has not been made. Correct the interrupt setting of the network parameter. Correct the interrupt setting of the intelligent function module buffer memory. Correct the basic program of the QD51.	Q00J/Q00/ Q01 ^{*5} QnPRH QnU
	1401	• There was no response from the intelligent function module/special function module in the initial processing. • The size of the buffer memory of the intelligent function module/special function module is invalid. • The unsupported module is mounted.	When the unsupported module is mounted, remove it. When the corresponding module is supported, this suggests the intelligent function module/special function module, CPU module and/or base unit is expecting a hardware fault (Contact your local Mitsubishi representative.)	QCPU Rem
		When PLC parameter I/O allocation was being made, there was no return signal from the special function module during initial processing stage.(When error is generated, the head I/O number of the special function module that corresponds to the common information is stored.)	The CPU module, base unit and/or the special function module that was accessed is experiencing a hardware fault. (Contact your local Mitsubishi representative.)	QnA

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1402	SP. UNIT DOWN	Module No. (Slot No.)	Program error location	Off/On	Flicker/On	Stop/Continue ^{*2}	When an intelligent function module access instruction is executed	
				Off	Flicker	Stop	During execution of FROM/TO instruction set	
1403	SP. UNIT DOWN	Module No. (Slot No.)	—	Off/On	Flicker/On	Stop/Continue ^{*2}	When an END instruction executed	
				Off/On	Flicker/On	Stop/Continue ^{*2}	Always	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALM LED is displayed at BATTERY ERROR.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	1402	The intelligent function module/special function module was accessed in the program, but there was no response.	This suggests the intelligent function module/special function module , CPU module and/or base unit is expecting a hardware fault (Contact your local Mitsubishi representative.)	QCPU Rem
		The special function module was accessed during the execution of a FROM/TO instruction set, but there was no response. (When an error is generated, the program error location corresponding to the individual information is stored.)	The CPU module, base unit and/or the special function module that was accessed is experiencing a hardware fault.(Contact your local Mitsubishi representative.)	QnA
	1403	• The unsupported module is mounted.	When the unsupported module is mounted, remove it. When the corresponding module is supported, this suggests the intelligent function module/special function module , CPU module and/or base unit is expecting a hardware fault (Contact your local Mitsubishi representative.)	QCPU
		• There was no response from the intelligent function module/special function module when the END instruction is executed. • An error is detected at the intelligent function module/special function module. • The I/O module (intelligent function module/special function module) is nearly removed, completely removed, or mounted during running.	The CPU module, base module and/or the intelligent function module/special function module that was accessed is experiencing a hardware fault. (Contact your local Mitsubishi representative.)	QCPU Rem

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1411	CONTROL-BUS. ERR.	Module No. (Slot No.)	–	Off	Flicker	Stop	At power ON/ At reset	
1412	CONTROL-BUS. ERR.	Module No. (Slot No.)	Program error location	Off	Flicker	Stop	During execution of FROM/TO instruction set	
1413	CONTROL-BUS. ERR.	–	–	Off	Flicker	Stop	Always	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALM LED is displayed at BATTERY ERROR.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	1411	When performing a parameter I/O allocation the intelligent function module/special function module could not be accessed during initial communications. (On error occurring, the head I/O number of the corresponding intelligent function module/special function module is stored in the common information.)	Reset the CPU module and RUN it again. If the same error is displayed again, the intelligent function module/special function module, CPU module or base unit is faulty. (Contact your local Mitsubishi representative.)	○ Rem
	1412	The FROM/TO instruction is not executable, due to a control bus error with the intelligent function module/special function module. (On error occurring, the program error location is stored in the individual information.)		○
	1413	In a multiple CPU system, a CPU module incompatible with the multiple CPU system is mounted.	- Remove the CPU module incompatible with the multiple CPU system from the main base unit, or replace the CPU module incompatible with the multiple CPU system with a CPU module compatible with the multiple CPU system. - The intelligent function module, CPU module or base unit is faulty. (Contact your local Mitsubishi representative.)	Q00J/Q00/ Q01 ^{*4} Qn(H) ^{*4} QnPH
		An error is detected on the system bus. - Self-diagnosis error of the system bus. - Self-diagnosis error of the CPU module	Reset the CPU module and RUN it again. If the same error is displayed again, the intelligent function module, CPU module or base unit is faulty. (Contact your local Mitsubishi representative.)	QCPU Rem

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1414	CONTROL-BUS. ERR.	Module No. (Slot No.)	—	Off	Flicker	Stop	Always	
1415	CONTROL-BUS. ERR.	Module No. (Slot No.)	—	Off	Flicker	Stop	When an END instruction executed	
							At power-ON/ At reset/ When an END instruction executed	
1416	CONTROL-BUS. ERR.	Module No. (Slot No.)	—	Off	Flicker	Stop	At power ON/ At reset	
1417	CONTROL-BUS. ERR.	—	—	Off	Flicker	Stop	Always	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALM LED is displayed at BATTERY ERROR.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	1414	- Fault of a loaded module was detected. - In a multiple CPU system, a CPU module incompatible with the multiple CPU system is mounted.	- Remove the CPU module incompatible with the multiple CPU system from the main base unit, or replace the CPU module with a CPU module compatible with the multiple CPU system. - Reset the CPU module and RUN it again. If the same error is displayed again, the intelligent function module, CPU module or base unit is faulty. (Contact your local Mitsubishi representative.)	Q00J/Q00/ Q01*4 Qn(H)*4 QnPH QnU
		An error is detected on the system bus.	Reset the CPU module and RUN it again. If the same error is displayed again, the intelligent function module, CPU module or base unit is faulty. (Contact your local Mitsubishi representative.)	Q00J/Q00/ Q01*4 Qn(H) QnPH QnPRH QnU Rem
	1415	Fault of the main or extension base unit was detected.	Reset the CPU module and RUN it again. If the same error is displayed again, the intelligent function module, CPU module or base unit is faulty. (Contact your local Mitsubishi representative.)	Q00J/Q00/Q01 Qn(H)*4 QnPH QnPRH QnU Rem
	1416	System bus fault was detected at power-on or reset.		Qn(H)*4 QnPH QnU
		In a multiple CPU system, a bus fault was detected at power-on or reset.		Q00/Q01*4 QnU
	1417	A reset signal error was detected on the system bus.	Reset the CPU module and RUN it again. If the same error is displayed again, the intelligent function module, CPU module or base unit is faulty. (Contact your local Mitsubishi representative.)	QnPRH

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1418	CONTROL-BUS.ERR.	—	—	Off	Flicker	Stop	At power-ON/ At reset/ At Switching execution	
1421	SYS. UNIT DOWN	—	—	Off	Flicker	Stop	Always	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALM LED is displayed at BATTERY ERROR.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	1418	In the redundant system, at power-on/ reset or switching system, the control system cannot access the extension base unit since it failed to acquire the access right.	Reset the CPU module and RUN it again. If the same error is displayed again, the CPU module, the Q6□WRB, or hardware of extension cable is faulty. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	QnPRH ^{*9}
	1421	Hardware fault at the system management module AS92R.	This suggests a system management module AS92R hardware fault. (Contact your local Mitsubishi representative.)	Q4AR

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1430	MULTI-C.BUS ERR.	—	—	Off	Flicker	Stop	At power ON/ At reset	
1431		Module No. (CPU No.)						
1432								
1433	MULTI-C.BUS ERR.	Module No. (CPU No.)	—	Off	Flicker	Stop	Always	
1434								
1435								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALM LED is displayed at BATTERY ERROR.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	1430	The error of host CPU is detected in the Multiple CPU high speed bus.	Reset the CPU module and RUN it again. If the same error is displayed again, the CPU module has hardware failure. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	QnU*10
	1431	The communication error with other CPU is detected in the Multiple CPU high speed bus.	• Take noise reduction measures. • Check the main base unit mounting status of the CPU module. • Reset the CPU module and RUN it again. If the same error is displayed again, the CPU module has hardware failure. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	
	1432	The communication time out with other CPU is detected in the Multiple CPU high speed bus.	Reset the CPU module and RUN it again. If the same error is displayed again, the CPU module has hardware failure. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	
	1433	The communication error with other CPU is detected in the Multiple CPU high speed bus.	• Take noise reduction measures. • Check the main base unit mounting status of the CPU module. • Reset the CPU module and RUN it again. If the same error is displayed again, the CPU module has hardware failure. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	
	1434			
	1435			

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1436	MULTI-C.BUS ERR.	—	—	Off	Flicker	Stop	At power ON/ At reset	
1437								
1439	MULTI-C.BUS ERR.	—	—	Off	Flicker	Stop	At power ON/ At reset	
1500	AC/DC DOWN	—	—	On	Off	Continue	Always	
1510	DUAL DC DOWN 5V	—	—	On	On	Continue	Always	
	SINGLE PS. DOWN	Base No./ Power supply No.	—	On	On	Continue	Always	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALM LED is displayed at BATTERY ERROR.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	1436	The error of the Multiple CPU high speed main base unit is detected. (The error of the Multiple CPU high speed bus is detected.)	Reset the CPU module and RUN it again. If the same error is displayed again, the CPU module has hardware failure. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	QnU* ¹⁰
	1437		• Take noise reduction measures. • Check the main base unit mounting status of the CPU module. • Reset the CPU module and RUN it again. If the same error is displayed again, the CPU module has hardware failure. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	
	1439	An error of the multiple CPU high speed main base unit was detected. (An error of the multiple CPU high speed bus was detected.)	Reset the CPU module and run it again. If the same error is displayed again, the CPU module has hardware failure. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	
	1500	• A momentary power supply interruption has occurred. • The power supply went off.	Check the power supply.	○ Rem
	1510	The power supply voltage (100 to 240VAC) of either of the two power supply modules on the power supply duplexing extension base unit dropped to or below 85% of the rated voltage. (This can be detected from the control system of the redundant system.)	Check the supply voltage of the power supply module. If the voltage is abnormal then replace the power supply module.	Q4AR
		The voltage of one power supply module dropped on the redundant base unit.	Check the power supplied to the redundant power supply modules mounted on the redundant base unit.	Qn(H)* ⁶ QnPH* ⁶ QnPRH Rem

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
1520	DC DOWN 5V	—	—	Off	Flicker	Stop	Always	
	SINGLE PS. ERROR	Base No./ Power supply No.	—	On	On	Continue	Always	
1530	DC DOWN 24V	—	—	On	On	Continue	Always	
1600	BATTERY ERROR*3	Drive Name	—	On	Off	Continue	Always	
1601								
1602					On			
1610	FLASH ROM ERROR	—	—	On	On	Continue	When writing to ROM	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 In the QCPU except for remote I/O module, either error stop or continue can be selected for each intelligent function module by the parameters.

*3 BAT.ALARM LED is displayed at BATTERY ERROR.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	1520	The voltage(100 to 240VAC) of the power supply module on the extension base unit dropped to or below 85% of the rated voltage. (This can be detected from the control system of the stand-alone system or redundant system.)	Check the supply voltage of the power supply module. If the voltage is abnormal then replace the power supply module.	Q4AR
		A fault of one redundant power supply module was detected in the redundant power supply system.	Hardware fault of the redundant power supply module. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	Qn(H) ^{*6} QnPH ^{*6} QnPRH Rem
	1530	The 24 VDC power supplied to the system management module AS92R has dropped below 90% of the rated voltage. (This can be detected from the control system or standby system of the redundant system.)	Check the 24VDC power supplied to the system management module AS92R.	Q4AR
	1600	- The battery voltage in the CPU module has dropped below stipulated level. - The lead connector of the CPU module battery is not connected.	- Change the battery. - If the battery is for program memory, standard RAM or for the back-up power function, install a lead connector.	○
	1601	Voltage of the battery on memory card 1 has dropped below stipulated level.	Change the battery.	QnA Qn(H) QnPH QnPRH QnU
	1602	Voltage of the battery on memory card 2 has dropped below stipulated level.	Change the battery.	QnA
	1610	The number of writing to flash ROM (standard ROM and system securement area) exceeds 100,000 times. (Number of writings >100,000 times)	Change the CPU module.	QnU

*4 Function version is B or later.

*5 Function version is A.

*6 The module whose first 5 digits of serial No. is 04101 or later.

*7 The module whose first 5 digits of serial No. is 07032 or later.

*8 The module whose first 5 digits of serial No. is 08032 or later.

*9 The module whose first 5 digits of serial No. is 09012 or later.

*10 The Universal model QCPU except the Q02UCPU.

22.3.4 Error code list (2000 to 2999)

The following shows the error messages from the error code 2000 to 2999, the contents and causes of the errors, and the corrective actions for the errors.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2000	UNIT VERIFY ERR.	Module No. (Slot No.) [For Remote I/O network] Network No./ Station No.	—	Off/ On	Flicker/ On	Stop/ Continue ^{*1}	When an END instruction executed	
2001	UNIT VERIFY ERR.	Module No. (CPU No.)	—	Off/ On	Flicker/ On	Stop/ Continue ^{*2}	When an END instruction executed	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	2000	In a multiple CPU system, a CPU module incompatible with the multiple CPU system is mounted.	Replace the CPU module incompatible with the multiple CPU system with a CPU module compatible with the multiple CPU system.	Qn(H) ^{*3} QnPH
		The I/O module status is different from the I/O module information at power ON. • I/O module (or intelligent function module) is not installed properly or installed on the base unit.	Read the error common information at the GX Developer, and check and/or change the module that corresponds to the numerical value (module number) there. Alternatively, monitor special registers SD150 to SD157 using GX Developer, and check and replace the module where the bit of its data is "1".	Q00J/Q00/Q01
		I/O module information power ON is changed. • I/O module (or intelligent function module/special function module) not installed properly or installed on the base unit.	• Read the common information of the error using the peripheral device, and check and/or change the module that corresponds to the numerical value (module number) there. • Alternatively, monitor the special registers SD1400 to SD1431 at a peripheral device, and change the fuse at the output module whose bit has a value of "1". • When a GOT is bus-connected to the main base unit or extension base unit, check the connection status of the extension cable and the grounding status of the GOT.	QnA Qn(H) QnPH QnPRH QnU Rem
	2001	During operation, a module was mounted on the slot where the empty setting of the CPU module was made.	During operation, do not mount a module on the slot where the empty setting of the CPU module was made.	Q00J/Q00/ Q01 ^{*3} QnU

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2010	BASE LAY ERROR	Base No.	—	Off	Flicker	Stop	At power ON/ At reset	
2011								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	2010	• More than applicable number of extension base units have been used. • When a GOT was bus-connected, the CPU module was reset while the power of the GOT was OFF.	• Use the allowable number of extension base units or less. • Power on the PLC and GOT again.	Q00J/Q00/ Q01 ^{*3} QnPRH Q02U
	2011	The QA1S6□B or QA6□B was used as the base unit.	Do not use the QA1S6□B or QA6□B as the base unit.	Q00J/Q00/ Q01 ^{*3} QnPRH QnU

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2012	BASE LAY ERROR	Base No.	—	Off	Flicker	Stop	At power ON/ At reset	
2013								
2020	EXT.CABLE ERR.	—	—	Off	Flicker	Stop	At power-ON/ At reset/ When an END instruction executed	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	2012	The GOT is bus-connected to the main base unit of the redundant system. The following errors are detected in the CPU redundant system compatible with the extension base unit. • The base unit other than the Q6□WRB is connected to the extension stage No.1. • The base unit is connected to any one of the extension stages No.2 to No.7, although the Q6□WRB does not exist in the extension stage No.1. • The other system CPU module is incompatible with the extension base unit. • The Q5□B, QA1S6□B, or QA6□B is connected. • The number of slots of the main base unit for both systems is different. Information of the Q6□WRB cannot be read correctly.	• Remove a bus connection cable for GOT connection connected to the main base unit. • Use the Q6□WRB (fixed to the extension stage No.1) • Use the CPU module compatible with the extension base unit for the other system. • Do not use the Q5□B, QA1S6□B, or QA6□B for the base unit. • Use the main base unit which has the same number of slots. • Hardware failure of the Q6□WRB. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	QnPRH*6
	2013	Stage number of the Q6□WRB is recognized as other than extension stage No.1 in the redundant system.	Hardware failure of the Q6□WRB. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	
	2020	The following errors are detected in the redundant system. • At power-on/reset, the standby system has detected the error in the path between the control system and the Q6□WRB. • The standby system has detected the error in the path between the host system CPU and the Q6□WRB at END processing.	Check to see if the extension cable between the main base unit and the Q6□WRB is connected correctly. If not, connect it after turning OFF the main base unit where the extension cable will be connected. If the cable is connected correctly, hardware of the CPU module, Q6□WRB, or extension cable is faulty. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2100	SP. UNIT LAY ERR.	Module No. (Slot No.)	—	Off	Flicker	Stop	At power ON/ At reset	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
2100		The slot to which the QI60 is mounted is set to other than Inteli (intelligent function module) or Interrupt (interrupt module) in the I/O assignment of PLC parameter.	Make setting again to match the PLC parameter I/O assignment with the actual loading status.	Qn(H) ^{*3} QnPH QnPRH
		• In the I/O assignment setting of PLC parameter, Inteli (intelligent function module) was allocated to an I/O module or vice versa. • In the I/O assignment setting of PLC parameter, a module other than CPU (or nothing) was allocated to the location of a CPU module or vice versa. • In the I/O assignment setting of the PLC parameter, switch setting was made to the module that has no switch setting. • In the I/O assignment setting of the PLC parameter dialog box, the number of points assigned to the intelligent function module is less than the number of points of the mounted module.	• Make the PLC parameter's I/O assignment setting again so it is consistent with the actual status of the intelligent function module and the CPU module. • Delete the switch setting in the I/O assignment setting of the PLC parameter.	Qn(H) QnPH QnPRH QnU Rem
		• In the parameter I/O allocation settings, an Inteli (intelligent function module) was allocated to a location reserved for an I/O module or vice versa. • In the parameter I/O allocation settings, a module other than CPU (or nothing) was allocated to a location reserved for a CPU module or vice versa. • In the I/O assignment setting of the PLC parameter dialog box, the number of points assigned to the intelligent function module is less than the number of points of the mounted module.	Reset the parameter I/O allocation setting to conform to the actual status of the intelligent function module and the CPU module.	Q00J/Q00/Q01

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2100	SP. UNIT LAY ERR.	Module No. (Slot No.)	—	Off	Flicker	Stop	At power ON/ At reset	
2101	SP. UNIT LAY ERR.	Module No. (Slot No.)	—	Off	Flicker	Stop	At power ON/ At reset	
2102								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	2100	In PLC parameter I/O allocation settings, a special function module was allocated to a location reserved for an I/O module. Or, the opposite has happened.	Reset the PLC parameter I/O allocation setting to conform with the actual status of the special function modules.	QnA
	2101	13 or more A-series special function modules (except for the A1SI61) that can initiate an interrupt to the CPU module have been installed.	Reduce the A series special function modules (except the A1SI61) that can make an interrupt start to the CPU module to 12 or less.	Qn(H)
		13 or more special function modules (not counting the A(1S)I61) capable of sending an interrupt to the CPU module have been installed.	Keep the number of special function modules that can initiate an interrupt (with the exception of the A(1S)I61 module) to 12 or fewer.	QnA
	2102	Seven or more A1SD51S have been installed.	Keep the number of A1SD51S to six or fewer.	Qn(H)
		Seven or more serial communication modules (excludes A (1S) J71QC24) have been installed.	Keep the number of serial communication modules (excludes A(1S)J71QU24) installed to six or fewer.	QnA

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2103	SP. UNIT LAY ERR.	Module No. (Slot No.)	—	Off	Flicker	Stop	At power ON/ At reset	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
2103		- Two or more QI60/A1SI61 modules are mounted in a single CPU system. - Two or more QI60/A1SI61 modules are set to the same control CPU in a multiple CPU system. - Two or more A1SI61 modules are loaded in a multiple CPU system.	- Reduce the number of QI60/A1SI61 modules mounted in the single CPU system to one. - Change the number of QI60/A1SI61 modules set to the same control CPU to only one in the multiple CPU system. - Reduce the number of A1SI61 modules to only one in the multiple CPU system. When using an interrupt module with each QCPU in a multiple CPU system, replace it with the QI60. (Use one A1SI61 module + max. three QI60 modules or only the QI60 modules.)	Qn(H) ^{*3} QnPH
		Two or more QI60, A1SI61 interrupt modules have been mounted.	Install only 1 QI60, A(1S)I61 module.	Qn(H) QnPRH
		The QI60 is mounted.	Remove the QI60.	Rem
		Two or more A1SI61 interrupt modules have been mounted.	Install only 1 AI61 module.	QnA
		Two or more QI60 modules are mounted.	Reduce the QI61 modules to one.	Q00J/Q00/ Q01 ^{*5}
		Two or more QI60 modules where interrupt pointer setting has not been made are mounted.	- Reduce the QI60 modules to one. - Make interrupt pointer setting to the second QI60 module and later.	Q00J/Q00/ Q01 ^{*3} QnU

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2104	SP. UNIT LAY ERR.	Module No. (Slot No.)	—	Off	Flicker	Stop	At power ON/ At reset	
2105								
2106	SP.UNIT LAY ERR.	Module No.	—	Off	Flicker	Stop	At power ON/ At reset	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU																	
	2104	At the MELSECNET/MINI auto refresh network parameter settings, the module allocation that was set is different from the actual module models at the station numbers in the link system.	Reset the network parameter MELSECNET/MINI auto refresh unit module allocation setting so that it conforms to the station number of the module that is actually linked.	QnA																	
	2105	There are too many special function modules that can use dedicated instructions allocated (number of modules installed). (The total of the figures indicated below is above 1344.) <table><tr><td>(AD59</td><td>modules installed × 5)</td></tr><tr><td>(AD57(S1)/AD58</td><td>modules installed × 8)</td></tr><tr><td>(AJ71C24(S3/S6/S8)</td><td>modules installed × 10)</td></tr><tr><td>(AJ71UC24</td><td>modules installed × 10)</td></tr><tr><td>(AJ71C21(S1)</td><td>modules installed × 29)</td></tr><tr><td>(AJ71PT32-S3/AJ71T32-S3</td><td>modules installed × 125) *</td></tr><tr><td>(AJ71QC24(R2,R4)</td><td>modules installed × 29)</td></tr><tr><td>(AJ71ID1(2)-R4</td><td>modules installed × 8)</td></tr><tr><td>+(AD75</td><td>modules installed × 12)</td></tr></table> total > 1344 *: When the expansion mode is used.	(AD59		modules installed × 5)	(AD57(S1)/AD58	modules installed × 8)	(AJ71C24(S3/S6/S8)	modules installed × 10)	(AJ71UC24	modules installed × 10)	(AJ71C21(S1)	modules installed × 29)	(AJ71PT32-S3/AJ71T32-S3	modules installed × 125) *	(AJ71QC24(R2,R4)	modules installed × 29)	(AJ71ID1(2)-R4	modules installed × 8)	+(AD75	modules installed × 12)
(AD59	modules installed × 5)																				
(AD57(S1)/AD58	modules installed × 8)																				
(AJ71C24(S3/S6/S8)	modules installed × 10)																				
(AJ71UC24	modules installed × 10)																				
(AJ71C21(S1)	modules installed × 29)																				
(AJ71PT32-S3/AJ71T32-S3	modules installed × 125) *																				
(AJ71QC24(R2,R4)	modules installed × 29)																				
(AJ71ID1(2)-R4	modules installed × 8)																				
+(AD75	modules installed × 12)																				
	2106	• Three or more MELSECNET/H and MELSECNET/G modules in total are mounted in the entire system. • Three or more Ethernet interface modules are mounted in the entire system.	• Reduce the MELSECNET/H and MELSECNET/G modules up to two or less in the entire system. • Reduce the Ethernet interface modules up to two or less in the entire system.	Q02U																	
		• Five or more MELSECNET/H and MELSECNET/G modules in total are mounted in the entire system. • Five or more Ethernet interface modules are mounted in the entire system.	• Reduce the MELSECNET/H and MELSECNET/G modules up to four or less in the entire system. • Reduce the Ethernet interface modules up to four or less in the entire system.	QnU ^{*7}																	
		• Three or more MELSECNET/G modules are mounted in the entire system. • Five or more MELSECNET/H and MELSECNET/G modules in total are mounted in the entire system.	• Reduce the MELSECNET/G modules up to two or less in the entire system. • Reduce the total number of the MELSECNET/H and MELSECNET/G modules up to four or less in the entire system.	Qn(H) ^{*6}																	

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2106	SP. UNIT LAY ERR.	Module No. (Slot No.)	—	Off	Flicker	Stop	At power ON/ At reset	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
2106		• Five or more MELSECNET/H modules have been installed. • Five or more Q series Ethernet interface modules have been installed.	• Reduce the number of MELSECNET/H modules to four or less. • Reduce the number of Q series Ethernet modules to four or less.	Qn(H) QnPH QnPRH Rem
		• Two or more MELSECNET/H modules were installed. • Two or more Q series Ethernet modules were installed. • Three or more Q series CC-Link modules were installed.	• Reduce the MELSECNET/H modules to one or less. • Reduce the Q series Ethernet modules to one or less. • Reduce the Q series CC-Link modules to two or less.	Q00J/Q00/Q01
		• The same network number or same station number is duplicated in the MELSECNET/H network system.	• Check the network number and station number.	QCPU Rem
		• Five or more AJ71QLP21 & AJ71QBR11 modules are installed. • Three or more AJ71AP21/R21 & AJ71AT21B modules are installed. • The total number of installed AJ71QLP21, AJ71QBR11, AJ71AP21/R21, and AJ71AT21B modules exceeds five. • The same network numbers or identical station numbers exist in the MELSECNET/10 network system. • Two or more master or load stations exist simultaneously at the MELSECNET(II) or MELSECNET/B data link system.	• Reduce the AJ71QLP21 and AJ71QBR11 modules to four or less. • Reduce the AJ71AP21/R21 and AJ71AT21B modules to two or less. • Reduce the AJ71QLP21, AJ71QBR11, AJ71AP21/R21 and AJ71AT21B modules to a total of four or less. • Check the network Nos. and station Nos. • Check the station Nos.	QnA

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2107	SP. UNIT LAY ERR.	Module No. (Slot No.)	—	Off	Flicker	Stop	At power ON/ At reset	
2108								
2109						Stop/ Continue ^{*2}		
2110	SP. UNIT ERROR	Module No. (Slot No.)	Program error location	Off/ On	Flicker/ On	Stop/ Continue ^{*1}	When instruction executed	
2111								

^{*1} CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

^{*2} Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	2107	The start X/Y set in the PLC parameter's I/O assignment settings is overlapped with the one for another module.	Make the PLC parameter's I/O assignment setting again so it is consistent with the actual status of the intelligent function module/special function modules.	○ Rem
	2108	- Network module A1SJ71LP21, A1SJ71BR11, A1SJ71AP21, A1SJ71AR21, or A1SJ71AT21B dedicated for the A2USCPU has been installed. - Network module A1SJ71QLP21 or A1SJ71QBR11 dedicated for the Q2AS has been installed.	Replace the network module to MELSECNET/H module.	Qn(H)
		A(1S)J71LP21 or A(1S)J71BR11 for use with the AnUCPU network module has been installed.	Replace the network module to A(1S)J71QLP21 or A(1S)J71QBR11.	QnA
	2109	The control system and standby system module configurations are different when a redundant system is in the backup mode.	Check the module configuration of the standby system.	Q4AR
	2110	- The location designated by the FROM/TO instruction set is not the intelligent function module/special function module. - The module that does not include buffer memory has been specified by the FROM/TO instruction. - The intelligent function module/special function module, Network module being accessed is faulty. - Station not loaded was specified using the instruction whose target was the CPU share memory.	- Read the individual information of the error using the GX Developer, check the FROM/TO instruction that corresponds to that numerical value (program error location), and correct when necessary. - The intelligent function module/special function module that was accessed is experiencing a hardware fault. Therefore, change the faulty module. Alternatively, contact your local Mitsubishi representative.	Q00J/Q00/Q01 Qn(H) ^{*3} QnPH QnPRH QnU
	2111	- The location designated by a link direct device (J□\□) is not a network module. - The I/O module (intelligent function module/special function module) was nearly removed, completely removed, or mounted during running.		○

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2112	SP. UNIT ERROR	Module No. (Slot No.)	Program error location	Off/On	Flicker/On	Stop/Continue ^{*1}	When instruction executed/ STOP → RUN	
2113	SP. UNIT ERROR	FFFF _H (fixed)	Program error location	Off/On	Flicker/On	Stop/Continue ^{*2}	When instruction executed/ STOP → RUN	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	2112	- The module other than special function module is specified by the special function module dedicated instruction. Or, it is not the corresponding special function module. - The module model specified by the special function module dedicated instruction and that specified by the parameter I/O assignment is different.	- Read the individual information of the error using a peripheral device, and check the special function module dedicated instruction (network instruction) that corresponds to the value (program error part) to make modification. - Set the module model by PLC parameter I/O assignment according to the special function module dedicated instruction setting. Example) Although AJ71QC24N is used actually, AJ71QC24 is set.	QnA
		- The module other than intelligent function module/special function module is specified by the intelligent function module/special function module dedicated instruction. Or, it is not the corresponding intelligent function module/special function module. - There is no network No. specified by the network dedicated instruction. Or the relay target network does not exit.	Read the individual information of the error using a peripheral device, and check the special function module / special function module dedicated instruction (network instruction) that corresponds to the value (program error part) to make modification.	QCPU Rem
	2113	The module other than network module is specified by the network dedicated instruction.		QnA Qn(H) QnPH

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2114	SP. UNIT ERROR	Module No. (Slot No.)	Program error location	Off/ On	Flicker/ On	Stop/ Continue	When instruction executed/ STOP → RUN	
2115								
2116								
2117								
2118							When instruction executed	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	2114	An instruction, which on execution specifies other stations, has been used for specifying the host CPU. (An instruction that does not allow the host CPU to be specified).	Read the individual information of the error using the GX Developer, check the program corresponding that value (program error location), and make correction.	Q00J/Q00/ Q01 ^{*3} Qn(H) ^{*3} QnPH QnU
	2115	An instruction, which on execution specifies the host CPU, has been used for specifying other CPUs. (An instruction that does not allow other stations to be specified).		Q00J/Q00/ Q01 ^{*3} Qn(H) ^{*3} QnPH
	2116	- An instruction that does not allow the .under the control of another CPU to be specified is being used for a similar task. - Instruction was executed for the A or QnA module under control of another CPU.		Q00J/Q00/ Q01 ^{*3} Qn(H) ^{*3} QnPH QnU
	2117	A CPU module that cannot be specified in the instruction dedicated to the multiple CPU system was specified.		Q00J/Q00/ Q01 ^{*3} Qn(H) ^{*3} QnPH QnU
	2118	When the online module change setting is set to be "enabled" in the PLC parameter in a multiple CPU system, intelligent function module controlled by other CPU using the FROM instruction/ intelligent function module device (U□\G□) is specified.	- When performing the online module change in a multiple CPU system, correct the program so that access will not be made to the intelligent function module controlled by the other CPU. - When accessing the intelligent function module controlled by the other CPU in a multiple CPU system, set the online module change setting to be "disabled" by parameter.	Qn(H) ^{*3} QnPH QnU

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2120	SP. UNIT LAY ERR.	—	—	Off	Flicker	Stop	At power ON/ At reset	
2121								
2122								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	2120	The locations of the Q5□B/Q6□B and QA1S6□B/QA6□B are improper.	Check the location of the base unit.	Q00J/Q00/ Q01 ^{*4} Qn(H) QnPH
	2121	The CPU module is installed to other than the CPU slot and slots 0 to 2.	Check the loading position of the CPU module and reinstall it at the correct slot.	Qn(H) QnPH Rem
	2122	The QA1S6□B/QA6□B are used for the main base unit.	Replace the main base unit with a usable one.	Qn(H) QnPH QnPRH Rem

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2124	SP. UNIT LAY ERR.	—	—	Off	Flicker	Stop	At power ON/ At reset	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
2124		• A module is mounted on the 65th slot or later slot. • A module is mounted on the slot whose number is greater than the number of slots specified at [Slots] in [Standard setting] of the base setting. • A module is mounted on the slot whose number of I/O points exceeds 4096 points. • A module is mounted on the slot whose number of I/O points strides 4096 points.	• Remove the module mounted on the 65th slot or later slot. • Remove the module mounted on the slot whose number is greater than the number of slots specified at [Slots] in [Standard setting] of the base setting. • Remove the module mounted on the slot whose number of I/O points exceeds 4096 points. • Replace the module with the one whose number of occupied points does not exceed 4096 points.	Qn(H) QnPH QnPRH QnU*7 Rem
		• A module is mounted on the 37th slot or later slot. • A module is mounted on the slot whose number is greater than the number of slots specified at [Slots] in [Standard setting] of the base setting. • A module is mounted on the slot whose number of I/O points exceeds 2048 points. • A module is mounted on the slot whose number of I/O points strides 2048 points.	• Remove the module mounted on the 37th slot or later slot. • Remove the module mounted on the slot whose number is greater than the number of slots specified at [Slots] in [Standard setting] of the base setting. • Remove the module mounted on the slot whose number of I/O points exceeds 2048 points. • Replace the module with the one whose number of occupied points does not exceed 2048 points.	Q02U
		• A module is mounted on the 25th slot or later slot. (The 17th slot or later slot for the Q00J.) • A module is mounted on the slot whose number is greater than the number of slots specified at [Slots] in [Standard setting] of the base setting. • A module is mounted on the slot whose number of I/O points exceeds 1024 points. (256 points for the Q00J.) • A module is mounted on the slot whose number of I/O points strides 1024 points. (256 points for the Q00J.)	• Remove the module mounted on the 25th slot or later slot. (The 17th slot or later slot for the Q00J.) • Remove the module mounted on the slot whose number is greater than the number of slots specified at [Slots] in [Standard setting] of the base setting. • Remove the module mounted on the slot whose number of I/O points exceeds 1024 points. (256 points for the Q00J.) • Replace the module with the one whose number of occupied points does not exceed 1024 points. (256 points for the Q00J.)	Q00J/Q00/Q01
		5 or more extension base units were added. (3 bases for Q00J)	Remove 5 or more extension base units. (3 bases for Q00J)	Q00J/Q00/ Q01*4

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2125	SP. UNIT LAY. ERR.	Module No. (Slot No.)	—	Off	Flicker	Stop	At power ON/ At reset	
2126								
2128	SP.UNIT LAY ERR.	Module No.	—	Off	Flicker	Stop	At power-ON/ At reset	
2150	SP. UNIT VER. ERR.	Module No. (Slot No.)	—	Off	Flicker	Stop	At power ON/ At reset/ At PLC writing	
2151								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	2125	• A module which the QCPU cannot recognise has been installed. • There was no response from the intelligent function module/special function module.	• Install a usable module. • The intelligent function module/special function module is experiencing a hardware fault. (Contact your local Mitsubishi representative.)	QCPU Rem
	2126	CPU module locations in a multiple CPU system are either of the following. • There are empty slots between the QCPU and QCPU/motion controller. • A module other than the High Performance model QCPU/Process CPU (including the motion controller) is mounted on the left-hand side of the High Performance model QCPU/Process CPU.	• Mount modules on the available slots so that the empty slots will be located on the right-hand side of the CPU module.) • Remove the module mounted on the left-hand side of the High Performance model QCPU/Process CPU, and mount the High Performance model QCPU/Process CPU on the empty slot. Mount the motion CPU on the right-hand side of the High Performance model QCPU/Process CPU.	Qn(H) ^{*3} QnPH
	2128	The unusable module is mounted on the extension base unit in the redundant system.	• Remove the unusable module from the extension base unit.	QnPRH ^{*6}
	2150	In a multiple CPU system, the control CPU of the intelligent function module incompatible with the multiple CPU system is set to other than CPU No.1.	• Change the intelligent function module for the one compatible with the multiple CPU system (function version B). • Change the setting of the control CPU of the intelligent function module incompatible with the multiple CPU system to CPU No.1.	Q00J/Q00/ Q01 QnPH QuU
	2151	Either of the following modules incompatible with the redundant system has been mounted in a redundant system. • MELSECNET/H • Ethernet	Use either of the following modules compatible with the redundant system. • MELSECNET/H • Ethernet	QnPRH

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2200	MISSING PARA.	Drive Name	–	Off	Flicker	Stop	At power ON/ At reset/ STOP→RUN	
2210	BOOT ERROR	Drive name	–	Off	Flicker	Stop	At power ON/ At reset	
2211								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	2200	There is no parameter file in the drive specified as valid parameter drive by the DIP switches.	• Check and correct the valid parameter drive settings made by the DIP switches. • Set the parameter file to the drive specified as valid parameter drive by the DIP switches.	Qn(H) QnPH QnPRH
		There is no parameter file at the program memory.	Set the parameter file to the program memory.	Q00J/Q00/Q01
		Parameter file does not exist in all drives where parameters will be valid.	Set a parameter file in a drive to be valid.	QuU
	2210	The contents of the boot file are incorrect.	Check the boot setting.	Q00J/Q00/ Q01 ^{*3} Qn(H) QnPH QnPRH QnU
		There is no boot file in the drive designated by the parameter enabled drive switch even though the Boot DIP switch is ON.	Check and correct the valid parameter drive settings made by the DIP switches. Set the boot file to the drive specified by the parameter drive DIP switches.	QnA
	2211	File formatting is failed at a boot.	• Reboot. • CPU module hardware fault. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	Qn(H) QnPRH QnU

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2220	RESTORE ERROR	—	—	Off	Flicker	Stop	At power ON/ At reset	
2221								
2300	ICM. OPE. ERROR	Drive name	—	Off/ On	Flicker/ On	Stop/ Continue ^{*1}	When memory card is inserted or removed	
2301								
2302								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	2220	The device information (number of points) backed up by the device data backup function is different from the number of device points of the PLC parameter. After this error occurred, perform restore per power-on/reset until the number of device points is identical to the number of device points in the PLC parameter, or until the backup data is deleted.	- Set the number of device points at the time of backup to the device point setting in [PLC parameter]. Then, turn ON from OFF power supply, or reset the CPU and cancel reset. - Delete the backed up data, and turn ON from OFF power supply, or reset the CPU and cancel reset.	QnU
	2221	The device information backed up by the device data backup function is incomplete. (Turning power supply OFF or reset is suspected.) Do not return the data when this error occurs. Also, delete the incomplete device information at the time of this error occurrence.	Reset the CPU module and run it again.	QnU
	2300	- A memory card was removed without switching the memory card in/out switch OFF. - The memory card in/out switch is turned ON although a memory card is not actually installed.	- Remove memory card after placing the memory card in/out switch OFF. - Turn on the card insert switch after inserting a memory card.	QnA Qn(H) QnPH QnPRH QnU
	2301	- The memory card has not been formatted. - Memory card format status is incorrect. - The QCPU file does not exist in the Flash card.	- Format memory card. - Reformat memory card. - Write the QCPU file to the Flash card.	
		SRAM card failure is detected. (It occurs when automatic format is not set.)	Format SRAM card after changing battery of SRAM card.	QnU
	2302	A memory card that cannot be used with the CPU module has been installed.	- Format memory card. - Reformat memory card. - Check memory card.	QnA Qn(H) QnPH QnPRH QnU

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2400	FILE SET ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power ON/ At reset/ At PLC writing	

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
2400		Automatic write to standard ROM was performed on the CPU module that is incompatible with automatic write to standard ROM. (Memory card where automatic write to standard ROM was selected in the boot file was fitted and the parameter enable drive was set to the memory card.)	• Execute automatic write to standard ROM on the CPU module which is compatible with automatic write to standard ROM. • Using GX Developer, perform write of parameters and programs to standard ROM. • Change the memory card for the one where automatic write to standard ROM has not been set, and perform boot operation from the memory card.	Qn(H) ^{*3} QnPH QnPRH
		The file designated at the PLC file settings in the parameters cannot be found.	• Read the individual information of the error using peripheral device, check to be sure that the parameter drive name and file name correspond to the numerical values there (parameter number), and correct. • Create a file created using parameters, and load it to the CPU module.	○
		The Ethernet parameter that was added for QnACPU, with the function version "B," has been set to QnACPU without the function version "B."	Change to QnACPU with the function version "B". Delete the Ethernet parameter.	QnA

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2401	FILE SET ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power ON/ At reset/ At PLC writing	
2402								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	2401	Program memory capacity was exceeded by performing boot operation or automatic write to standard ROM.	• Check and correct the parameters (boot setting). • Delete unnecessary files in the program memory.	Qn(H) ^{*3} QnPH QnPRH
		Program memory capacity was exceeded by performing boot operation.		QnU
		The file specified by parameters cannot be made.	• Choose "Clear program memory" for boot in the parameter so that boot is started after the program memory is cleared.	○
		Although setting is made to use the device data storage file, there is no empty capacity required for creating the device data storage file in the standard ROM.	• Read the individual information of the error using the peripheral device, check to be sure that the parameter drive name and file name correspond to the numerical values there (parameter number), and correct. • Check the space remaining in the memory card.	
	2402	Though the file register has been set in the pairing setting/tracking setting, the file register does not exist.	Secure the empty capacity of the standard ROM. Confirm the file register and parameter.	QnU Q4AR

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2410	FILE OPE. ERROR	File name/ Drive name	Program error location	Off/ On	Flicker/ On	Stop/ Continue ^{*1}	When instruction executed	
2411								
2412								
2413								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	2410	- The specified program does not exist in the program memory. This error may occur when the ECALL, EFCALL, PSTOP, PSCAN, POFF or PLOW instruction is executed. - The specified file does not exist.	- Read the individual information of the error using the peripheral device, check to be sure that the program corresponds to the numerical values there (program location), and correct. Create a file created using parameters, and load it to the CPU module. - In case a specified file does not exist, write the file to a target memory and/or check the file specified with the instruction again.	QnA Qn(H) QnPH QnPRH QnU
	2411	- The file is the one which cannot be specified by the sequence program (such as comment file). - The specified program exists in the program memory, but has not been registered in the program setting of the Parameter dialog box. This error may occur when the ECALL, EFCALL, PSTOP, PSCAN or POFF instruction is executed.	Read the individual information of the error using the peripheral device, check to be sure that the program corresponds to the numerical values there (program location), and correct.	
	2412	The SFC program file is one that cannot be designated by the sequence program.	Read the individual information of the error using the peripheral device, check to be sure that the program corresponds to the numerical values there (program location), and correct.	QnA Qn(H) QnPH QnPRH QnU
	2413	No data has been written to the file designated by the sequence program.	Read the individual information of the error using the peripheral device, check to be sure that the program corresponds to the numerical values there (program location), and correct. Check to ensure that the designated file has not been write protected.	QnA Qn(H) QnPH QnPRH

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
2500	CAN'T EXE. PRG.	File name/ Drive name	—	Off	Flicker	Stop	At power ON/ At reset	
2501								
2502								
2503								
2504								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 Either error stop or continue can be selected for each module by the parameters.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	2500	- There is a program file that uses a device that is out of the range set in the PLC parameter device setting. - After the PLC parameter setting is changed, only the parameter is written into the PLC.	- Read the common information of the error using the peripheral device, check to be sure that the parameter device allocation setting and the program file device allocation correspond to the numerical values there (file name), and correct if necessary. - If PLC parameter device setting is changed, batch-write the parameter and program file into the PLC.	○
		After the index modification of the PLC parameter is changed, only the parameter is written to the PLC.	When the index modification of the PLC parameter is changed, batch-write the parameter and program file into the PLC.	QnU
	2501	There are multiple program files although "none" has been set at the PLC parameter program settings.	Edit the PLC parameter program setting to "yes". Alternatively, delete unneeded programs.	QnA Qn(H) QnPH QnPRH QnU
		- There are three or more program files. - The program name differs from the program contents.	- Delete unnecessary program files. - Match the program name with the program contents.	Q00J/Q00/Q01
	2502	The program file is incorrect. Alternatively, the file contents are not those of a sequence program.	Check whether the program version is * * *.QPG, and check the file contents to be sure they are for a sequence program.	○
		The program file is not the one for the redundant CPU.	Create a program using GX Developer or PX Developer for which the PLC type has been set to the redundant CPU (Q12PRH/Q25PRH), and write it to the CPU module.	QnPRH
	2503	There are no program files at all.	- Check program configuration. - Check parameters and program configuration.	○
	2504	Two or more SFC normal programs or control programs have been designated.		QnA Qn(H) QnPH QnPRH QnU
		There are two or more SFC programs.		Q00J/Q00/ Q01*3

*3 The function version is B or later.

*4 The function version is A.

*5 The module whose first 5 digits of serial No. is 04101 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

22.3.5 Error code list (3000 to 3999)

The following shows the error messages from the error code 3000 to 3999, the contents and causes of the errors, and the corrective actions for the errors.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
3000	PARAMETER ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power ON/ At reset/ STOP→RUN/ At PLC writing	
3001								

*1 The function version is B or later.

*2 Parameter No. is the value gained by dividing the head I/O number of parameter in the intelligent function module set by GX Configurator by 10H.

Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
3000	In a multiple CPU system, the intelligent function module under control of another CPU is specified in the interrupt pointer setting of the PLC parameter.	- Specify the head I/O number of the intelligent function module under control of the host CPU. - Delete the interrupt pointer setting of the parameter.	Qn(H) ^{*1} QnPH QnU
	The PLC parameter settings for timer time limit setting, the RUN-PAUSE contact, the common pointer number, general data processing, number of empty slots, system interrupt settings, baud rate setting, and service processing setting are outside the range that can be used by the CPU module.	- Read the individual information of the error using the peripheral device, check the parameter item corresponding to the numerical value (parameter No.), and correct it. - Rewrite corrected parameters to the CPU module, reload the CPU power supply and/or reset the module. - If the same error occurs, it is thought to be a hardware error. (Contact your local Mitsubishi representative.)	○ Rem
	In a program memory check, the check capacity has not been set within the range applicable for the CPU module.		QnPH QnPRH ^{*4}
	The parameter settings in the error individual information (special register SD16) are illegal.		○
	The ATA card is set to the PLC card slot when the specified drive for the file register is set to "memory card ROM" and [Use the following file] or [Use the same file name as the program] (either one is allowed) is set in the PLC file setting.		QnU
3001	The parameter settings are corrupted.		○ Rem

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07032 or later.

*5 The MELSECNET/H module whose first 5 digits of serial No. is 08102 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
3002	PARAMETER ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power ON/ At reset/ STOP→RUN/ At PLC writing	
3003	PARAMETER ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	When an END instruction executed	
	PARAMETER ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power-On/ At reset/ STOP→RUN/ At PLC writing	
3004	PARAMETER ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power-On/ At reset/ STOP→RUN/ At PLC writing	

*1 The function version is B or later.

*2 Parameter No. is the value gained by dividing the head I/O number of parameter in the intelligent function module set by GX Configurator by 10H.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	3002	When "Use the following file" is selected for the file register in the PLC file setting of the PLC parameter dialog box, the specified file does not exist although the file register capacity has been set.	• Read the individual information of the error using the peripheral device, check the parameter item corresponding to the numerical value (parameter No.), and correct it. • Rewrite corrected parameters to the CPU module, reload the CPU power supply and/or reset the module. • If the same error occurs, it is thought to be a hardware error. (Contact your local Mitsubishi representative.)	QnA Qn(H) QnPH QnPRH
		When [Use the following file] is set for the file register in the PLC file setting of the PLC parameter dialog box and the capacity of file register is not set, the file register file does not exist in the specified target memory.		QnU
		When [Use the following file.] is set for the device data storage file in [PLC file] of [PLC parameter], and [Capacity] is not set, the device data storage file does not exist in the target memory.		QnU
	3003	The automatic refresh range of the multiple CPU system exceeded the file register capacity.	Change the file register file for the one refresh-enabled in the whole range.	Qn(H) ^{*1} QnPH QnU
		The number of devices set at the PLC parameter device settings exceeds the possible CPU module range.	• Read the individual information of the error using the peripheral device, check the parameter item corresponding to the numerical value (parameter No.), and correct it. • If the error is still generated following the correction of the parameter settings, the possible cause is the memory error of the CPU module's built-in RAM or program memory or the memory card. (Contact your local Mitsubishi representative.)	○
	3004	The parameter file is incorrect. Alternatively, the contents of the file are not parameters.	Check whether the parameter file version is * * * .QPA, and check the file contents to be sure they are parameters.	○

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07032 or later.

*5 The MELSECNET/H module whose first 5 digits of serial No. is 08102 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
3005	PARAMETER ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power-ON/ At reset/ STOP→RUN	
3006	PARAMETER ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power-On/ At reset/ STOP→RUN/ At PLC writing	
3007								
3009								

*1 The function version is B or later.

*2 Parameter No. is the value gained by dividing the head I/O number of parameter in the intelligent function module set by GX Configurator by 10H.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	3005	The contents of the parameter are broken.	• Read the individual information of the error using the peripheral device, check the parameter item corresponding to the numerical value (parameter No.), and correct it. • Write the modified parameter items to the CPU module again, and power-on the PLC or reset the CPU module. • When the same error occurs again, the hardware is faulty. Contact your local Mitsubishi representative, explaining a detailed description of the problem.	Qn(H) ^{*6}
	3006	• The high speed interrupt is set in a Q02CPU. • The high speed interrupt is set in a multiple CPU system. • The high speed interrupt is set when aQA1S6□B or QA6□B is used. • No module is installed at the I/O address designated by the high speed interrupt.	• Delete the setting of the Q02CPU's high speed interrupt. To use high speed interrupts, change the CPU module to one of the Q02H/Q06H/Q12H/Q25H CPU. • To use a multiple CPU system, delete the setting of the high-speed interrupt. To use high speed interrupts, change the system to a single CPU system. • To use either the QA1S6□B or QA6□B, delete the setting of the high speed interrupt. To use high speed interrupts, do not use the QA1S6□B/QA6□B. • Re-examine the I/O address designated by the high speed interrupt setting.	Qn(H) ^{*3}
	3007	The parameter file in the drive specified as valid parameter drive by the DIP switches is inapplicable for the CPU module.	Create parameters using GX Developer, and write them to the drive specified as valid parameter drive by the DIP switches.	QnPRH
	3009	In a multiple CPU system, the modules for AnS, A, Q2AS and QnA have been set to multiple control CPUs.	Re-set the parameter I/O assignment to control them under one CPU module. (Change the parameters of all CPUs in the multiple CPU system.)	Qn(H) ^{*1}

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07032 or later.

*5 The MELSECNET/H module whose first 5 digits of serial No. is 08102 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
3010	PARAMETER ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power-On/ At reset/ STOP→RUN/ At PLC writing	
3012								
3013	PARAMETER ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power-On/ At reset/ STOP→RUN/ At PLC writing	

*1 The function version is B or later.

*2 Parameter No. is the value gained by dividing the head I/O number of parameter in the intelligent function module set by GX Configurator by 10H.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	3010	The parameter-set number of CPU modules differs from the actual number in a multiple CPU system.	Match the number of (CPU modules in multiple CPU setting) - (CPUs set as empty in I/O assignment) with that of actually mounted CPU modules.	Qn(H) ^{*1} QnPH
	3012	Multiple CPU setting or control CPU setting differs from that of the reference CPU settings in a multiple CPU system.	Match the multiple CPU setting or control CPU setting in the PLC parameter with that of the reference CPU (CPU No.1) settings.	Q00/Q01 ^{*1} Qn(H) ^{*1} QnU
	3013	Multiple CPU auto refresh setting is any of the followings in a multiple CPU system. • When a bit device is specified as a refresh device, a number other than a multiple of 16 is specified for the refresh-starting device. • The device specified is other than the one that may be specified. • The number of send points is an odd number.	Check the following in the multiple CPU auto refresh setting and make correction. • When specifying the bit device, specify a multiple of 16 for the refresh starting device. • Specify the device that may be specified for the refresh device. • Set the number of send points to an even number.	Qn(H) ^{*1} QnPH
		In a multiple CPU system, the multiple CPU auto refresh setting is any of the following. • The total number of transmission points is greater than the maximum number of refresh points.	Check the following in the multiple CPU auto refresh setting and make correction. • The total number of transmission points is within the maximum number of refresh points.	Q00/Q01 ^{*1}
		In a multiple CPU system, the multiple CPU auto refresh setting is any of the following. • The device specified is other than the one that may be specified. • The number of send points is an odd number. • The total number of send points is greater than the maximum number of refresh points.	Check the following in the multiple CPU auto refresh setting and make correction. • Specify the device that may be specified for the refresh device. • Set the number of send points to an even number. • Set the total number of send points within the range of the maximum number of refresh points.	QnU

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07032 or later.

*5 The MELSECNET/H module whose first 5 digits of serial No. is 08102 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
3014	PARAMETER ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power-On/ At reset/ STOP→RUN/ At PLC writing	
3015	PARAMETER ERROR	File name/ Drive name	Parameter number/ CPU No.	Off	Flicker	Stop	At power-On/ At reset/ STOP→RUN/ At PLC writing	
3016	PARAMETER ERROR	File name/ Drive name	Parameter number/ CPU No.	Off	Flicker	Stop	At power ON/ At reset/ At PLC writing	
3040	PARAMETER ERROR	—	—	Off	Flicker	Stop	At power ON/ At reset	
3041								

*1 The function version is B or later.

*2 Parameter No. is the value gained by dividing the head I/O number of parameter in the intelligent function module set by GX Configurator by 10H.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	3014	- In a multiple CPU system, the online module change parameter (multiple CPU system parameter) settings differ from those of the reference CPU. - In a multiple CPU system, the online module change setting is enabled although the CPU module mounted does not support online module change parameter.	- Match the online module change parameter with that of the reference CPU. - If the CPU module that does not support online module change is mounted, replace it with the CPU module that supports online module change.	Qn(H) QnPH QnU
	3015	In a multiple CPU system configuration, the CPU verified is different from the one set in the parameter setting.	Read the individual information of the error using the peripheral device, check the parameter item corresponding to the numerical value (parameter No./CPU No.) and parameter of target CPU, and correct them.	QnU
	3016	The CPU module incompatible with multiple CPU synchronized boot-up is set as the target for the synchronized boot-up in the [Multiple CPU synchronous startup setting].	Delete the CPU module incompatible with multiple CPU synchronized boot-up from the setting.	QnU ^{*7}
	3040	The parameter file is damaged.	With GX Developer, write [PLC parameter/network parameter/remote password] to a valid drive then reload the power supply for system and/or reset the CPU module. If the same error occurs, it is thought to be hardware error. (Contact your local Mitsubishi representative.)	Qn(H) ^{*4} QnPH ^{*4} QnPRH ^{*4}
	3041	Parameter file of intelligent function module is damaged.	With GX Developer, write [Intelligent function module parameter] to a valid drive to write the parameters then reload the power supply for system and/or reset the CPU module. If the same error occurs, it is thought to be a hardware error. (Contact your local Mitsubishi representative.)	Qn(H) ^{*4} QnPH ^{*4} QnPRH ^{*4}

^{*3} The module whose first 5 digits of serial No. is 04012 or later.

^{*4} The module whose first 5 digits of serial No. is 07032 or later.

^{*5} The MELSECNET/H module whose first 5 digits of serial No. is 08102 or later.

^{*6} The module whose first 5 digits of serial No. is 09012 or later.

^{*7} The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
3042	PARAMETER ERROR	—	—	Off	Flicker	Stop	At power ON/ At reset	
3100	LINK PARA. ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power-ON/ At reset/ STOP→RUN	

*1 The function version is B or later.

*2 Parameter No. is the value gained by dividing the head I/O number of parameter in the intelligent function module set by GX Configurator by 10H.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	3042	The system file that have stored the remote password setting information is damaged.	• With GX Developer, write [PLC parameter/network parameter/remote password] to a valid drive then reload the power supply for system and/or reset the CPU module. If the same error occurs, it is thought to be a hardware error. (Contact your local Mitsubishi representative.) • When a valid drive for parameter is set to other than [program memory], set the parameter file (PARAM) at the boot file setting to be able to transmit to the program memory. With GX Developer, write [PLC parameter/network parameter/remote password] to a valid drive then reload the power supply for system and/or reset the CPU module. If the same error occurs, it is thought to be hardware error. (Contact your local Mitsubishi representative.)	Qn(H) ^{*4} QnPH ^{*4} QnPRH ^{*4}
	3100	In a multiple CPU system, the MELSECNET/G module controlled by another CPU is specified as the head I/O number of the MELSECNET/G module.	• Delete the net work parameter of the MELSECNET/G module controlled by another CPU. • Change the setting to the head I/O number of the MELSECNET/G module controlled by host CPU.	Qn(H) ^{*6} QnU
		The network parameter of the MELSECNET/G operating as the normal station is overwritten to the control station. Or, the network parameter of the MELSECNET/G operating as the control station is overwritten to the normal station. (The network parameter is updated on the module by resetting.)	Reset the CPU module.	

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07032 or later.

*5 The MELSECNET/H module whose first 5 digits of serial No. is 08102 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
3100	LINK PARA. ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power-ON/ At reset/ STOP→RUN	

*1 The function version is B or later.

*2 Parameter No. is the value gained by dividing the head I/O number of parameter in the intelligent function module set by GX Configurator by 10H.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	3100	• The number of actually mounted modules is different from the number of modules set in the network parameter of the MELSECNET/G. • The head I/O number of the actually mounted module is different from the one set in the network parameter of the MELSECNET/G. • Data cannot be handled in the parameter exists. • The network type of MELSECNET/G is overwritten during power-on. (When changing the network type, switch RESET to RUN.)	• Check the network parameter and actual mounting status, and if they differ, make them matched. When network parameters are modified, write them to the CPU module. • Check the setting of extension base unit stage number. • Check the connection status of extension base unit and extension cable. When the GOT is bus-connected to the main base unit or extension base unit, also check its connection status. If an error occurs even after performing the above checks, the hardware may be faulty. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	Qn(H) ^{*6} QnU
		• The MELSECNET/G module is specified for the head I/O number of network parameter in the MELSECNET/H. • The MELSECNET/H module is specified for the head I/O number of network parameter in the MELSECNET/G.		
		• Although the MELSECNET/G module is mounted, network parameter for the MELSECNET/G module is not set. • Although the MELSECNET/G and MELSECNET/H modules are mounted, network parameter for the MELSECNET/H module is not set.		

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07032 or later.

*5 The MELSECNET/H module whose first 5 digits of serial No. is 08102 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
3100	LINK PARA. ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power ON/ At reset/ STOP→RUN	

*1 The function version is B or later.

*2 Parameter No. is the value gained by dividing the head I/O number of parameter in the intelligent function module set by GX Configurator by 10h.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
3100		In a multiple CPU system, the MELSECNET/H under control of another CPU is specified as the head I/O number in the network setting parameter of the MELSECNET/H.	- Delete the MELSECNET/H network parameter of the MELSECNET/H under control of another CPU. - Change the setting to the head I/O number of the MELSECNET/H under control of the host CPU.	Q00/Q01 ^{*1} Qn(H) ^{*1} QnPH QnU
		The network parameter of the MELSECNET/H operating as the normal station is overwritten to the control station. Or, the network parameter of the MELSECNET/H operating as the control station is overwritten to the normal station. (The network parameter is updated on the module by resetting.)	Reset the CPU module.	Qn(H) ^{*1} QnPH QnPRH QnU
		- The number of actually installed modules is different from that designated in the number of modules setting parameter of MELSECNET/H. - The head I/O number of actually installed modules is different from that designated in the network parameter of MELSECNET/H. - Some data in the parameters cannot be handled. - The network type of MELSECNET/H is overwritten during power-on. (When changing the network type, switch RESET to RUN.) - The mode switch of MELSECNET/H module^{*5} is outside the range.	- Check the network parameters and actual mounting status, and if they differ, make them matched. If any network parameter has been corrected, write it to the CPU module. - Check the extension base unit stage No. setting. - Check the connection status of the extension base units and extension cables. When the GOT is bus-connected to the main base unit and extension base units, also check the connection status. If the error occurs after the above checks, the possible cause is a hardware fault. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.) - Set the mode switch of MELSECNET/H module^{*5} within the range.	QCPU
		Although the QnACPU is a control station or master station, the network parameters have not been written.	- Correct and write the network parameters. - If the error occurs after correction, it suggests a hardware fault. (Contact your local Mitsubishi representative.)	QnA

^{*3} The module whose first 5 digits of serial No. is 04012 or later.

^{*4} The module whose first 5 digits of serial No. is 07032 or later.

^{*5} The MELSECNET/H module whose first 5 digits of serial No. is 08102 or later.

^{*6} The module whose first 5 digits of serial No. is 09012 or later.

^{*7} The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
3101	LINK PARA. ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	When an END instruction executed	
	LINK PARA. ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power ON/ At reset/ STOP→RUN	

*1 The function version is B or later.

*2 Parameter No. is the value gained by dividing the head I/O number of parameter in the intelligent function module set by GX Configurator by 10H.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
		The link refresh range exceeded the file register capacity.	Change the file register file for the one that enables entire range refresh.	Qn(H) ^{*1} QnPH QnPRH QnU
		- When the station number of the MELSECNET/H module is 0, the inter-PLC network parameter setting has been made. - When the station number of the MELSECNET/H module is other than 0, the remote master parameter setting has been made.	Correct the type or station number of the MELSECNET/H module in the network parameter to meet the used system.	Qn(H) ^{*1} QnPH QnPRH
		The refresh parameter for the MELSECNET/G is outside the range.	Check the network parameters and mounting status, and if they differ, match the network parameters and mounting status.	Qn(H) ^{*6} QnU
	3101	- The network No. specified by a network parameter is different from that of the actually mounted network. - The head I/O No. specified by a network parameter is different from that of the actually mounted I/O unit. - The network class specified by a network parameter is different from that of the actually mounted network. - The network refresh parameter of the MELSECNET/H, MELSECNET/10 is out of the specified area.	- If any network parameter has been corrected, write it to the CPU module. - Confirm the setting of the number of extension stages of the extension base units. - Check the connection status of the extension base units and extension cables. When the GOT is bus-connected to the main base unit and extension base units, also check their connection status. If the error occurs after the above checks, the cause is a hardware fault. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	○
		A multi-remote I/O network was configured using a module that does not support the MELSECNET/H multi-remote I/O network.	Use a module that supports the MELSECNET/H multi-remote I/O network.	QnPH
		- The system A of the MELSECNET/H remote master station has been set to other than Station No. 0. - The system B of the MELSECNET/H remote master station has been set to Station No. 0.	- Set the system A of the MELSECNET/H remote master station to Station No. 0. - Set the system B of the MELSECNET/H remote master station to any of Station No. 1 to 64.	QnPRH

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07032 or later.

*5 The MELSECNET/H module whose first 5 digits of serial No. is 08102 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
3102	LINK PARA. ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power ON/ At reset/ STOP→RUN	

*1 The function version is B or later.

*2 Parameter No. is the value gained by dividing the head I/O number of parameter in the intelligent function module set by GX Configurator by 10H.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
3102		A MELSECNET/G network parameter error was detected.	• Correct and write the network parameters. • If the error occurs after correction, it suggests a hardware fault. (Contact your local Mitsubishi representative.)	Qn(H) ^{*6} QnU
		• The network module detected a network parameter error. • A MELSECNET/H network parameter error was detected.		○
		The station No. specified in pairing setting are not correct. • The stations are not numbered consecutively. • Pairing setting has not been made for the CPU module at the normal station.	Refer to the troubleshooting of the network module, and if the error is due to incorrect pairing setting, reexamine the pairing setting of the network parameter.	QnPRH
		The MELSECNET/G module whose first 5 digits of serial No. is "09041" or earlier is mounted.	Mount the MELSECNET/G module whose first 5 digits of serial No. is "09042" or later.	QnU

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07032 or later.

*5 The MELSECNET/H module whose first 5 digits of serial No. is 08102 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
3103	LINK PARA. ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power ON/ At reset/ STOP→RUN	

*1 The function version is B or later.

*2 Parameter No. is the value gained by dividing the head I/O number of parameter in the intelligent function module set by GX Configurator by 10H.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
3103		In a multiple CPU system, the Q series Ethernet interface module under control of another station is specified to the start I/O number of the Ethernet network parameter.	- Delete the Ethernet network parameter of the Q series Ethernet interface module under control of another station. - Change the setting to the start I/O number of the Q series Ethernet interface module under control of the host station.	Q00/Q01 ^{*1} Qn(H) ^{*1} QnPH QnU
		- Although the number of modules has been set to one or greater number in the Ethernet module count parameter setting, the number of actually mounted module is zero. - The start I/O No. of the Ethernet network parameter differs from the I/O No. of the actually mounted module.	- Correct and write the network parameters. - If the error occurs after correction, it suggests a hardware fault. (Contact your local Mitsubishi representative.)	○ Rem
		- AJ71QE71 does not exist in the position of I/O number set by the parameter. - I/O number designation is overlapping. - Numbers of the network parameter and loaded AJ71QE71 are different. - Ethernet (parameter + dedicated instruction) is set to more than five.		QnA
		- Ethernet module whose network type is set to "Ethernet (main base)" is mounted on the extension base unit in the redundant system. - Ethernet module whose network type is set to "Ethernet (extension base)" is mounted on the main base unit in the redundant system.		QnPRH ^{*6}

^{*3} The module whose first 5 digits of serial No. is 04012 or later.

^{*4} The module whose first 5 digits of serial No. is 07032 or later.

^{*5} The MELSECNET/H module whose first 5 digits of serial No. is 08102 or later.

^{*6} The module whose first 5 digits of serial No. is 09012 or later.

^{*7} The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
3104	LINK PARA. ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power ON/ At reset/ STOP→RUN	
3105								

*1 The function version is B or later.

*2 Parameter No. is the value gained by dividing the head I/O number of parameter in the intelligent function module set by GX Configurator by 10h.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	3104	• The Ethernet, MELSECNET/H and MELSECNET/10 use the same network number. • The network number, station number or group number set in the network parameter is out of range. • The specified I/O number is outside the range of the used CPU module. • The Ethernet-specific parameter setting is not normal.	• Correct and write the network parameters. • If the error occurs after correction, it suggests a hardware fault. (Contact your local Mitsubishi representative.)	○ Rem
	3105	In a multiple CPU system, the Q series CC-Link module under control of another station is specified as the head I/O number of the CC-Link network parameter.	• Delete the CC-Link network parameter of the Q series CC-Link module under control of another station. • Change the setting to the start I/O number of the Q series CC-Link module under control of the host station.	Q00/Q01 ^{*1} Qn(H) ^{*1} QnPH QnU
		• Though the number of CC-Link modules set in the network parameters is one or more, the number of actually mounted modules is zero. • The start I/O number in the common parameters is different from that of the actually mounted module. • The station type of the CC-Link module count setting parameters is different from that of the actually mounted station.	• Correct and write the network parameters. • If the error occurs after correction, it suggests a hardware fault. (Contact your local Mitsubishi representative.)	○ Rem
		• CC-Link module whose station type is set to “master station (compatible with redundant function)” is mounted on the extension base unit in the redundant system. • CC-Link module whose station type is set to “master station” is mounted on the main base unit in the redundant system.		QnPRH ^{*6}
		The contents of the Ethernet parameter are incorrect.	Write after correcting parameters.	QnA

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07032 or later.

*5 The MELSECNET/H module whose first 5 digits of serial No. is 08102 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
3106	LINK PARA. ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	When an END instruction executed	
	LINK PARA. ERROR	File name	Parameter number	Off	Flicker	Stop	At power ON/ At reset/ STOP→RUN	
3107	LINK PARA. ERROR	File name	Parameter number	Off	Flicker	Stop	At power ON/ At reset/ STOP→RUN	
3200	SFC PARA. ERROR	File name	Parameter number	Off	Flicker	Stop	STOP→RUN	
3201								
3202								
3203								

*1 The function version is B or later.

*2 Parameter No. is the value gained by dividing the head I/O number of parameter in the intelligent function module set by GX Configurator by 10H.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	3106	The CC-Link link refresh range exceeded the file register capacity.	Change the file register file for the one refresh-enabled in the whole range.	Qn(H) ^{*1} QnPH QnPRH QnU
		The network refresh parameter for CC-Link is out of range.	Check the parameter setting.	QCPU Rem
	3107	- The CC-Link parameter setting is incorrect. - The set mode is not allowed for the version of the mounted CC-Link module.	Check the parameter setting.	○ Rem
	3200	The parameter setting is illegal. Though Block 0 was set to "Automatic start" in the SFC setting of the PLC parameter dialog box, Block 0 does not exist.	Read the common information of the error using the peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem.	QnA Q00J/Q00/ Q01 ^{*1} QnPH QnPRH QnU
	3201	The block parameter setting is illegal.		QnA Qn(H) QnPH QnPRH
	3202	The number of step relays specified in the device setting of the PLC parameter dialog box is less than that used in the program.		
	3203	The execution type of the SFC program specified in the program setting of the PLC parameter dialog box is other than scan execution.		QnA Qn(H) QnPH QnPRH QnU

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07032 or later.

*5 The MELSECNET/H module whose first 5 digits of serial No. is 08102 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
3300	SP. PARA ERROR	File name	Parameter number*2	Off	Flicker	Stop	At power-On/ At reset/ STOP→RUN/ At PLC writing	
3301								
3302								
3303	SP. PARA ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power-On/ At reset/ STOP→RUN/ At PLC writing	
3400	REMOTE PASS. ERR.	—	—	Off	Flicker	Stop	At power ON/ At reset/ STOP→RUN	

*1 The function version is B or later.

*2 Parameter No. is the value gained by dividing the head I/O number of parameter in the intelligent function module set by GX Configurator by 10H.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	3300	The start I/O number in the intelligent function module parameter set on GX Configurator differs from the actual I/O number.	Check the parameter setting.	QCPU Rem
	3301	The refresh setting of the intelligent function module exceeded the file register capacity.	Change the file register file for the one which allows refresh in the whole range.	Q00J/Q00/Q01 Qn(H) ^{*1} QnPH QnPRH QnU
		The intelligent function module's refresh parameter setting is outside the available range.	Check the parameter setting.	QCPU Rem
	3302	The intelligent function module's refresh parameter are abnormal.	Check the parameter setting.	QCPU
	3303	In a multiple CPU system, the automatic refresh setting or other parameter setting was made to the intelligent function module under control of another station.	- Delete the automatic refresh setting or other parameter setting of the intelligent function module under control of another CPU. - Change the setting to the automatic refresh setting or other parameter setting of the intelligent function module under control of the host CPU.	Q00/Q01 ^{*1} Qn(H) ^{*1} QnPH QnU
	3400	The head I/O number of the target module of the remote password is set to other than 0 _H to 0FF0 _H .	Change the head I/O number of the target module to be within the 0 _H to 0FF0 _H range.	Qn(H) ^{*1} QnPH QnPRH QnU ^{*7} Rem
		The head I/O number of the target module of the remote password is set to other than 0 _H to 07E0 _H .	Change the head I/O number of the target module to be within the 0 _H to 07E0 _H range.	Q02U
		The head I/O number of the target module of the remote password is outside the following range. • Q00JCPU: 0_H to 1E0_H • Q00CPU/Q01CPU: 0_H to 3E0_H	Change the head I/O number of the target module of the remote password for the number within the following range. • Q00JCPU: 0_H to 1E0_H • Q00CPU/Q01CPU: 0_H to 3E0_H	Q00J/Q00/ Q01 ^{*1}

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07032 or later.

*5 The MELSECNET/H module whose first 5 digits of serial No. is 08102 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
3401	REMOTE PASS. ERR.	—	—	Off	Flicker	Stop	At power ON/ At reset/ STOP→RUN	

*1 The function version is B or later.

*2 Parameter No. is the value gained by dividing the head I/O number of parameter in the intelligent function module set by GX Configurator by 10H.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
3401		Position specified as the head I/O number of the remote password file is incorrect due to one of the following reasons: • Module is not loaded. • Other than a the intelligent function module (I/O module) • Intelligent function module other than the Q series serial communication module, modem interface module or Ethernet module • Q series serial communication module or Ethernet module of function version A The intelligent function module where remote password is available is not mounted.	Mount the Q series serial communication module, modem interface module or Ethernet module of function version B or later in the position specified in the head I/O No. of the remote password file.	Qn(H) ^{*1} QnPH QnPRH QnU Rem
		Any of the following modules is not mounted on the slot specified for the head I/O number of the remote password. • Serial communication module of function version B or later • Ethernet module of function version B or later • Modem interface module of function version B or later	Mount any of the following modules in the position specified for the head I/O number of the remote password. • Serial communication module of function version B or later • Ethernet module of function version B or later • Modem interface module of function version B or later	Q00J/Q00/ Q01 ^{*1}
		The Q series serial communication module, modem interface module or Ethernet module of function version B or later controlled by another CPU was specified in a multiple CPU system.	• Change it for the Ethernet module of function version B or later connected by the host CPU. • Delete the remote password setting.	Qn(H) ^{*1} QnPH QnU

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07032 or later.

*5 The MELSECNET/H module whose first 5 digits of serial No. is 08102 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

22.3.6 Error code list (4000 to 4999)

The following shows the error messages from the error code 4000 to 4999, the contents and causes of the errors, and the corrective actions for the errors.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
4000	INSTRCT. CODE ERR	Program error location	—	Off	Flicker	Stop	At power ON/ At reset/ STOP→RUN When instruction executed	
4001								
4002								
4003								
4004								
4010	MISSING END INS.	Program error location	—	Off	Flicker	Stop	At power ON/ At reset/ STOP→RUN	
4020	CAN'T SET(P)	Program error location	—	Off	Flicker	Stop		
4021								
4030	CAN'T SET(I)	Program error location	—	Off	Flicker	Stop		

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 The function version is B or later.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	4000	- The program contains an instruction code that cannot be decoded. - An unusable instruction is included in the program.	Read the common information of the error using a peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem.	○
	4001	The program contains a dedicated instruction for SFC although it is not an SFC program.		QnA Q00J/Q00/ Q01 ^{*2} Qn(H) QnPH QnPRH QnU
	4002	- The name of dedicated instruction specified by the program is incorrect. - The dedicated instruction specified by the program cannot be executed by the specified module.		○ Rem
	4003	The number of devices for the dedicated instruction specified by the program is incorrect.		
	4004	The device which cannot be used by the dedicated instruction specified by the program is specified.		
	4010	There is no END (FEND) instruction in the program.		○
	4020	The total number of internal file pointers used by the program exceeds the number of internal file pointers set in the parameters.		QnA Qn(H) QnPH QnPRH QnU
	4021	- The common pointer Nos. assigned to files overlap. - The local pointer Nos. assigned to files overlap.		○
	4030	The allocation pointer Nos. assigned by files overlap.		

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07012 or later.

*5 The module whose first 5 digits of serial No. is 07032 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
4100	OPERATION ERROR	Program error location	—	Off/On	Flicker/On	Stop/Continue ^{*1}	When instruction executed	
4101								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 The function version is B or later.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	4100	The instruction cannot process the contained data.	Read the common information of the error using the peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem.	○ Rem
		Access error of ATA card occurs by FREAD/FWRITE instructions.	• Take measurements against noise. • Reset and restart the CPU module. When the same error is displayed again, the ATA card has hardware failure. (Please consult your local Mitsubishi service center or representative, explaining a detailed description of the problem.)	Qn(H) QnPH QnPRH
	4101	• The number of setting data dealt with the instruction exceeds the applicable range. • The storage data and constant of the device specified by the instruction exceeds the applicable range. • When writing to the host CPU shared memory, the write prohibited area is specified for the write destination address. • The range of storage data of the device specified by the instruction is duplicated. • The device specified by the instruction exceeds the range of the number of device points. • The interrupt pointer No. specified by the instruction exceeds the applicable range.	Read the common information of the error using the peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem.	○ Rem
		• The storage data of file register specified by the instruction exceeds the applicable range. Or, file register is not set.		QnU

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07012 or later.

*5 The module whose first 5 digits of serial No. is 07032 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
4102	OPERATION ERROR	Program error location	—	Off/On	Flicker/On	Stop/Continue ^{*1}	When instruction executed	
4103								
4104								
4105								
4107								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 The function version is B or later.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
		In a multiple CPU system, the link direct device (J□\□) was specified for the network module under control of another station.	- Delete from the program the link direct device which specifies the network module under control of another CPU. - Using the link direct device, specify the network module under control of the host CPU.	Q00/Q01 ^{*2} Qn(H) ^{*2} QnPH QnU
	4102	- The network No. or station No. specified for the dedicated instruction is wrong. - The link direct device (J□\□) setting is incorrect. - The module No./ network No./number of character strings exceeds the range that can be specified.	Read the common information of the error using the peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem.	○ Rem
		The specification of character string (" ") specified by dedicated instruction cannot be used for the character string.		QnU
	4103	The configuration of the PID dedicated instruction is incorrect.		QnA Q00J/Q00/ Q01 ^{*2} Qn(H) QnPRH QnU
	4104	The number of settings is beyond the range.	Read the common information of the error using peripheral device, and check and correct the program corresponding to that value (program error location).	Q4AR
	4105	PLOADP/PUNLOADP/PSWAPP instructions were executed while setting program memory check.	- Delete the program memory check setting. - When using the program memory check, delete PLOADP/PUNLOADP/PSWAPP instructions.	QnPH ^{*5}
	4107	33 or more multiple CPU dedicated instructions were executed from one CPU module.	Using the multiple CPU dedicated instruction completion bit, provide interlocks to prevent one CPU module from executing 33 or more multiple CPU dedicated instructions.	Q00/Q01 ^{*2} Qn(H) ^{*2} QnPH Q02U
		Numbers of execution to the CC-Link instruction are beyond 32.	Set the numbers of execution to the CC-Link instruction to 32 or less.	QnA

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07012 or later.

*5 The module whose first 5 digits of serial No. is 07032 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
4108	OPERATION ERROR	Program error location	—	Off/On	Flicker/On	Stop/Continue ^{*1}	When instruction executed	
4109	OPERATION ERROR	Program error location	—	Off/On	Flicker/On	Stop/Continue ^{*1}	When instruction executed	
4111	OPERATION ERROR	Program error location	—	Off/On	Flicker/On	Stop/Continue ^{*2}	When instruction executed	
4112								
4113	OPERATION ERROR	Program error location	—	Off/On	Flicker/On	Stop/Continue	When instruction executed	
4120	OPERATION ERROR	Program error location	—	Off/On	Flicker/On	Stop/Continue ^{*2}	When instruction executed	
4121								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 The function version is B or later.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	4108	The CC-Link parameter is not set when the CC-Link instruction is executed.	Execute the CC-Link instruction after setting the CC-Link parameter.	QnA
	4109	With high speed interrupt setting PR, PRC, UDCNT1, UDCNT2, PLSY or PWM instruction is executed.	Delete the high-speed interrupt setting. When using high-speed interrupt, delete the PR, PRC, UDCNT1, UDCNT2, PLSY and PWM instructions.	Qn(H) ^{*3}
	4111	An attempt was made to perform write/read to/from the CPU shared memory write/read disable area of the host station CPU module with the instruction.	Read the common information of the error using GX Developer, and check and correct the error step corresponding to that value (program error location).	Q00/Q01 ^{*2} QnU
	4112	The CPU module that cannot be specified with the multiple CPU dedicated instruction was specified.		
	4113	- When the SP.DEVST instruction is executed, the number of writing to the standard ROM of the day exceeds the value specified by SD695. - The value outside the specified range is set to SD695.	- Check that the number of execution of the SP.DEVST instruction is proper. - Execute the SP.DEVST instruction again the following day or later day. Or, arrange the value of SD695. - Correct the value of SD695 so that it does not exceed the range.	QnU
	4120	Since the manual system switching enable flag (special register SM1592) is OFF, manual system switching cannot be executed by the control system switching instruction (SP. CONTSW).	To execute control system switching by the SP. CONTSW instruction, turn ON the manual system switching enable flag (special register SM1592).	QnPRH
	4121	- In the separate mode, the control system switching instruction (SP. CONTSW) was executed in the standby system CPU module. - In the debug mode, the control system switching instruction (SP. CONTSW) was executed.	- Reexamine the interlock signal for the SP. CONTSW instruction, and make sure that the SP. CONTSW instruction is executed in the control system only. (Since the SP. CONTSW instruction cannot be executed in the standby system, it is recommended to provide an interlock using the operation mode signal or like.) - As the SP. CONTSW instruction cannot be executed in the debug mode, reexamine the interlock signal related to the operation mode.	

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07012 or later.

*5 The module whose first 5 digits of serial No. is 07032 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
4122	OPERATION ERROR	Program error location	—	Off/On	Flicker/On	Stop/Continue	When instruction executed	
4130	OPERATION ERROR	Program error location	—	Off/On	Flicker/On	Stop/Continue ^{*2}	When END/other instruction executed	
4131	OPERATION ERROR	Program error location	—	Off/On	Flicker/On	Stop/Continue	When instruction executed	
4140	OPERATION ERROR	Program error location	—	OFF/On	Flicker/On	Stop/Continue ^{*2}	When instruction executed	
4141								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 The function version is B or later.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	4122	• The dedicated instruction was executed to the module mounted on the extension base unit in the redundant system. • The instruction for accessing the intelligent function module mounted on the extension base unit from the standby system at separate mode was executed.	• Delete the dedicated instruction for the module mounted on the extension base unit. • Delete the instruction for accessing the intelligent function module mounted on the extension base unit from the standby system.	QnPRH ^{*6}
	4130	Instructions to read SFC step comment (S(P).SFCSCOMR) and SFC transition condition comment (S(P).SFCTCOMR) are executed for the comment file in ATA card	Target comment file is to be other than the comment file in ATA card.	Qn(H) ^{*4} QnPH ^{*5} QnPRH
	4131	The SFC program is started up by the instruction while the other SFC program has not yet been completed.	Check the SFC program specified by the instruction. Or, check the executing status of the SFC program.	QnU
	4140	Operation where the input data is special value ("0", unnormalized number, nonnumeric, $\pm \infty$) is performed.	Read the common information of the error using the peripheral device, check the error step corresponding to the numerical value (program error part), and correct it.	QnU
	4141	Overflow occurs at operation.		

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07012 or later.

*5 The module whose first 5 digits of serial No. is 07032 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
4200	FOR NEXT ERROR	Program error location	—	Off	Flicker	Stop	When instruction executed	
4201	FOR NEXT ERROR	Program error location	—	Off	Flicker	Stop	When instruction executed	
4202								
4203								
4210	CAN'T EXECUTE(P)	Program error location	—	Off	Flicker	Stop	When instruction executed	
4211								
4212								
4213								
4220	CAN'T EXECUTE(I)	Program error location	—	Off	Flicker	Stop	When instruction executed	
4221								
4223								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 The function version is B or later.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	4200	No NEXT instruction was executed following the execution of a FOR instruction. Alternatively, there are fewer NEXT instructions than FOR instructions.	Read the common information of the error using the peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem.	○
	4201	A NEXT instruction was executed although no FOR instruction has been executed. Alternatively, there are more NEXT instructions than FOR instructions.		
	4202	More than 16 nesting levels are programmed.		
	4203	A BREAK instruction was executed although no FOR instruction has been executed prior to that.		
	4210	The CALL instruction is executed, but there is no subroutine at the specified pointer.	Read the common information of the error using the peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem.	○
	4211	There was no RET instruction in the executed subroutine program.		
	4212	The RET instruction exists before the FEND instruction of the main routine program.		
	4213	More than 16 nesting levels are programmed.	Keep nesting levels at 16 or under.	
	4220	Though an interrupt input occurred, the corresponding interrupt pointer does not exist.	Read the common information of the error using the peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem.	○
	4221	An IRET instruction does not exist in the executed interrupt program.		
	4223	The IRET instruction exists before the FEND instruction of the main routine program.		
		• The IRET instruction was executed in the fixed scan execution type program. • The STOP instruction was executed in the fixed scan execution type program.		

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07012 or later.

*5 The module whose first 5 digits of serial No. is 07032 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
4225	CAN'T EXECUTE(I)	—	—	Off	Flicker	Stop	At power-ON/ At reset	
4230	INST. FORMAT ERR.	Program error location	—	Off	Flicker	Stop	When instruction executed	
4231								
4235								
4300	EXTEND INST. ERR.	Program error location	—	Off/ On	Flicker/ On	Stop/ Continue ^{*1}	When instruction executed	
4301								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 The function version is B or later.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	4225	The interrupt pointer for the module mounted on the extension base unit is set in the redundant system.	Delete the setting of interrupt pointer for the module mounted on the extension base unit, since it cannot be used.	QnPRH* ⁶
	4230	The number of CHK and CHKEND instructions is not equal.	Read the common information of the error using the peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem.	QnA Qn(H) QnPH
	4231	The number of IX and IXEND instructions is not equal.		○
	4235	The configuration of the check conditions for the CHK instruction is incorrect. Alternatively, a CHK instruction has been used in a low speed execution type program.		QnA Qn(H) QnPH
	4300	The designation of a MELSECNET/ MINI-S3 master module control instruction was wrong.	Read the common information of the error using the peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem.	QnA
	4301	The designation of an AD57/AD58 control instruction was wrong.		

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07012 or later.

*5 The module whose first 5 digits of serial No. is 07032 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
4350	OPERATION ERROR	Program error location	–	OFF	Flicker	Stop	When instruction executed	
4351								
4352								
4353								
4354								
4355								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 The function version is B or later.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	4350	• The target CPU module specified by the dedicated instruction of Multiple CPU high speed bus specified by the program. • The reserved CPU is specified. • The uninstalled CPU is specified. • The head I/O number of the target CPU/16 (n1) is outside the range of 3EH to 3E3H. • The CPU module where the instruction cannot be executed is specified. • The instruction is executed in a single CPU system. • The host CPU is specified.	Read the common information of the error using the peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem.	QnU
	4351	• The dedicated instruction of Multiple CPU high speed bus specified by the program cannot be executed to the specified target CPU module. • The instruction name is wrong. • The instruction unsupported by the target CPU module is specified.		QnU ^{*7}
	4352	The number of devices for the dedicated instruction of Multiple CPU high speed bus specified by the program is wrong.		
	4353	The device which cannot be used for the dedicated instruction of Multiple CPU high speed bus specified by the program is specified.		QnU
	4354	The character string which cannot be handled by the dedicated instruction of Multiple CPU high speed bus is specified.		
	4355	The number of read/write data (number of request/receive data) for the dedicated instruction of Multiple CPU high speed bus specified by the program is not valid.		QnU ^{*7}

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07012 or later.

*5 The module whose first 5 digits of serial No. is 07032 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
4400	SFCP. CODE ERROR	Program error location	—	Off	Flicker	Stop	STOP→RUN	
4410	CAN'T SET(BL)	Program error location	—	Off	Flicker	Stop	STOP→RUN	
4411								
4420	CAN'T SET(S)	Program error location	—	Off	Flicker	Stop	STOP→RUN	
4421	CAN'T SET(S)	Program error location	—	Off	Flicker	Stop	STOP→RUN	
4422								
4423								
4430	SFC EXE. ERROR	File name/ Drive name	—	Off	Flicker	Stop	STOP→RUN	
4431								
4432								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 The function version is B or later.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	4400	No SFCP or SFCPEND instruction in SFC program.	Write the program to the CPU module again using GX Developer.	QnA Qn(H) QnPH QnPRH
	4410	The block number designated by the SFC program exceeds the range.		QnA Q00J/Q00/ Q01* ² Qn(H) QnPH QnPRH QnU
	4411	Block number designations overlap in SFC program.		
	4420	A step number designated in an SFC program exceeds the range.		QnA Q00J/Q00/ Q01* ² Qn(H) QnPH QnPRH QnU
	4421	Total number of steps in all SFC programs exceed the maximum.		
	4422	Step number designations overlap in SFC program.		
	4423	The total number of (maximum step No.+1) of each block exceeds the total number of step relays.	Correct the total number of step relays so that it does not exceed the total number of (maximum step No.+1) of each block.	Q00J/Q00/ Q01* ² QnU
	4430	The SFC program cannot be executed. • The data of the block data setting is illegal. • The SFC data device of the block data setting is beyond the device setting range set in the PLC parameter.	• Write the program to the CPU module again using GX Developer. • After correcting the setting of the SFC data device, write it to the CPU module. • After correcting the device setting range set in the PLC parameter, write it to the CPU module.	
	4431	The SFC program cannot be executed. • The block parameter setting is abnormal.	Write the program to the CPU module again using GX Developer.	
	4432	The SFC program cannot be executed. • The structure of the SFC program is illegal.		

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07012 or later.

*5 The module whose first 5 digits of serial No. is 07032 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
4500	SFCP. FORMAT ERR.	Program error location	—	Off	Flicker	Stop	STOP→RUN	
4501								
4502								
4503								
4504								
4505								
4506								
4600	SFCP. OPE. ERROR	Program error location	—	Off/ On	Flicker/ On	Stop/ Continue *1	When instruction executed	
4601								
4602								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 The function version is B or later.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	4500	The numbers of BLOCK and BEND instructions in an SFC program are not equal.	Write the program to the CPU module again using the peripheral device.	QnA Qn(H) QnPH QnPRH
	4501	The configuration of the STEP* to TRAN* to TSET to SEND instructions in the SFC program is incorrect.		QnA Q00J/Q00/ Q01* ² Qn(H) QnPH QnPRH QnU
	4502	The structure of the SFC program is illegal. • STEP1* instruction does not exist in the block of the SFC program.		
	4503	The structure of the SFC program is illegal. • The step specified in the TSET instruction does not exist. • In jump transition, the host step number was specified as the destination step number.	• Write the program to the CPU module again using GX Developer. • Read the common information of the error using GX Developer, and check and correct the error step corresponding to that value (program error location).	
	4504	The structure of the SFC program is illegal. • The step specified in the TAND instruction does not exist.	Write the program to the CPU module again using GX Developer.	
	4505	The structure of the SFC program is illegal. • In the operation output of a step, the SET Sn/BLmSn or RST Sn/BLmSn instruction was specified for the host step.	Read the common information of the error using GX Developer, and check and correct the error step corresponding to that value (program error location).	Q00J/Q00/ Q01* ² QnU
4506	The structure of the SFC program is illegal. • In a reset step, the host step number was specified as the destination step.			
	4600	The SFC program contains data that cannot be processed.	Read common information of the error using the peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem.	QnA Qn(H) QnPH QnPRH
	4601	Exceeds device range that can be designated by the SFC program.		
	4602	The START instruction in an SFC program is preceded by an END instruction.		

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07012 or later.

*5 The module whose first 5 digits of serial No. is 07032 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
4610	SFCP. EXE. ERROR	Program error location	—	On	On	Continue	STOP→RUN	
4611								
4620	BLOCK EXE. ERROR	Program error location	—	Off	Flicker	Stop	When instruction executed	
4621								
4630	STEP EXE. ERROR	Program error location	—	Off	Flicker	Stop	When instruction executed	
4631								
4632								
4633								

*1 CPU operation can be set in the parameters at error occurrence. (LED indication varies.)

*2 The function version is B or later.

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	4610	The active step information at presumptive start of an SFC program is incorrect.	Read common information of the error using the peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem. The program is automatically subjected to an initial start.	QnA Qn(H) QnPH QnPRH
	4611	Key-switch was reset during RUN when presumptive start was designated for SFC program.		
	4620	Startup was executed at a block in the SFC program that was already started up.	Read common information of the error using the peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem.	
	4621	Startup was attempted at a block that does not exist in the SFC program.	• Read the common information of the error using GX Developer, and check and correct the error step corresponding to that value (program error location). • Turn ON if the special relay SM321 is OFF.	QnA Q00J/Q00/ Q01* ² Qn(H) QnPH QnPRH QnU
	4630	Startup was executed at a block in the SFC program that was already started up.	Read common information of the error using the peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem.	QnA Qn(H) QnPH QnPRH
	4631	• Startup was attempted at the step that does not exist in the SFC program. - Or, the step that does not exist in the SFC program was specified for end. • Forced transition was executed based on the transition condition that does not exist in the SFC program. - Or, the transition condition for forced transition that does not exist in the SFC program was canceled.	• Read the common information of the error using the peripheral device, and check and correct the error step corresponding to that value (program error location). • Turn ON if the special relay SM321 is OFF.	QnA Q00J/Q00/ Q01* ² Qn(H) QnPH QnPRH QnU
	4632	There were too many simultaneous active steps in blocks that can be designated by the SFC program.	Read common information of the error using the peripheral device, check error step corresponding to its numerical value (program error location), and correct the problem.	QnA Qn(H) QnPH QnPRH QnU
	4633	There were too many simultaneous active steps in all blocks that can be designated.		

*3 The module whose first 5 digits of serial No. is 04012 or later.

*4 The module whose first 5 digits of serial No. is 07012 or later.

*5 The module whose first 5 digits of serial No. is 07032 or later.

*6 The module whose first 5 digits of serial No. is 09012 or later.

*7 The Universal model QCPU except the Q02UCPU.

22.3.7 Error code list (5000 to 5999)

The following shows the error messages from the error code 5000 to 5999, the contents and causes of the errors, and the corrective actions for the errors.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
5000	WDT ERROR	Time (value set)	Time (value actually measured)	Off	Flicker	Stop	Always	

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	5000	The scan time of the initial execution type program exceeded the initial execution monitoring time specified in the PLC RAS setting of the PLC parameter.	- Read the individual information of the error from the peripheral device, check its value (time), and shorten the scan time. - Change the initial execution monitoring time or the WDT value in the PLC RAS setting of the PLC parameter. - Resolve the endless loop caused by jump transition.	QnA Qn(H) QnPH QnPRH QnU
		- The power supply of the standby system is turned OFF. - The tracking cable is disconnected or connected without turning off or resetting the standby system. - The tracking cable is not secured by the connector fixing screws.	- Since power-off of the standby system increases the control system scan time, reset the WDT value, taking the increase of the control system scan time into consideration. - When the tracking cable is disconnected during operation, securely connect it and restart the CPU module. If the same error is displayed again, the tracking cable or CPU module has a hardware fault. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	QnPRH

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
5001	WDT ERROR	Time (value set)	Time (value actually measured)	Off	Flicker	Stop	Always	

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	5001	The scan time of the program exceeded the WDT value specified in the PLC RAS setting of the PLC parameter.	- Read the individual information of the error using the peripheral device, check its value (time), and shorten the scan time. - Change the initial execution monitoring time or the WDT value in the PLC RAS setting of the PLC parameter. - Resolve the endless loop caused by jump transition.	○
		- The power supply of the standby system is turned OFF. - The tracking cable is disconnected or connected without turning off or resetting the standby system. - The tracking cable is not secured by the connector fixing screws.	- Since power-off of the standby system increases the control system scan time, reset the WDT value, taking the increase of the control system scan time into consideration. - When the tracking cable is disconnected during operation, securely connect it and restart the CPU module. If the same error is displayed again, the tracking cable or CPU module has a hardware fault. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	QnPRH

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
5010	PRG. TIME OVER	Time (value set)	Time (value actually measured)	On	On	Continue	Always	
5011								

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	5010	The program scan time exceeded the constant scan setting time specified in the PLC RAS setting of the PLC parameter.	- Review the constant scan setting time. - Review the constant scan setting time and low speed program execution time in the PLC parameter so that the excess time of constant scan can be fully secured.	QnA Qn(H) QnPH QnPRH QnU
		The low speed program execution time specified in the PLC RAS setting of the PLC parameter exceeded the excess time of the constant scan.		QnA Qn(H) QnPH QnPRH
		The program scan time exceeded the constant scan setting time specified in the PLC RAS setting of the PLC parameter.	Review the constant scan setting time in the PLC parameter so that the excess time of constant scan can be fully secured.	Q00J/Q00/Q01
	5011	The scan time of the low speed execution type program exceeded the low speed execution watch time specified in the PLC RAS setting of the PLC parameter dialog box.	Read the individual information of the error using the peripheral device, check the numerical value (time) there, and shorten scan time if necessary. Change the low speed execution watch time in the PLC RAS setting of the PLC parameter dialog box.	QnA Qn(H) QnPH

22.3.8 Error code list (6000 to 6999)

The following shows the error messages from the error code 6000 to 6999, the contents and causes of the errors, and the corrective actions for the errors

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
6000	PRG. VERIFY ERR.	File name	–	Off	Flicker	Stop	Always	
	FILE DIFF.	File name	–	Off	Flicker	Stop	At power ON/ At reset/ At tracking cable connection/ At changing to backup mode/ At completion of write during RUN/ At system switching/ At switching both systems into RUN	

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
		The control system and standby system in the redundant system do not have the same programs and parameters. (This can be detected from the standby system of the redundant system.)	Synchronise the programs and parameters of the control system and standby system.	Q4AR
	6000	In a redundant system, the control system and standby system do not have the same programs and parameters. The file type detected as different between the two systems can be checked by the file name of the error common information. • The program is different. (File name = *****.QPG) • The PLC parameters/network parameters/redundant parameters are different. (File name = PARAM.QPA) • The remote password is different. (File name = PARAM.QPA) • The intelligent function module parameters are different. (File name = IPARAM.QPA) • The device initial values are different. (File name = *****.QDI) • The capacity of each write destination within the CPU for online pchange of multiple program blocks is different. (File name = MBOC.QMB) (This can be detected from the standby system of the redundant system.)	• Match the programs and parameters of the control system and standby system. • Perform PLC verify in either of the following procedures 1), 2) to clarify the differences between the files of the two systems, then correct the wrong file, and write the corrected file to the PLC again. 1) After reading the programs/parameters of System A using GX Developer or PX Developer, verify them with those of System B. 2) Verify the programs/parameters of GX Developer or PX Developer saved in the offline environment with those written to the CPU modules of both systems. • When the capacity of each write destination within the CPU for online change of multiple program blocks is different between the two systems, take corrective action 1) or 2). 1) Using the memory copy from control system to standby system, copy the program memory from the control system to the standby system. 2) Format the CPU module program memories of both systems. (For the capacity of each write destination within the CPU for online change of multiple program blocks, set the same value to both systems.)	QnPRH

*1 The module whose first 5 digits of serial No. is 09012 or later.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
6001	FILE DIFF.	—	—	Off	Flicker	Stop	At power ON/ At reset/At tracking cable connection/At operation mode change	
6010	MODE. VERIFY ERR.	—	—	On	On	Continue	Always	
	OPE. MODE DIFF.	—	—	On	On	Continue	Always	
6020	OPE. MODE DIFF.	—	—	Off	Flicker	Stop	At power ON/ At reset	
6030	UNIT LAY. DIFF.	Module No.	—	Off	Flicker	Stop	At power ON/ At reset/At tracking cable connection/At operation mode change	
6035	UNIT LAY. DIFF.	—	—	Off	Flicker	Stop		

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	6001	In a redundant system, the valid parameter drive settings (SW2, SW3) made by the DIP switches are not the same.	Match the valid parameter drive settings (SW2, SW3) by the DIP switches of the control system and standby system.	QnPRH
	6010	The operational status of the control system and standby system in the redundant system is not the same. (This can be detected from the standby system of the redundant system.)	Synchronise the operation statuses of the control system and standby system.	Q4AR
		The operational status of the control system and standby system in the redundant system is not the same. (This can be detected from the standby system of the redundant system.)	Synchronise the operation statuses of the control system and standby system.	QnPRH
	6020	At power ON/reset, the RUN/STOP switch settings of the control system and standby system are not the same in a redundant system. (This can be detected from the control system or standby system of the redundant system.)	Set the RUN/STOP switches of the control system and standby system to the same setting.	
	6030	- In a redundant system, the module configuration differs between the control system and standby system. - The network module mode setting differs between the two systems. (This can be detected from the control system or standby system of the redundant system.)	- Match the module configurations of the control system and standby system. - In the redundant setting of the network parameter dialog box, match the mode setting of System B to that of System A.	
	6035	In a redundant system, the CPU module model name differs between the control system and standby system. (This can be detected from the standby system of the redundant system.)	Match the model names of the control system and standby system.	

*1 The module whose first 5 digits of serial No. is 09012 or later.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
6036	UNIT LAY. DIFF.	Module No.	—	Off	Flicker	Stop	Always	
6040	CARD TYPE DIFF.	—	—	Off	Flicker	Stop	At power ON/ At reset	
6041		—	—	Off	Flicker	Stop	At power ON/ At reset	
6050	CAN'T EXE. MODE	—	—	On	On	Continue	Always	
6060	CPU MODE DIFF.	—	—	Off	Flicker	Stop	At power ON/ At reset/At tracking cable connection	
6061	CPU MODE DIFF.	—	—	Off	Flicker	Stop	When an END instruction executed	
6062	CPU MODE DIFF.	—	—	Off	Flicker	Stop	At power ON/ At reset/At tracking cable connection	

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	6036	A difference in the remote I/O configuration of the MELSECNET/H multiplexed remote I/O network between the control system and standby system of a redundant system was detected. (This can be detected from the control system or standby system of the redundant system.)	Check the network cables of the MELSECNET/H multiplexed remote I/O network for disconnection.	QnPRH
	6040	In a redundant system, the memory card installation status (installed/not installed) differs between the control system and standby system.	Match the memory card installation statuses (set/not set) of the control system and standby system.	
	6041	In a redundant system, the memory card type differs between the control system and standby system.	Match the memory card types of the control system and standby system.	
	6050	The function inexecutable in the debug mode or operation mode (backup/separate mode) was executed. (This can be detected from the control system or standby system of the redundant system.)	Execute the function executable in the debug mode or operation mode (backup/separate mode).	QnPRH
	6060	In a redundant system, the operation mode (backup/separate) differs between the control system and standby system.	Match the operation modes of the control system and standby system.	
	6061	(This can be detected from the standby system of the redundant system.)		
	6062	Both System A and B are in the same system status (control system). (This can be detected from the system B of the redundant system.)	Power the CPU module (System B) which resulted in a stop error, OFF and then ON.	QnPRH

*1 The module whose first 5 digits of serial No. is 09012 or later.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
6100	TRUCKINERR.	—	—	On	On	Continue	At power ON/ At reset/ STOP→RUN	
	TRK. TRANS. ERR.	Tracking transmission data classification	—	On	On	Continue	Always	

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
		A CPU module tracking memory error was detected during initial. (This can be detected from the control system or standby system of the redundant system.)	Hardware fault of the CPU module. (Please contact your local nearest Mitsubishi or sales representative, explaining a detailed description of the problem. Change the CPU modules in order of the standby system CPU module and control system CPU module.)	Q4AR
	6100	• An error (e.g. retry limit exceeded) occurred in tracking data transmission. (This error may be caused by tracking cable removal or other system power-off (including reset).) • The error occurred at a startup since the redundant system startup procedure was not followed.	• Check the CPU module or tracking cable. If the error still occurs, this indicates the CPU module or tracking cable is faulty. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.) • Confirm the redundant system startup procedure, and execute a startup again.	QnPRH

*1 The module whose first 5 digits of serial No. is 09012 or later.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
6101	TRUCKIN ERR.	—	—	On	On	Continue	When an END instruction executed	
		Tracking transmission data classification						
6102	TRK. TRANS. ERR.		—	On	On	Continue	Always	
6103		—						

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
		The CPU module detected an error during the handshake for tracking. (This can be detected from the control system or standby system of the redundant system.)	Check the condition of the other stations.	Q4AR
	6101	• A timeout error occurred in tracking (data transmission). (This error may be caused by tracking cable removal or other system power-off (including reset).) • The error occurred at a startup since the redundant system startup procedure was not followed. (This can be detected from the control system or standby system of the redundant system.)		
	6102	A data sum value error occurred in tracking (data reception). (This can be detected from the control system or standby system of the redundant system.)		
	6103	• A data error (other than sum value error) occurred in tracking (data reception). (This error may be caused by tracking cable removal or other system power-off (including reset).) • The error occurred at a startup since the redundant system startup procedure was not followed. (This can be detected from the control system or standby system of the redundant system.)	• Check the CPU module or tracking cable. If the error still occurs, this indicates the CPU module or tracking cable is faulty. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.) • Confirm the redundant system startup procedure, and execute a startup again.	QnPRH

*1 The module whose first 5 digits of serial No. is 09012 or later.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
6105	TRK. TRANS. ERR.	Tracking transmission data classification	—	On	On	Continue	Always	
6106								
6107	TRK. TRANS. ERR.	—	—	On	On	Continue	Always	
6108								
6110	TRK. SIZE ERROR	Tracking capacity excess error factor	—	On	On	Continue	When an END instruction executed	

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	6105	- An error (e.g. retry limit exceeded) occurred in tracking (data transmission). (This error may be caused by tracking cable removal or other system power-off (including reset).) - The error occurred at a startup since the redundant system startup procedure was not followed. (This can be detected from the control system or standby system of the redundant system.)	- Check the CPU module or tracking cable. If the error still occurs, this indicates the CPU module or tracking cable is faulty. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.) - Confirm the redundant system startup procedure, and execute a startup again.	QnPRH
	6106	- A timeout error occurred in tracking (data transmission). (This error may be caused by tracking cable removal or other system power-off (including reset).) - The error occurred at a startup since the redundant system startup procedure was not followed. (This can be detected from the control system or standby system of the redundant system.)		
	6107	A data sum value error occurred in tracking (data reception). (This can be detected from the control system or standby system of the redundant system.)	- Check the CPU module or tracking cable. If the error still occurs, this indicates the CPU module or tracking cable is faulty. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.) - Confirm the redundant system startup procedure, and execute a startup again.	QnPRH
	6108	- A data error (other than sum value error) occurred in tracking (data reception). (This error may be caused by tracking cable removal or other system power-off (including reset).) - The error occurred at a startup since the redundant system startup procedure was not followed. (This can be detected from the control system or standby system of the redundant system.)		
	6110	The tracking capacity exceeded the allowed range. (This can be detected from the control system or standby system of the redundant system.)	Reexamine the tracking capacity.	QnPRH

*1 The module whose first 5 digits of serial No. is 09012 or later.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
6111	TRK. SIZE ERROR	—	—	On	On	Continue	When an END instruction executed	
6112	TRK. SIZE ERROR	—	—	On	On	Continue	When an END instruction executed	
6120	TRK. CABLE ERR.	—	—	Off	Flicker	Stop	At power ON/ At reset	

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	6111	The control system does not have enough file register capacity for the file registers specified in the tracking settings. (This can be detected from the control system or standby system of the redundant system.)	Switch to the file registers of which capacity is greater than the file registers specified in the tracking settings.	QnPRH
	6112	File registers greater than those of the standby system were tracked and transmitted from the control system. (This can be detected from the standby system of the redundant system.)	Switch to the file registers of which capacity is greater than the file registers specified in the tracking settings.	
	6120	• A start was made without the tracking cable being connected. • A start was made with the tracking cable faulty. • As the tracking hardware on the CPU module side was faulty, communication with the other system could not be made via the tracking cable. (This can be detected from the control system or standby system of the redundant system.)	Make a start after connecting the tracking cable. If the same error still occurs, this indicates the tracking cable or CPU module side tracking transmission hardware is faulty. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	

*1 The module whose first 5 digits of serial No. is 09012 or later.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
6130	TRK. DISCONNECT	—	—	On	On	Continue	Always	
6140	TRK.INIT. ERROR	—	—	Off	Flicker	Stop	At power ON/ At reset	
6200	CONTROL EXE.	Reason(s) for system switching	—	On	Off	Continue	Always	
	CONTROL EXE.	Reason(s) for system switching	—	On	Off	No error	Always	

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	6130	• The tracking cable was removed. • The tracking cable became faulty while the CPU module is running. • The CPU module side tracking hardware became faulty. (This can be detected from the control system or standby system of the redundant system.)	• If the tracking cable was removed, connect the tracking cable to the connectors of the CPU modules of the two systems. • When the error is not resolved after connecting the tracking cable to the connectors of the CPU modules of the two systems and resetting the error, the tracking cable or CPU module side tracking hardware is faulty. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	QnPRH
	6140	• The other system did not respond during initial communication at power ON/reset. • The error occurred at a startup since the redundant system startup procedure was not followed. (This can be detected from the control system or standby system of the redundant system.)	• Power the corresponding CPU module OFF and then ON again, or reset it and then unreset. If the same error still occurs, this indicates the CPU module is faulty. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.) • Confirm the redundant system startup procedure, and execute a startup again.	
		The standby system in a redundant system is switched to the control system. (This can be detected from the standby system of the redundant system.)	Check the control system condition.	Q4AR
	6200	The standby system has been switched to the control system in a redundant system. (Detected by the CPU that was switched from the standby system to the control system) Since this error code does not indicate the error information of the CPU module but indicates its status, the error code and error information are not stored into SD0 to 26, but are stored into the error log every system switching. (Check the error information by reading the error log using GX Developer.)	—	QnPRH

*1 The module whose first 5 digits of serial No. is 09012 or later.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
6210	CONTROL WAIT	Reason(s) for system switching	–	On	Off	Continue	Always	
	STANDBY	Reason(s) for system switching	–	On	Off	No error	Always	
6220	CAN'T EXE. CHANGE	Reason(s) for system switching	–	On	On	Continue	At switching request	
	CAN'T SWITCH	Reason(s) for system switching	Reason(s) for system switching failure	On	On	Continue	At switching execution	

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	6210	The control system in a redundant system is switched to the standby system. (This can be detected from the standby system of the redundant system.)	Check the control system condition.	Q4AR
		The control system has been switched to the standby system in a redundant system. (Detected by the CPU that was switched from the control system to the standby system) Since this error code does not indicate the error information of the CPU module but indicates its status, the error code and error information are not stored into SD0 to 26, but are stored into the error log every system switching. (Check the error information by reading the error log using GX Developer.)	—	QnPRH
	6220	• Since the standby system is in an error or similar status in the redundant system, the control system cannot be switched to the standby system. • When an attempt was made to execute system switching, the control system could not be switched to the standby system due to a network error of the control system. (This can be detected from the control system of the redundant system.)	Check the standby system condition.	Q4AR
		System switching cannot be executed due to standby system error/ tracking cable error/ online module change in execution at separate mode. Causes for switching system at control system are as follows: • System switching by SP. CONTSW instruction • System switching request from network module	• Check the status of the standby system and resolve the error. • Complete the online module change.	QnPRH

*1 The module whose first 5 digits of serial No. is 09012 or later.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
6221	CAN'T EXE. CHANGE	Reason(s) for system switching	–	On	On	Continue	At switching request	
6230	DUAL SYS. ERROR	–	–	On	On	Continue	Always	
6300	STANDBY SYS. DOWN	–	–	On	On	Continue	Always	

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	6221	Switching is disabled because of a bus switching module error. (This can be detected from the control system of the redundant system.)	This is a bus switching module hardware fault. (Contact your local Mitsubishi representative.)	Q4AR
	6230	The link module mounted on the standby system CPU module is the remote master station.	Check the system configuration status.	
	6300	Any of the following errors was detected in the backup mode. • The standby system has not started up in the redundant system. • The standby system has developed a stop error in the redundant system. • The CPU module in the debug mode was connected to the operating control system. (This can be detected from the control system of the redundant system.)	• Check whether the standby system is on or not, and if it is not on, power it on. • Check whether the standby system has been reset or not, and if it has been reset, unreset it. • Check whether the standby system has developed a stop error or not, and if it has developed the error, remove the error factor and restart it. • When the CPU module in the debug mode was connected to the control system operating in the backup mode, make connection so that the control system and standby system are combined correctly.	QnPRH

*1 The module whose first 5 digits of serial No. is 09012 or later.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
6310	CONTROL SYS. DOWN	—	—	Off	Flicker	Stop	Always	
6311	CONTROL SYS. DOWN	—	—	Off	Flicker	Stop	At power ON/ At reset	
6312								
6313	CONTROL SYS. DOWN	—	—	Off	Flicker	Stop	At power ON/ At reset	

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	6310	Any of the following errors was detected in the backup mode. • The control system has not started up in the redundant system. • The control system has developed a stop error in the redundant system. • The CPU module in the debug mode was connected to the operating standby system. • The error occurred at a startup since the redundant system startup procedure was not followed. (This can be detected from the standby system of the redundant system.)	• The standby system exists but the control system does not exist. • Check whether the system other than the standby system is on or not, and if it is not on, power it on. • Check whether the system other than the standby system has been reset or not, and if it has been reset, unreset it. • Check whether the system other than the standby system has developed a stop error or not, and if has developed the error, remove the error factor, set the control system and standby system to the same operating status, and restart. • When the CPU module in the debug mode was connected to the control system operating in the backup mode, make connection so that the control system and control system are combined correctly. • Confirm the redundant system startup procedure, and execute a startup again.	QnPRH
	6311	• As consistency check data has not transmitted from the control system in a redundant system, the other system cannot start as a standby system. • The error occurred at a startup since the redundant system startup procedure was not followed. (This can be detected from the standby system of the redundant system.)	• Replace the tracking cable. If the same error still occurs, this indicates the CPU module is faulty. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.) • Confirm the redundant system startup procedure, and execute a startup again.	QnPRH
	6312			
	6313	The control system detected the error of the system configuration and informed it to the standby system (host system) in the redundant system.	Restart the system after checking that the connection between base unit and the system configuration (type/number/parameter of module) are correct.	QnPRH*1

*1 The module whose first 5 digits of serial No. is 09012 or later.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
6400	PRG. MEM. CLEAR	—	—	Off	Flicker	Stop	At execution of the memory copy from control system to standby system	
6410	MEM.COPY EXE	—	—	On	On	Continue	At execution of the function of copying memory from control system to standby system	
6500	TRK. PARA. ERROR	File name/ Drive name	Parameter number	Off	Flicker	Stop	At power ON/ At reset	
6501		File name/ Drive name	Parameter number	Off	Flicker	Stop	At power ON/ At reset	

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	6400	The memory copy from control system to standby system was executed, and the program memory was cleared.	After the memory copy from control system to standby system is completed, switch power OFF and then ON, or make a reset.	QnPRH
	6410	The memory copy from control system to standby system was executed. (This can be detected from the control system of the redundant system.)	—	
	6500	The file register file specified in the tracking setting of the PLC parameter dialog box does not exist.	Read the individual information of the error using GX Developer, and check and correct the drive name and file name. Create the specified file.	QnPRH
	6501	The file register range specified in the device detail setting of the tracking setting of the PLC parameter dialog box exceeded the specified file register file capacity.	Read the individual information of the error using GX Developer, and increase the file register capacity.	

*1 The module whose first 5 digits of serial No. is 09012 or later.

22.3.9 Error code list (7000 to 10000)

The following shows the error messages from the error code 7000 to 10000, the contents and causes of the errors, and the corrective actions for the errors.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
7000	MULTI CPU DOWN	Module No. (CPU No.)	–	Off	Flicker	Stop	Always	
7002	MULTI CPU DOWN	Module No. (CPU No.)	–	Off	Flicker	Stop	At power ON/ At reset	
7003								

*1 The function version is B or later.

*2 For the Basic model QCPU, the special register (SD207 to DS209) for LED indication priority can turn off the indication. (The LED indication is always OFF for the High Performance model QCPU, Process CPU, Redundant CPU, and Universal model QCPU.)

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	7000	- In the operating mode of a multiple CPU system, a CPU error occurred at the CPU where "All station stop by stop error of CPU " was selected. - In a multiple CPU system, a CPU module incompatible with the multiple CPU system was mounted.	- Read the individual information of the error using the GX Developer, check the error of the PLC resulting in CPU module fault, and remove the error. - Remove the CPU module incompatible with the multiple CPU system from the main base unit.	Q00/Q01* ¹ Qn(H)* ¹ QnPH QnU
		In a multiple CPU system, CPU other than CPU No.1 cannot be started up due to stop error of the CPU No.1 at power-on, which occurs to CPU No.2 to No.4.	Read the individual information of the error using the GX Developer, check the error of the PLC resulting in CPU module fault, and remove the error.	Q00/Q01* ¹ Qn(H)* ¹ QnPH QnU
	7002	- There is no response from the target CPU module in a multiple CPU system during initial communication. - In a multiple CPU system, a CPU module incompatible with the multiple CPU system was mounted.	- Reset the CPU module and RUN it again. If the same error is displayed again, this suggests the hardware fault of any of the CPU modules. (Contact your local Mitsubishi representative.) - Remove the CPU module incompatible with the multiple CPU system from the main base unit. Or, replace the CPU module incompatible with the multiple CPU system with the compatible one.	Q00/Q01* ¹ Qn(H)* ¹ QnPH
		There is no response from the target CPU module in a multiple CPU system during initial communication.	Reset the CPU module and RUN it again. If the same error is displayed again, this suggests the hardware fault of any of the CPU modules. (Contact your local Mitsubishi representative.)	QnU
	7003	There is no response from the target CPU module in a multiple CPU system at initial communication stage.	Reset the CPU module and RUN it again. If the same error is displayed again, this suggests the hardware fault of any of the CPU modules. (Contact your local Mitsubishi representative.)	Q00/Q01* ¹ Qn(H)* ¹ QnPH

*3 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
7004	MULTI CPU DOWN	Module No. (CPU No.)	—	Off	Flicker	Stop	Always	
7010	MULTI EXE. ERROR	Module No. (CPU No.)	—	Off	Flicker	Stop	At power ON/ At reset	

*1 The function version is B or later.

*2 For the Basic model QCPU, the special register (SD207 to DS209) for LED indication priority can turn off the indication. (The LED indication is always OFF for the High Performance model QCPU, Process CPU, Redundant CPU, and Universal model QCPU.)

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	7004	In a multiple CPU system, a data error occurred in communication between the CPU modules.	• Check the system configuration to see if modules are mounted in excess of the number of I/O points. • When there are no problems in the system configuration, this indicates the CPU module hardware is faulty. (Contact your local Mitsubishi representative, explaining a detailed description of the problem.)	Q00/Q01* ¹ QnU
	7010	• In a multiple CPU system, a faulty CPU module was mounted. • In a multiple CPU system, a CPU module incompatible with the multiple CPU system was mounted. (The CPU module compatible with the multiple CPU system was used to detect an error.) • In a multiple CPU system, any of the CPU No. 2 to 4 was reset with power ON. (The CPU whose reset state was cancelled was used to detect an error.) • In a multiple CPU system, the PC CPU module used the QFB (bus interface driver) of version 1.06 or earlier.	• Read the individual information of the error using GX Developer, and replace the faulty CPU module. • Replace the CPU module with the one compatible with the multiple CPU system. • Do not reset any of the No. 2 to 4 CPU modules. • Use the PC CPU module that uses the QFB of version 1.07 or later. • Reset CPU No. 1 and restart the multiple CPU system.	Q00/Q01* ¹ Qn(H)* ¹ QnPH QnU

*3 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
7011	MULTI EXE. ERROR	Module No. (CPU No.)	—	Off	Flicker	Stop	At power ON/ At reset	
7013	MULTI EXE. ERROR	Module No. (CPU No.)	—	Off	Flicker	Stop	At power ON/ At reset	
7020	MULTI CPU ERROR	Module No. (CPU No.)	—	On	On	Continue	Always	
7030	CPU LAY. ERROR	Module No. (CPU No.)	—	Off	Flicker	Stop	At power ON/ At reset	
7031								

*1 The function version is B or later.

*2 For the Basic model QCPU, the special register (SD207 to DS209) for LED indication priority can turn off the indication. (The LED indication is always OFF for the High Performance model QCPU, Process CPU, Redundant CPU, and Universal model QCPU.)

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	7011	Either of the following settings was made in a multiple CPU system. - Multiple CPU automatic refresh setting was made for the inapplicable CPU module. "I/O sharing when using multiple CPUs" setting was made for the inapplicable CPU module.	- Correct the multiple CPU automatic refresh setting. - Correct the "I/O sharing when using multiple CPUs" setting.	Q00/Q01* ¹ QnU
		The system configuration for using the Multiple CPU high speed transmission function is not met. - The QnUD(H)CPU is not used for the CPU No.1. - The Multiple CPU high speed main base unit (Q3□DB) is not used. - Points other than 0 is set to the send range for the CPU module incompatible with the multiple CPU high speed transmission function. - Points other than 0 is set to the send range for the CPU module incompatible with the multiple CPU.	Change the system configuration to meet the conditions for using the Multiple CPU high speed transmission function.	QnU* ³
	7013	The Q172(H)CPU(N) or Q173(H)CPU(N) is mounted to the CPU slot or slots 0 to 2. (The module may break down.)	Remove the Q172(H)CPU(N) or Q173(H)CPU(N).	QnU
	7020	In the operating mode of a multiple CPU system, an error occurred in the CPU where "system stop" was not selected. (The CPU module where no error occurred was used to detect an error.)	Read the individual information of the error using the peripheral device, check the error of the CPU module resulting in CPU module fault, and remove the error.	Q00/Q01* ¹ Qn(H)* ¹ QnPH QnU
	7030	An assignment error occurred in the CPU-mountable slot (CPU slot, I/O slot 0, 1) in excess of the number of CPU modules specified in the multiple CPU setting of the PLC parameter dialog box.	Set the same value to the number of CPU modules specified in the multiple CPU setting of the PLC parameter dialog box and the number of mounted CPU modules (including CPU (empty)).	Q00J/Q01/ Q01* ¹ QnU
	7031	An assignment error occurred within the range of the number of CPUs specified in the multiple CPU setting of the PLC parameter dialog box.	Make the type specified in the I/O assignment setting of the PLC parameter dialog box consistent with the CPU module configuration.	

*3 The Universal model QCPU except the Q02UCPU.

Error Code (SD0)	Error Message	Common Information (SD5 to 15)	Individual Information (SD16 to 26)	LED Status		CPU Operation Status	Diagnostic Timing	
				RUN	ERROR			
7032	CPU LAY. ERROR	Module No. (CPU No.)	—	Off	Flicker	Stop	At power ON/ At reset	
7035	CPU LAY. ERROR	Module No. (Slot No.)	—	Off	Flicker	Stop	At power ON/ At reset	
7036	CPU RAY ERROR	Module No. (CPU No.)	—	Off	Flicker	Stop	At power ON/ At reset	
8031	INCORRECT FILE	—	File diagnostic information	Off	Off	Stop	At power-On/ At reset/ STOP→RUN/ At PLC writing	
9000	F****	Program error location	Annunciator number	On	On/ Off *2	Continue	When instruction executed	
				USER LED On				
9010	<CHK>ERR ***_***	Program error location	Failure No.	On	Off	Continue	When instruction executed	
				USER LED On				
9020	BOOT OK	—	—	Off	Flicker	Stop	At power ON/ At reset	
10000	CONT. UNIT ERROR	—	—	Off	Flicker	Continue	Always	

*1 The function version is B or later.

*2 For the Basic model QCPU, the special register (SD207 to DS209) for LED indication priority can turn off the indication. (The LED indication is always OFF for the High Performance model QCPU, Process CPU, Redundant CPU, and Universal model QCPU.)

	Error Code (SD0)	Error Contents and Cause	Corrective Action	Corresponding CPU
	7032	The number of CPU modules mounted in a multiple CPU system is wrong.	Configure a system so that the number of mountable modules of each CPU module does not exceed the maximum number of mountable modules specified in the specification.	Q00/Q01* ¹ QnU
	7035	The CPU module has been mounted on the inapplicable slot.	Mount the CPU module on the applicable slot.	Q00J/Q00/ Q01* ¹ QnPRH QnU
	7036	The host CPU No. set by the multiple CPU setting and the host CPU No. determined by the mounting position of the CPU module are not the same.	- Mount the mounting slot of the CPU module correctly. - Correct the host CPU No. set by the multiple CPU setting to the CPU No. determined by the mounting position of the CPU module.	QnU* ³
	8031	The error of stored file (enabled parameter file) is detected.	Write the file shown as SD17 to SD22 of individual information to the drive shown as SD16(L) of individual information, and turn ON from OFF the power supply of the CPU module or cancel the reset. If the same error is displayed again, the CPU module has hardware failure. Contact your local Mitsubishi representative, explaining a detailed description of the problem.	QnU
	9000	Annunciator (F) was set ON	Read the individual information of the error using the peripheral device, and check the program corresponding to the numerical value (annunciator number).	○
	9010	Error detected by the CHK instruction.	Read the individual information of the error using the peripheral device, and check the program corresponding to the numerical value (error number) there.	QnA Qn(H) QnPH QnPRH
	9020	Storage of data onto ROM was completed normally in automatic write to standard ROM. (BOOT LED also flickers.)	Use the DIP switches to set the valid parameter drive to the standard ROM. Then, switch power on again, and perform boot operation from the standard ROM.	Qn(H)* ¹ QnPH QnPRH
	10000	In the multiple CPU system, an error occurred in the CPU module other than the Process CPU/High Performance model QCPU.	Check the details of the generated error by connecting to the corresponding CPU module using GX Developer.	Qn(H)* ¹ QnPH

*3 The Universal model QCPU except the Q02UCPU.

22.3.10 Canceling of Errors

Q series CPU module can perform the cancel operation for errors only when the errors allow the CPU module to continue its operation.

To cancel the errors, follow the steps shown below.

- 1) Eliminate the cause of the error.
- 2) Store the error code to be canceled in the special register SD50.
- 3) Energize the special relay SM50 (OFF → ON).
- 4) The error to be canceled is canceled.

After the CPU module is reset by the canceling of the error, the special relays, special registers, and LEDs associated with the error are returned to the status under which the error occurred.

If the same error occurs again after the cancellation of the error, it will be registered again in the error history.

When multiple enunciators(F) detected are canceled, the first one with No. F only is canceled.

Refer to the following manual for details of error canceling.

→ QCPU User's Manual (Function Explanation, Program Fundamentals)

POINT	
(1)	When the error is canceled with the error code to be canceled stored in the SD50, the lower one digit of the code is neglected. (Example) If error codes 2100 and 2101 occur, and error code 2100 to cancel error code 2101. If error codes 2100 and 2111 occur, error code 2111 is not canceled even if error code 2100 is canceled.
(2)	Errors developed due to trouble in other than the CPU module are not canceled even if the special relay (SM50) and special register (SD50) are used to cancel the error. (Example) Since "SP. UNIT DOWN" is the error that occurred in the base unit (including the extension cable), intelligent function module, etc. the error cause cannot be removed even if the error is canceled by the special relay (SM50) and special register (SD50). Refer to the error code list and remove the error cause.

22.4 Resetting Errors

The CPU module allows error resetting only for the errors that does not block the CPU module operation.

The procedure for resetting an error is as follows.

- 1) Eliminate the cause of the error.
- 2) Store the error code to be reset to special register SD50.
- 3) Switch special relay SM50 from OFF to ON.
- 4) The error is reset.

If the CPU module is returned with the error reset, the special relay and special register relating to the error, and the LED/LED indicator return to their state before the error occurred.

If the same error occurs again after the error has been reset, it is recorded in breakdown history again.

To reset multiple detected annunciators, only the first detected F number is reset.

POINT	
	When storing the error code to be reset in SD50 at error reset, the lower one digit of the code number is ignored. Example: When error codes 2100 and 2101 occurred, resetting of error code 2100 results in also resetting of error code 2101. When error codes 2100 and 2111 occurred, resetting of error code 2100 does not result in resetting of error code 2111.

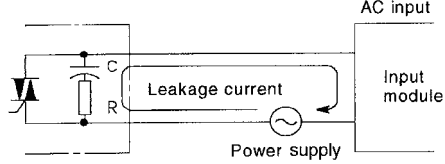
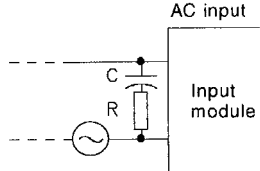
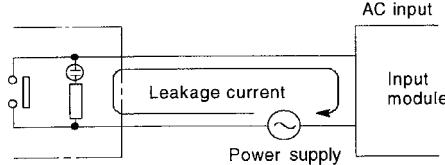
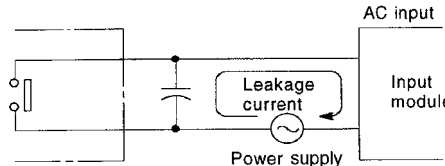
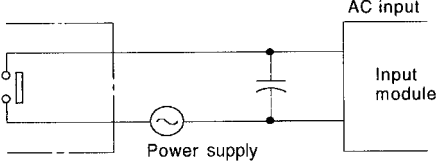
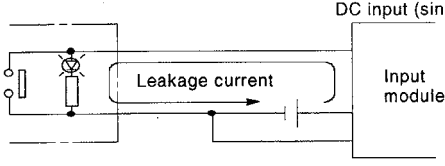
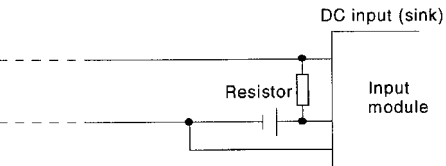
22.5 Fault Examples with I/O Modules

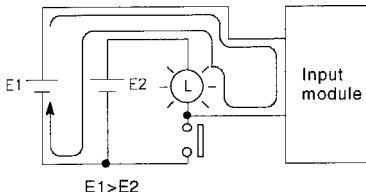
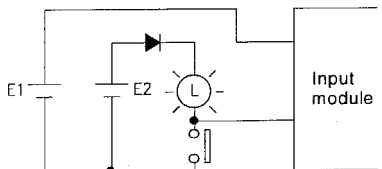
Examples of faults concerning I/O circuits and the corrective actions are explained.

22.5.1 Faults with the input circuit and the corrective actions

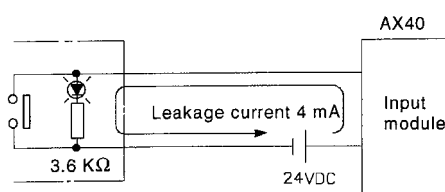
Examples of faults concerning input circuit and the corrective actions are explained.

Faults with the input circuit and the corrective actions

	Situation	Cause	Countermeasure
Example 1	Input signal does not turn OFF.	Leak current from input switch (driven by a contactless switch, etc.) 	Connect an appropriate resistance so that voltage between the terminals of the input module is lower than the OFF voltage.  For CR constant, 0.1 to 0.47 μF + 47 to 120 Ω (1/2W) is recommended.
Example 2	Input signal does not turn OFF.	Driven by a limit switch with a neon lamp 	- Same as the example 1. - Or, provide a totally independent display circuit separately.
Example 3	Input signal does not turn OFF.	Line capacity C of the leak current twisted pair cable due to line capacity of the wiring cable is about 100PF/m. 	- Same as the example 1. - However, leakage current does not occur when a power supply is on the side of input device as shown below. 
Example 4	Input signal does not turn OFF.	Driven by a switch with LED indication 	Connect an appropriate resistance so that voltage between the terminal of the input module and the common is lower than the OFF voltage as shown below.  * An example of calculation of resistor to be connected is provided on the following page.

	Situation	Cause	Countermeasure
Example 5	Input signal does not turn OFF.	Sneak path due to the use of two power supplies. 	- Use only one power supply. - Connect a diode for a sneak path. (Figure below). 

Calculation example for Example 4

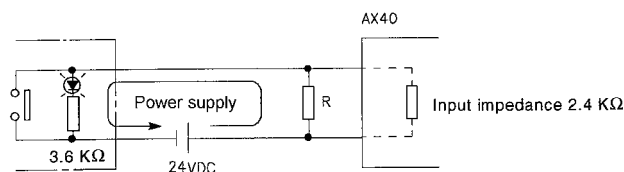


If a switch with LED indication is connected to the AX40 and leak current of 4mA is generated

- Voltage V_{TB} between the terminal and common is as follows:

$$V_{TB} = 4[\text{mA}] \times 2.4[\text{k}\Omega] = 9.6[\text{V}] \text{ (Ignore the voltage drop caused by the LED.)}$$

Because the condition for the OFF voltage (6[V]) is not satisfied, the input does not turn off. To correct this, connect a resistor as shown below.



- Calculation of resistance of connected resistor R

The voltage of AX40 between the terminals must be reduced to within 6[V]. The current for reducing the voltage between the terminals to within 6 [V] is:

$$(24 - 6[\text{V}]) / 3.6[\text{k}\Omega] = 5\text{mA}$$

Therefore, resistor R for flowing current I of 5[mA] has to be connected.

- Resistance of the connected resistor R is obtained in the following equations.

$$6[\text{V}] / R > 5 - 2.5[\text{mA}] \leftarrow 6[\text{V}] / \text{Input impedance } 2.4[\text{k}\Omega]$$

$$6[\text{V}] / 2.5\text{mA} > R$$

$$2.4[\text{k}\Omega] > R$$

Suppose that the resistance R is 2[kΩ].

The power capacity W of the resistor when the switch turned on is:

$$W = (\text{Applied voltage})^2 / R$$

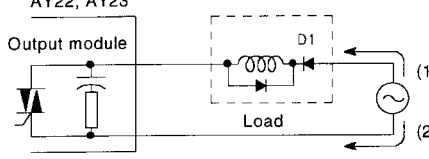
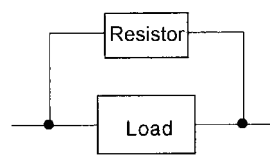
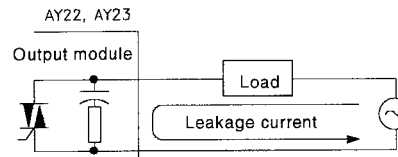
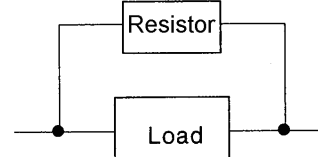
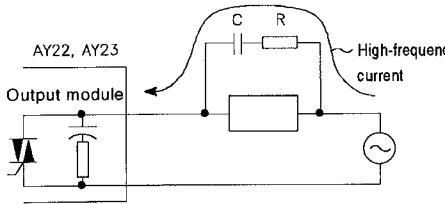
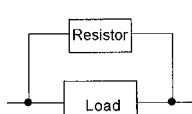
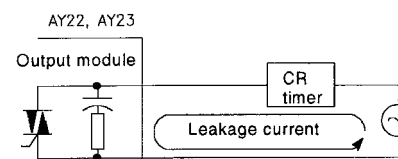
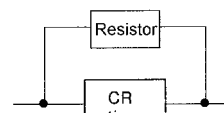
$$W = (26.4[\text{V}])^2 / 2[\text{k}\Omega] = 0.348[\text{W}]$$

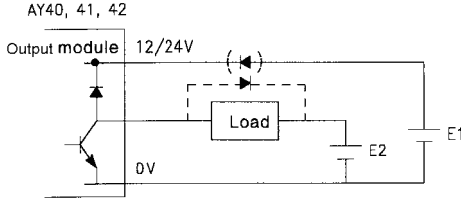
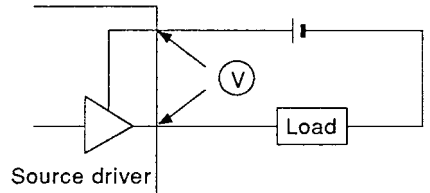
- Because the resistance is selected so that the power capacity is three to five times the actual power consumption, 1.5 to 2 [W] should be selected. From the above, the resistor to be connected across the terminal in question and COM is 2[kΩ] 1.5 to 2[W].

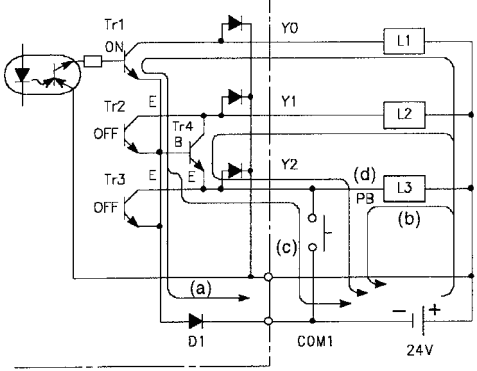
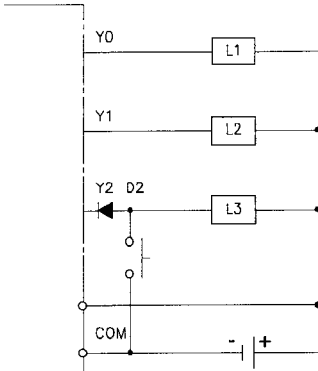
22.5.2 Faults in the output circuit

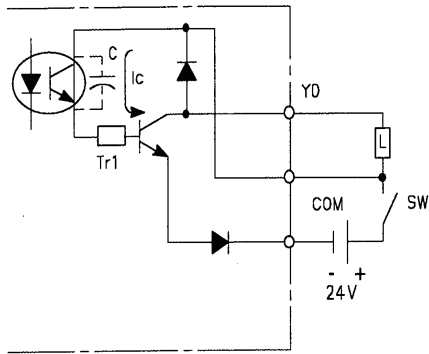
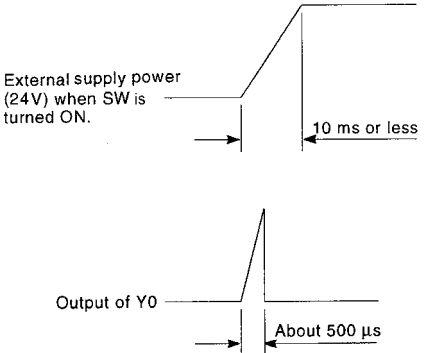
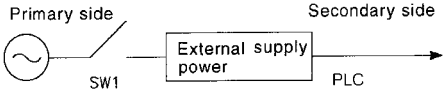
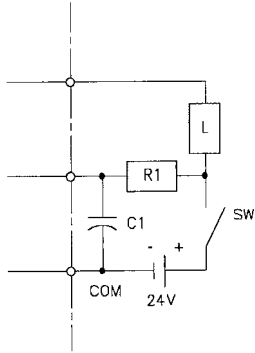
Faults concerning output circuits and the corrective actions are explained.

Faults in the output circuit

	Situation	Cause	Countermeasure
Example 1	An excessive voltage is applied to the load when output is off. (Triac output)	- When the load is subjected to half wave rectification inside (Solenoids have these types.)  - When the polarity of the power supply is (1), C is charged, and when the polarity is (2), the voltage charged in C + voltage of the power supply are applied to the both ends of D1. The maximum value of the voltage is about 2.2E.	Connect a resistor at several tens to several hundred of $k\Omega$ to the both ends of the load. (With this kind of usage, there is no problem with the output element, but the diode built-in to the load may deteriorate and burn-out.) 
Example 2	Load does not turn OFF. (Triac output)	Leak current caused by built-in noise suppressor 	Connect a resistor to the both ends of the load. (When the wiring distance from the output module to the load is long, be aware of the risk of a leak current due to line capacity.) 
Example 3	Load turns OFF with a delay. (Triac output)	Leakage current due to surge suppressor for the load. 	Disconnect the surge suppressor from across the loads, leaving only the resistance. (When the wiring distance from the output module to the load is long, be aware of the risk of a leak current due to line capacity.)  Guide to resistive value: At 100VAC: 5 to 10 $k\Omega$, 5 to 3 W At 200 VAC: 10 to 20 $k\Omega$, 15 to 10 W
Example 4	When load is CR type timer, the time limit fluctuates. (Triac output)	Leakage current caused by built-in noise suppressor 	Connect a resistance between the CR timer terminals. (In some timers, internal circuit may be half wave rectification type, so the caution as to the example 1 is necessary here.) (When the wiring distance from the output module to the load is long, be aware of the risk of a leak current due to line capacity.)  Calculate the resistance constant in accordance with the load.

	Situation	Cause	Countermeasure
Example 5	Load does not turn OFF. (Transistor output with clamp diode)	- Sneak path due to the use of two power supplies.  - Sneak path occurs when $E1 < R E2$.	- Use only one power supply. - Connect a diode for a sneak path. (When the load is a relay or similar device, a reverse voltage absorbing diode must be connected to it.) (Shown by dotted line in the figure at left)
Example 6	Load does not operate normally (due to external shorting, etc.) AY60EP, AY80EP, AY81EP, AY82EP,	External load malfunction or incorrect connection.	- Check the external load. - Check voltages across the following terminals with output (Y) on. If output voltage $> 3V$, check external load and wiring for short circuits. 

Situation		Cause	Countermeasure
Example 7	When an external switch is connected in parallel between the output and common, the voltage between Y1 and COM1 drops to between 0 and 24V even though the output Y1 which is not connected to the external switch is OFF. Especially when the load L2 is relatively small, (Load current of several mA only) such as LED lamps and photocouplers, the outputs drop. AY40 AY41 AY42	Incorrect output by parasitic transistor (Tr4)  Y2 can turn the load L3 on either from a PC or PB. When PB is ON, Y0 is ON with a PC, and Y1 is OFF: (1) L1 (current (a)) and L3 (current (b)) turn ON. (2) A potential difference to COM1 occurs in the emitter E of Tr1 to Tr3 since diode D1 is connected between COM1 and the emitter. (3) The transistors AY40 to 42, etc., are accompanied by a parasitic transistor (Tr4). (4) The potential difference described in (2) above is supplied between the base (B) of Tr4 and emitter (E), which causes the base current (c) to flow. (Tr4 turns ON). (5) The current in (4) causes the collector current (d) to flow, and voltage Y1 drops to between 0 and 24V.	 Add a diode D2 of the class IF=1A to the output Y2 to connect an external switch as shown in the diagram above to prevent current (c) and (d) in the diagram at left from flowing. However, check the operation voltage of L3 as the amount of voltage drop of Y2 at power ON increases for 0.6 to 1V.

	Situation	Cause	Countermeasure
Example 8	The load is momentarily turned ON when the external supply power is started up. (Transistor output)	Incorrect output due to the floating capacitance (C) between the collector and emitter of the photocoupler (This does not affect normal loads, but in case of highly sensitive loads (such as solid state relays), incorrect outputs may occur.) Photocoupler  (1) If the external supply power is suddenly started up, current I_c flows due to the floating capacitance (C) between the collector and emitter of the photocoupler. (2) Current I_c flows to the base of transistor Tr1 in the next stage, and output Y0 turns ON for about 500 μs. 	(1) After checking the external supply power takes at least 10ms to start up when turned it ON/OFF, set the switch SW1 at the primary side of the external supply power.  (2) If setting the switch at the secondary side of the external supply power is required, connect a capacitor and resistor so that the start-up of the power is slowly performed (Longer than 10ms).  R1: Several tens of ohms Power capacity $\geq (\text{External supply power current})^2 \times 1$ $\times \text{Resistive value} \times (3 \text{ to } 5)^2$ C1: Several hundreds of μF, 50 mV *1 For the current consumption of the external supply power, refer to the manual attached to the module to be used. *2 Select the resistance for power capacity in the range of between 3 and 5 times higher than the actual power consumption. Example: R1 = 40 Ω , C1 = 300 μF Calculate the time constant as follows: $C1 \times R1 = 300 \times 10^{-6} \times 40$ $= 12 \times 10^{-3} \text{S}$ $= 12 \text{ms}$

APPENDICES

APPENDIX 1 INSTRUCTION LIST

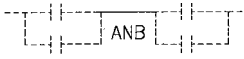
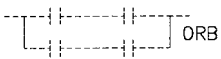
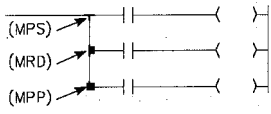
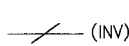
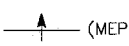
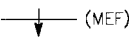
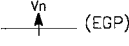
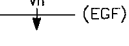
For details on SFC-related instructions, refer to the QnACPU Programming Manual (SFC).

Appendix 1.1 Sequence Instructions

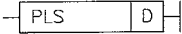
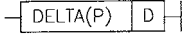
(1) Contact instructions

Classification	Symbol	Description
Contact		• Logical operation start (N/O contact logical operation start)
		• Logical NOT operation start (N/C contact logical operation start)
		• Logical product (N/O contact series connection)
		• Logical product NOT (N/C contact series connection)
		• Logical sum (N/O contact parallel connection)
		• Logical sum NOT (N/C contact parallel connection)
		• Rising edge pulse operation start
		• Falling edge pulse operation start
		• Rising edge pulse series connection
		• Falling edge pulse series connection
		• Rising edge pulse parallel connection
		• Falling edge pulse parallel connection

(2) Association commands

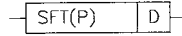
Classification	Symbol	Description
Association		ANDs logical blocks (series connection of blocks).
		ORs logical blocks (parallel connection of blocks).
		Stores the operation result.
		Reads the operation result from MPS.
		Reads the operation result from MPS and clears the result.
		Inverts the operation result.
		Converts the operation result to a rising edge pulse.
		Converts the operation result to falling edge pulse.
		Converts the operation result to rising edge pulse (stored at Vn).
		Converts the operation result to falling edge pulse (stored at Vn).

(3) Output instructions

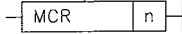
Classification	Symbol	Description
Output		• Device output
		• Sets a device.*
		• Resets a device.
		• Generates one-program cycle pulse at the rising edge of an input signal.
		• Generates one-program cycle pulse at the falling edge of an input signal.
		• Inverts device output.
		• Converts a direct output to pulse.

* When specifying input (X) for the target device, specify the device number out of the actual input (X) range.

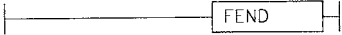
(4) Shift instructions

Classification	Symbol	Description
Shift		• Shifts a device 1 bit.

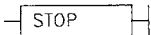
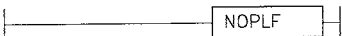
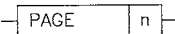
(5) Master control instructions

Classification	Symbol	Description
Master control		• Master control start
		• Master control reset

(6) End instructions

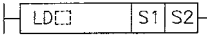
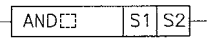
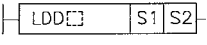
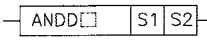
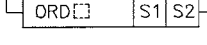
Classification	Symbol	Description
Program end		Ends the main program.
		Ends the sequence program.

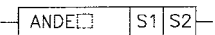
(7) Other instructions

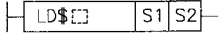
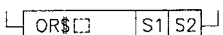
Classification	Symbol	Description
Stop		- Stops sequence operation when the input condition is met. - Sequence program execution can be resumed by turning the RUN/STOP key switch to RUN.
No processing	$\overline{(\text{NOP})}$	No processing (for program erasure or space)
		No processing (for starting a new page during printout)
		No processing (for managing the rest of the program as starting from step 0 of page "n")

Appendix 1.2 Basic Instructions

(1) Comparison operation instructions

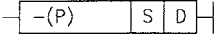
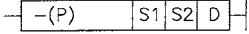
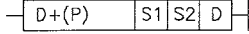
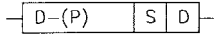
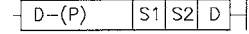
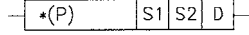
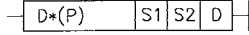
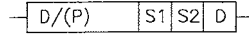
Classification	Symbol	Description
16-bit data comparison		 • Conductive status when $(S1) = (S2)$ • Non-conductive status when $(S1) \neq (S2)$
		 • Conductive status when $(S1) \neq (S2)$ • Non-conductive status when $(S1) = (S2)$
		 • Conductive status when $(S1) > (S2)$ • Non-conductive status when $(S1) \leq (S2)$
		 • Conductive status when $(S1) \leq (S2)$ • Non-conductive status when $(S1) > (S2)$
		 • Conductive status when $(S1) < (S2)$ • Non-conductive status when $(S1) \geq (S2)$
		 • Conductive status when $(S1) \geq (S2)$ • Non-conductive status when $(S1) < (S2)$
32-bit data comparison		 • Conductive status when $(S1 + 1, S1) = (S2 + 1, S2)$ • Non-conductive status when $(S1 + 1, S1) \neq (S2 + 1, S2)$
		 • Conductive status when $(S1 + 1, S1) \neq (S2 + 1, S2)$ • Non-conductive status when $(S1 + 1, S1) = (S2 + 1, S2)$
		 • Conductive status when $(S1 + 1, S1) > (S2 + 1, S2)$ • Non-conductive status when $(S1 + 1, S1) \leq (S2 + 1, S2)$
		 • Conductive status when $(S1 + 1, S1) \leq (S2 + 1, S2)$ • Non-conductive status when $(S1 + 1, S1) > (S2 + 1, S2)$
		 • Conductive status when $(S1 + 1, S1) < (S2 + 1, S2)$ • Non-conductive status when $(S1 + 1, S1) \geq (S2 + 1, S2)$
		 • Conductive status when $(S1 + 1, S1) \geq (S2 + 1, S2)$ • Non-conductive status when $(S1 + 1, S1) < (S2 + 1, S2)$

Classification	Symbol	Description
Real number data comparison		 • Conductive status when $(S1 + 1, S1) = (S2 + 1, S2)$ • Non-conductive status when $(S1 + 1, S1) \neq (S2 + 1, S2)$
		 • Conductive status when $(S1 + 1, S1) \neq (S2 + 1, S2)$ • Non-conductive status when $(S1 + 1, S1) = (S2 + 1, S2)$
		 • Conductive status when $(S1 + 1, S1) > (S2 + 1, S2)$ • Non-conductive status when $(S1 + 1, S1) \leq (S2 + 1, S2)$
		 • Conductive status when $(S1 + 1, S1) \geq (S2 + 1, S2)$ • Non-conductive status when $(S1 + 1, S1) < (S2 + 1, S2)$
		 • Conductive status when $(S1 + 1, S1) < (S2 + 1, S2)$ • Non-conductive status when $(S1 + 1, S1) \geq (S2 + 1, S2)$
		 • Conductive status when $(S1 + 1, S1) \leq (S2 + 1, S2)$ • Non-conductive status when $(S1 + 1, S1) > (S2 + 1, S2)$

Classification	Symbol	Description
Character string data comparison		Compares character strings (S1) and (S2) character by character. Condition for "match": Character string in which all characters match Condition for "larger character string": Character string that includes characters with larger character codes, or the longer character string Condition for "smaller character string": Character string that includes characters with smaller character codes, or the shorter character string
		- Conductive status when (character string S1) = (character string S2) - Non-conductive status when (character string S1) ≠ (character string S2)  - Conductive status when (S1 + 1, S1) ≠ (S2 + 1, S2) - Non-conductive status when (S1 + 1, S1) = (S2 + 1, S2)  - Conductive status when (character string S1) > (character string S2) - Non-conductive status when (character string S1) ≤ (character string S2)
		 - Conductive status when (character string S1) < (character string S2) - Non-conductive status when (character string S1) ≠ (character string S2)  - Conductive status when (character string S1) ≥ (character string S2) - Non-conductive status when (character string S1) < (character string S2)  - Conductive status when (character string S1) ≤ (character string S2) - Non-conductive status when (character string S1) > (character string S2)

Classification	Symbol	Description
Block data comparison	BKCMPE(P) S1 S2 D n	Compares n points of data from (S1) with n points of data from (S2) in 1 word units, and stores the comparison result in the n points starting from the bit device specified by (D).
	BKCMPL(P) S1 S2 D n	
	BKCMPL(P) S1 S2 D n	
	BKCMPL(P) S1 S2 D n	
	BKCMPL(P) S1 S2 D n	
	BKCMPL(P) S1 S2 D n	

(2) Arithmetic operation instructions

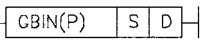
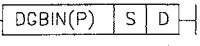
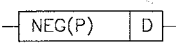
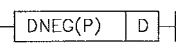
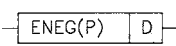
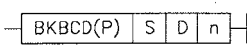
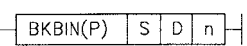
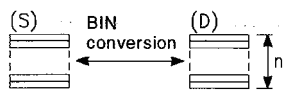
Classification	Symbol	Description
BIN 16-bit addition/ subtraction		• $(D) + (S) \rightarrow (D)$
		• $(S1) + (S2) \rightarrow (D)$
		• $(D) - (S) \rightarrow (D)$
		• $(S1) - (S2) \rightarrow (D)$
BIN 32-bit addition/ subtraction		• $(D+1, D) + (S+1, S) \rightarrow (D+1, D)$
		• $(S1+1, S1) + (S2+1, S2) \rightarrow (D+1, D)$
		• $(D+1, D) - (S+1, S) \rightarrow (D+1, D)$
		• $(S1+1, S1) - (S2+1, S2) \rightarrow (D+1, D)$
BIN 16-bit multiplication/division		• $(S1) \times (S2) \rightarrow (D+1, D)$
		• $(S1)/(S2) \rightarrow \text{quotient } (D), \text{ remainder } (D+1)$
BIN 32-bit multiplication/division		• $(S1+1, S1) \times (S2+1, S2) \rightarrow (D+3, D+2, D+1, D)$
		• $(S1+1, S1)/(S2+1, S2) \rightarrow \text{quotient } (D+1, D), \text{ remainder } (D+3, D+2)$

Classification	Symbol	Description
BCD 4-digit addition/ subtraction	$\boxed{B+(P)} \quad \boxed{S} \quad \boxed{D}$	• $(D) + (S) \rightarrow (D)$
	$\boxed{B+(P)} \quad \boxed{S1} \quad \boxed{S2} \quad \boxed{D}$	• $(S1) + (S2) \rightarrow (D)$
	$\boxed{B-(P)} \quad \boxed{S} \quad \boxed{D}$	• $(D) - (S) \rightarrow (D)$
	$\boxed{B-(P)} \quad \boxed{S1} \quad \boxed{S2} \quad \boxed{D}$	• $(S1) - (S2) \rightarrow (D)$
BCD 8-digit addition/ subtraction	$\boxed{DB+(P)} \quad \boxed{S} \quad \boxed{D}$	• $(D+1, D) + (S+1, S) \rightarrow (D+1, D)$
	$\boxed{DB+(P)} \quad \boxed{S1} \quad \boxed{S2} \quad \boxed{D}$	• $(S1+1, S1) + (S2+1, S2) \rightarrow (D+1, D)$
	$\boxed{DB-(P)} \quad \boxed{S} \quad \boxed{D}$	• $(D+1, D) - (S+1, S) \rightarrow (D+1, D)$
	$\boxed{DB-(P)} \quad \boxed{S1} \quad \boxed{S2} \quad \boxed{D}$	• $(S1+1, S1) - (S2+1, S2) \rightarrow (D+1, D)$
BCD 4-digit multiplication/division	$\boxed{B*(P)} \quad \boxed{S1} \quad \boxed{S2} \quad \boxed{D}$	• $(S1) \times (S2) \rightarrow (D+1, D)$
	$\boxed{B/(P)} \quad \boxed{S1} \quad \boxed{S2} \quad \boxed{D}$	• $(S1)/(S2) \rightarrow \text{quotient } (D), \text{ remainder } (D+1)$
BCD 8-digit multiplication/division	$\boxed{DB*(P)} \quad \boxed{S1} \quad \boxed{S2} \quad \boxed{D}$	• $(S1+1, S1) \times (S2+1, S2) \rightarrow (D+3, D+2, D+1, D)$
	$\boxed{DB/(P)} \quad \boxed{S1} \quad \boxed{S2} \quad \boxed{D}$	• $(S1+1, S1)/(S2+1, S2) \rightarrow \text{quotient } (D+1, D), \text{ remainder } (D+3, D+2)$
Floating point data addition/subtraction	$\boxed{E+(P)} \quad \boxed{S} \quad \boxed{D}$	• $(D+1, D) + (S+1, S) \rightarrow (D+1, D)$
	$\boxed{E+(P)} \quad \boxed{S1} \quad \boxed{S2} \quad \boxed{D}$	• $(S1+1, S1) + (S2+1, S2) \rightarrow (D+1, D)$
	$\boxed{E-(P)} \quad \boxed{S} \quad \boxed{D}$	• $(D+1, D) - (S+1, S) \rightarrow (D+1, D)$
	$\boxed{E-(P)} \quad \boxed{S1} \quad \boxed{S2} \quad \boxed{D}$	• $(S1+1, S1) - (S2+1, S2) \rightarrow (D+1, D)$

Classification	Symbol	Description
Floating point data multiplication/division		• $(S1+1, S1) \times (S2+1, S2) \rightarrow (D+1, D)$
		• $(S1+1, S1)/(S2+1, S2) \rightarrow \text{quotient } (D+1, D)$
Character string data addition		• Associates the character string specified at (S) to the character string specified at (D) and stores the result to devices starting from (D).
		• Associates the character string specified at (S2) to the character string specified at (S1) and stores the result to devices starting from (D).
BIN block addition/subtraction		• Adds n points of data from (S1) and n points of data from (S2) in a batch and stores the result to devices starting from (D).
BIN data increment		• $(D) + 1 \rightarrow (D)$
		• $(D+1, D) + 1 \rightarrow (D)$
BIN data decrement		• $(D) - 1 \rightarrow (D)$
		• $(D+1, D) - 1 \rightarrow (D)$

(3) Data conversion instructions

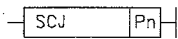
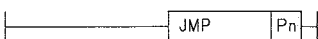
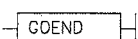
Classification	Symbol	Description
BCD conversion		• (S) $\xrightarrow{\text{BCD conversion}}$ (D) BIN (0 to 9999)
		• (S + 1, S) $\xrightarrow{\text{BCD conversion}}$ (D + 1, D) BIN (0 to 99999999)
BIN conversion		• (S) $\xrightarrow{\text{BIN conversion}}$ (D) BCD (0 to 9999)
		• (S + 1, S) $\xrightarrow{\text{BIN conversion}}$ (D + 1, D) BCD (0 to 99999999)
Floating point → BIN conversion		• (S + 1, S) $\xrightarrow{\text{BIN conversion}}$ (D) Real number (–32768 to 32767)
		• (S + 1, S) $\xrightarrow{\text{BIN conversion}}$ (D) Real number (–2147483648 to 2147483647)
BIN → floating point conversion		• (S + 1, S) $\xrightarrow{\text{Floating decimal point conversion}}$ (D) Real number (–32768 to 32767)
		• (S + 1, S) $\xrightarrow{\text{Floating decimal point conversion}}$ (D + 1, D) Real number (–2147483648 to 2147483647)
BIN 16-bit ↔ 32-bit conversion		• (S) $\xrightarrow{\text{Conversion to 32-bit data}}$ (D + 1, D) BIN (–32768 to 32767)
		• (S + 1, S) $\xrightarrow{\text{16-bit data conversion}}$ (D) BIN (–32768 to 32767)
BIN → gray code conversion		• (S) $\xrightarrow{\text{Gray code conversion}}$ (D) BIN (–32768 to 32767)
		• (S + 1, S) $\xrightarrow{\text{Gray code conversion}}$ (+1, DD) BIN (–32768 to 32767)

Classification	Symbol	Description
Gray code → BIN conversion		• (S) $\xrightarrow{\text{Gray code conversion}}$ (D) Gray code (-32768 to 32767)
		• $(S + 1, S)$ $\xrightarrow{\text{Gray code conversion}}$ $(D + 1, D)$ Gray code (-2147483648 to 2147483647)
2's complement		• (D) $\xrightarrow{\text{BIN data}}$ (D) BIN data
		• $(D + 1, D)$ $\xrightarrow{\text{BIN data}}$ $(D + 1, D)$ BIN data
		• $(D + 1, D)$ $\xrightarrow{\text{Real number data}}$ $(D + 1, D)$ Real number data
Block conversion		• Converts n points of BIN data from (S) to BCD data in a batch and stores the result to devices starting from (D). 
		• Converts n points of BCD data from (S) to BIN data in a batch and stores the result to devices starting from (D). 

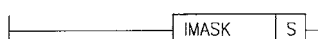
(4) Data transfer instructions

Classification	Symbol	Description
16-bit data transfer	MOV(P) S D	• (S) $\longrightarrow$ (D)
32-bit data transfer	DMOV(P) S D	• (S+1, S) $\longrightarrow$ (D+1, D)
Floating point data transfer	EMOV(P) S D	• (S+1, S) $\longrightarrow$ (D+1, D)
Character string data transfer	\$MOV(P) S D	• Transfers the character string specified at (S) to devices starting with the device specified at (D).
16-bit data negation transfer	CML(P) S D	• $\overline{(S)}$ $\longrightarrow$ $\overline{(D)}$
32-bit data negation transfer	DCML(P) S D	• $\overline{(S+1, S)}$ $\longrightarrow$ (D+1, D)
Data block transfer	BMOV(P) S D n	(S) $\longrightarrow$ (D) $\updownarrow$ n
Same data block transfer	FMOV(P) S D n	(S) $\longrightarrow$ (D) $\updownarrow$ n
16-bit data exchange	XCH(P) S D	• (S) $\longleftrightarrow$ (D)
32-bit data exchange	DXCH(P) S D	• (S+1, S) $\longleftrightarrow$ (D+1, D)
Block data exchange	BXCH(P) S D n	(S) $\longleftrightarrow$ (D) $\updownarrow$ n
Upper/lower byte swap	SWAP(P) S D	b15 to b8b7 to b0 (S) 8 bits 8 bits $\swarrow \searrow$ b15 to b8b7 to b0 (D) 8 bits 8 bits

(5) Program branch instructions

Classification	Symbol	Description
Jump		• Causes a jump to Pn when the input condition is met.
		• Causes a jump to Pn beginning with the scan after the one in which the input condition is met.
		• Causes a jump to Pn unconditionally.
		• Causes a jump to the END instruction when the input condition is met.

(6) Program execution control instructions

Classification	Symbol	Description
Interrupt disable		• Disables execution of interrupt programs.
Interrupt enable		• Cancels the execution disabled status for interrupt programs.
Interrupt disable/ enable setting		• Disables or enables execution of individual interrupt programs.
Return		• Returns from the interrupt program to the sequence program.

(7) I/O refresh instruction

Classification	Symbol	Description
I/O refresh		• Executes partial refresh for the specified I/O part in a scan.

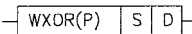
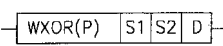
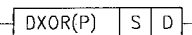
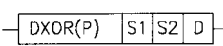
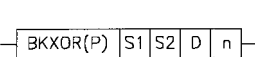
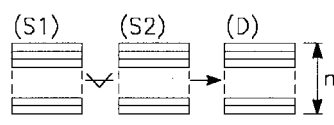
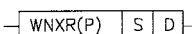
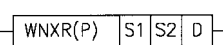
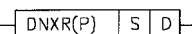
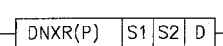
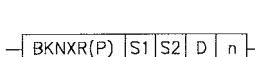
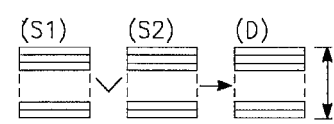
(8) Other convenient instructions

Classification	Symbol	Description
Up/down counter		Cn present value: 0 1 2 3 4 5 6 7 6 5 4 3 2 1 0 -1 -2 -3 -2 -1 0 Cn contact
		Cn present value: 0 1 2 3 4 5 4 3 2 1 0 -1 Cn contact
Teaching timer		• $(TTMR \text{ ON time}) \times n \rightarrow (D)$ ↑ $n=0:1, \quad n=0:10, \quad n=2:100$
Special timer		• Four bit devices starting with the bit device specified at (D) perform the following operations in accordance with the ON/OFF status of the STMR instruction. (D) + 0: Off delay timer output (D) + 1: One shot timer output after OFF (D) + 2: One shot timer output after ON (D) + 3: On delay timer
Shortest path control		• Rotates a rotary table that is partitioned into n1 from the position at which it is stopped to the position specified by (S+1) in the direction that gives the shortest path.
Ramp signal		• Changes the device data specified at (D1) in the range of n1 to n2 in n3 scans.
Pulse density		• Counts the pulse input of the device specified at (S) for the time specified at n and stores the result in the device specified at (D).
Pulse output		• $(n1)\text{Hz} \rightarrow (D)$ - Outputs "n2" times.
Pulse width modulation		(D)
Matrix input		• Consecutively reads the data of n rows of 16 devices starting from the device specified at (S1) and stores it in devices starting from the device specified at (D2).

Appendix 1.3 Application Instructions

(1) Logical operation instructions

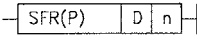
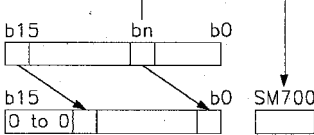
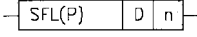
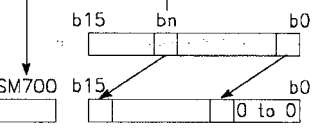
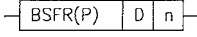
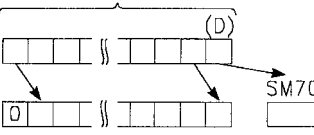
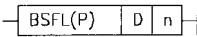
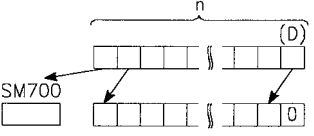
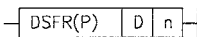
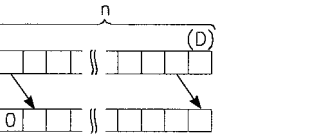
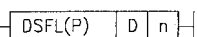
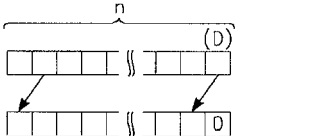
Classification	Symbol	Description
Logical product		$\bullet (D) \wedge (S) \rightarrow (D)$
		$\bullet (S1) \wedge (S2) \rightarrow (D)$
		$\bullet (D+1, D) \wedge (S+1, S) \rightarrow (D+1, D)$
		$\bullet (S1+1, S1) \wedge (S2+1, S2) \rightarrow (D+1, D)$
Logical sum		$\bullet (D) \vee (S) \rightarrow (D)$
		$\bullet (S1) \vee (S2) \rightarrow (D)$
		$\bullet (D+1, D) \vee (S+1, S) \rightarrow (D+1, D)$
		$\bullet (S1+1, S1) \vee (S2+1, S2) \rightarrow (D+1, D)$

Classification	Symbol	Description
Exclusive logical sum		• $(D) \nabla (S) \rightarrow (D)$
		• $(S1) \nabla (S2) \rightarrow (D)$
		• $(D+1, D) \nabla (S+1, S) \rightarrow (D+1, D)$
		• $(S1+1, S1) \nabla (S2+1, S2) \rightarrow (D+1, D)$
		
Not exclusive logical sum		• $\overline{(D) \nabla (S)} \rightarrow (D)$
		• $\overline{(S1) \nabla (S2)} \rightarrow (D)$
		• $\overline{(D+1, D) \nabla (S+1, S)} \rightarrow (D+1, D)$
		• $\overline{(S1+1, S1) \nabla (S2+1, S2)} \rightarrow (D+1, D)$
		

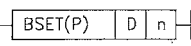
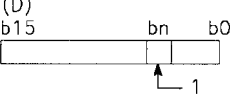
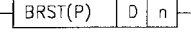
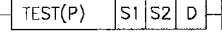
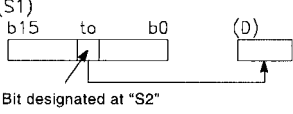
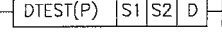
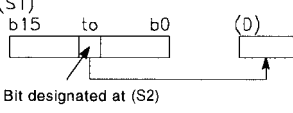
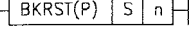
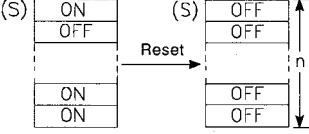
(2) Rotation instructions

Classification	Symbol	Description
Right rotation		Rotates "n" bits to the right.
		Rotates "n" bits to the right.
Left rotation		Rotates "n" bits to the left.
		Rotates "n" bits to the left.
Right rotation		Rotates "n" bits to the right.
		Rotates "n" bits to the right.
Left rotation		Rotates "n" bits to the left.
		Rotates "n" bits to the left.

(3) Shift instructions

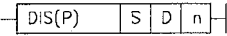
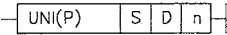
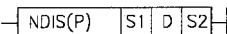
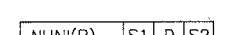
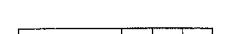
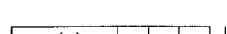
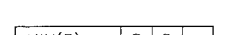
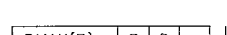
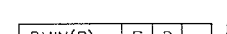
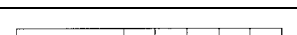
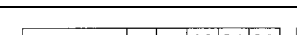
Classification	Symbol	Description
n bit shift		
		
1 bit shift		
		
1 word shift		
		

(4) Bit processing instructions

Classification	Symbol	Description
Bit set/reset		
		
Bit test		 Bit designated at "S2"
		 Bit designated at (S2)
Bit device batch reset		

(5) Data processing instructions

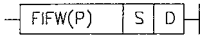
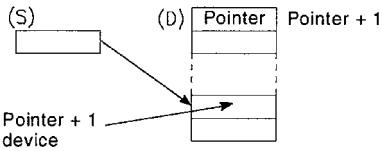
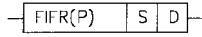
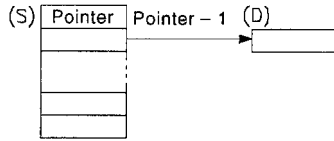
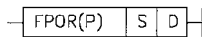
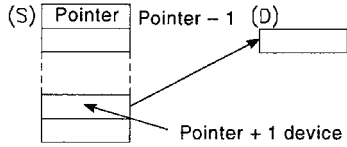
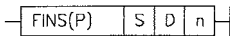
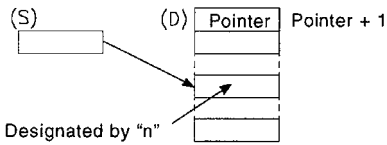
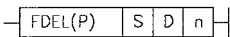
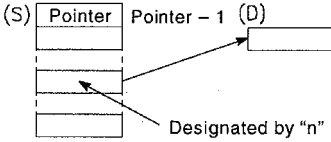
Classification	Symbol	Description
Data search		(D) : Coinciding position (D+1) : Coinciding quantity
		(D) : Coinciding position (D+1) : Coinciding quantity
Bit check		(D): Quantity of 1
		(D): Quantity of 1
Decode		8 → 256 decode (D) : 2ⁿ bits
Encode		256 → 8 decode (D) : 8 bits
7-segment decode		(D) : 7SEG

Classification	Symbol	Description
Dissociation/ Association		Dissociates the 16-bit data specified at (S) into 4-bit units, and stores these data in the least significant four bits of n devices starting with the one specified at (D). ($n \leq 4$)
		Associates the least significant 4-bit data of n devices starting from the one specified at (S) and stores this data in the device specified at (D). ($n \leq 4$)
		Dissociates data of the devices starting with the one specified at (S1) into the specified bits starting with the one specified by (S2), and stores this data in sequence starting at the device specified at (D).
		Associates each of the data starting from the one specified at (S1) to the data of the devices starting from the one specified by (S2) and stores the data to the devices in sequence starting at the device specified at (D).
		Dissociates the 16-bit data that starts from the device specified at (S) into 8-bit units, and stores the n points of data to the devices in sequence starting from the one specified at (D).
		Associates the lower 8 bits of 16-bit data for n points starting from the one specified at (S) to give 16-bit data, and stores the data to the devices in sequence starting from the one specified at (D).
Search		Searches the n points of data starting from the device specified at (S) in 16-bit units, and stores the maximum value to the device specified at (D).
		Searches the n points of data starting from the device specified at (S) in 16-bit units, and stores the minimum value to the device specified at (D).
		Searches the $2 \times n$ points of data starting from the device specified at (S) in 32-bit units, and stores the maximum value to the device specified at (D).
		Searches the $2 \times n$ points of data starting from the device specified at (S) in 32-bit units, and stores the minimum value in the device specified at (D).
Sort	 - S2: Number of comparisons executed at one time - D1: Device turned ON on completion of sorting - D2: For system use	- Sorts n points of data starting from the device specified at (S1) in 16-bit units. [Max. number of scans required: $\{n \times (n - 1)\}/2$ scans]
	 - S2: Number of comparisons executed at one time - D1: Device turned ON on completion of sorting - D2: For system use	- Sorts $2 \times n$ points of data starting from the device specified at (S1) in 32-bit units. [Max. number of scans required: $\{n \times (n - 1)\}/2$ scans]

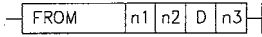
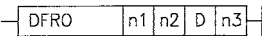
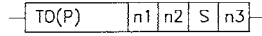
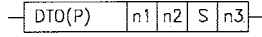
(6) Structured program instruction

Classification	Symbol	Description
Repeat		Executes the program section between FOR and NEXT n times.
		Forcibly ends execution of the program section between FOR and NEXT and causes a jump to Pn.
Subroutine program call		Executes the subroutine program Pn when the input condition is met. (S1 to Sn are arguments for the subroutine program. $0 \leq n \leq 5$)
		Causes a return from the subroutine program.
		Executes no-execution processing for the subroutine program Pn when the input condition is not met.
		Executes the subroutine program Pn of the specified program when the input condition is met. (S1 to Sn are arguments for the subroutine program. $0 \leq n \leq 5$)
		Executes no-execution processing for the subroutine program Pn of the specified program when the input condition is not met.
		Executes link refresh and general data processing.
Ladder indexing		Indexes each of the devices used in the device qualification ladder.
		Stores the qualification value for indexing at IX to IXEND to the devices starting from the one specified at (D).

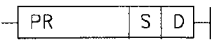
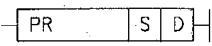
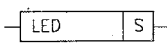
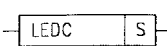
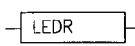
(7) Table operation instructions

Classification	Symbol	Description
Table processing		
		
		
		
		

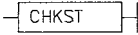
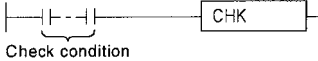
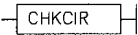
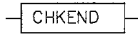
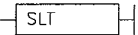
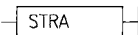
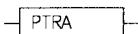
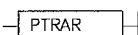
(8) Buffer memory access instructions

Classification	Symbol	Description
Data read		• Reads data in 16-bit units from special function modules.
		• Reads data in 32-bit units from special function modules.
Data write		• Writes data in 16-bit units to special function modules.
		• Writes data in 32-bit units to special function modules.

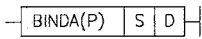
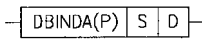
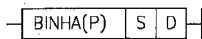
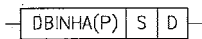
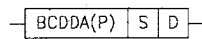
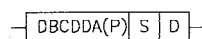
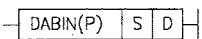
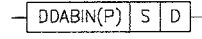
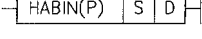
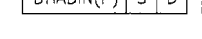
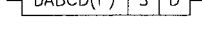
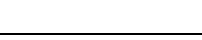
(9) Display instructions

Classification	Symbol	Description
ASCII print	* When SM701 is OFF 	Outputs ASCII codes in the 8 points of devices (16 characters) starting from the one specified at (S) to an output module.
	* When SM701 is ON 	Outputs ASCII codes in the devices starting from the one specified at (S) and ending at 00H, to an output module.
		Converts the device comment specified at (S) to ASCII codes and outputs the result to an output module.
Display		Displays ASCII codes in the 8 points of devices (corresponding to 16 characters) starting from the one specified at (S) on the LED indicator.
		Displays the comment of the device specified at (S) on the LED indicator.
Reset		Resets annunciators and LED indication.

(10) Debugging and fault diagnostics instructions

Classification	Symbol	Description
Error check		• Executes the CHK instruction when it is executed. • Causes a jump to the step following the step of the CHK instruction when it is not executed.
		• When normal → SM80: OFF, SD80: 0 • When abnormal → SM80: ON, SD80: fault No.
		• Indicates the start of ladder pattern change for the ladders to be checked with the CHK instruction.
		• Indicates the end of ladder pattern change for the ladders to be checked with the CHK instruction.
Status latch		• Executes status latch.
		• Resets the status latch to enable re-execution of status latch.
Sampling trace		• Triggers sampling trace.
		• Resets the sampling trace to enable re-execution of sampling trace.
Program trace		• Triggers program trace.
		• Resets the program trace to enable re-execution of program trace.
		• Executes program trace.

(11) Text string processing instructions

Classification	Symbol	Description
BIN ↓ Decimal ASCII		• Converts the 1-word BIN data specified at (S) into 5-digit decimal ASCII values, and stores them to the word devices starting from the one specified at (D).
		• Converts the 2-word BIN data specified at (S) into 10-digit decimal ASCII values, and stores them to the word devices starting from the one specified at (D).
BIN ↓ Hexadecimal ASCII		• Converts the 1-word BIN data specified at (S) into 4-digit hexadecimal ASCII values, and stores them to the word devices starting from the one specified at (D).
		• Converts the 2-word BIN data specified at (S) into 8-digit hexadecimal ASCII values, and stores them to the word devices starting from the one specified at (D).
BCD ↓ ASCII		• Converts the 1-word BCD value specified at (S) into 4-digit decimal ASCII values, and stores them to the word devices starting from the one specified at (D).
		• Converts the 2-word BCD value specified at (S) into 8-digit decimal ASCII values, and stores them to the word devices starting from the one specified at (D).
Decimal ASCII ↓ BIN		• Converts the 5-digit decimal ASCII value specified at (S) to a 1-word BIN value, and stores this to the word device specified at (D).
		• Converts the 10-digit decimal ASCII values specified at (S) to a 2-word BIN value, and stores this to the word device specified at (D).
Hexadecimal ASCII ↓ BIN		• Converts the 4-digit hexadecimal ASCII values specified at (S) to a 1-word BIN value, and stores this to the word device specified at (D).
		• Converts the 8-digit decimal ASCII values designated at (S) to a 2-word BIN value, and stores this at the word device number designated at (D).
ASCII ↓ BCD		• Converts the 4-digit decimal ASCII values specified at (S) to a 1-word BCD value, and stores this to the word device specified at (D).
		• Converts the 8-digit decimal ASCII values specified at (S) to a 2-word BCD value, and stores this to the word devices specified at (D).
Device comment read		• Stores the comment data of the device specified at (S) to the device specified at (D).
Text string length detection		• Stores the length of the character string data (number of characters) that is stored in the device specified at (S) to the device specified at (D).

Classification	Symbol	Description
BIN ↓ Decimal text string		• Converts the 1-word BIN value specified at (S2) into a decimal character string with the total number of digits and number of fraction part digits specified at (S1), and stores it in the device specified at (D).
		• Converts the 2-word BIN value specified at (S2) into a decimal character string with the total number of digits and number of fraction part digits specified at (S1), and stores it in the device specified at (D).
Decimal text string ↓ BIN		• Converts the character string that includes a decimal point specified at (S) to a 1-word BIN value and the number of fraction part digits, and stores them to the devices specified at (D1) and (D2).
		• Converts the character string that includes a decimal point specified at (S) to a 2-word BIN value and the number of fraction part digits, and stores them to the devices specified at (D1) and (D2).
Floating point ↓ Character string		• Converts the floating point data specified at (S) to a character string and stores it in the devices specified at (D).
Character string ↓ Floating decimal point		• Converts the character string specified at (S) to a floating point data and stores it in the devices specified at (D).
Hexadecimal BIN ↓ ASCII		• Converts the 1-word BIN value in the devices starting from the one specified at (S) to hexadecimal ASCII data, and stores them to the word devices starting from the one specified at (D) for n characters.
ASCII ↓ Hexadecimal BIN		• Converts the hexadecimal ASCII data in the devices starting from the one specified at (S) to BIN values for n characters, and stores them to the devices starting from the one specified at (D).
Character string processing		• Stores n characters from the final character of the character string specified at (S) to the devices specified at (D).
		• Stores n characters from the initial character of the character string specified at (S) to the devices specified at (D).
		• Stores the specified number of characters from the position specified at (S2) of the character string specified at (S1) to the devices specified at (D).
		• Stores the character string specified at (S1) for the specified number of characters to the position specified at (S2) of the devices specified at (D).
		• Searches for the character string specified at (S1) from the nth character of the character string specified at (S2) and stores the position where a match is found to (D).
Floating point data ↓ BCD resolution		• Converts the floating point data specified at (S1) to a BCD data with the number of fraction part digits specified at (S2), and stores this data to the devices specified at (D).

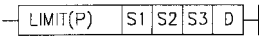
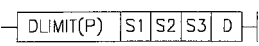
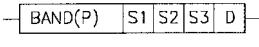
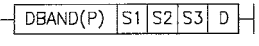
Classification	Symbol	Description
BCD ↓ Floating point data	— EREXP(P) S1 S2 D —	Converts the BCD data specified at (S1) to a floating point data with the number of fraction part digits specified at (S2) and stores this data to the devices specified at (D).

(12) Special function instructions

Classification	Symbol	Description
Trigonometric function (floating point data)		• $\text{Sin}(S+1, S) \rightarrow (D+1, D)$
		• $\text{Cos}(S+1, S) \rightarrow (D+1, D)$
		• $\text{Tan}(S+1, S) \rightarrow (D+1, D)$
		• $\text{Sin}^{-1}(S+1, S) \rightarrow (D+1, D)$
		• $\text{Cos}^{-1}(S+1, S) \rightarrow (D+1, D)$
		• $\text{Tan}^{-1}(S+1, S) \rightarrow (D+1, D)$
Degree $\longleftrightarrow$ radian conversion		• $(S + 1, S) \rightarrow (D + 1, D)$ Degree $\rightarrow$ radian conversion
		• $(S + 1, S) \rightarrow (D + 1, D)$ Radian $\rightarrow$ degree conversion
		• $\sqrt{(S + 1, S)} \rightarrow (D + 1, D)$
Exponent operation		• $e^{(S + 1, S)} \rightarrow (D + 1, D)$
Natural logarithm		• $\text{Log } e(S + 1, S) \rightarrow (D + 1, D)$
Square root		• $\sqrt{(S)} \rightarrow (D) + 0$ + 1 Integer part Fraction part
		• $\sqrt{(S + 1, S)} \rightarrow (D) + 0$ + 1 Integer part Fraction part

Classification	Symbol	Description
Trigonometric function		• Sin (S) → (D) + 0 + 1 + 2 Sign Integer part Fraction part
		• Cos (S) → (D) + 0 + 1 + 2 Sign Integer part Fraction part
		• Tan (S) → (D) + 0 + 1 + 2 Sign Integer part Fraction part
		• Sin⁻¹ (S) → (D) + 0 + 1 + 2 Sign Integer part Fraction part
		• Cos⁻¹ (S) → (D) + 0 + 1 + 2 Sign Integer part Fraction part
		• Tan⁻¹ (S) → (D) + 0 + 1 + 2 Sign Integer part Fraction part

(13) Data control instructions

Classification	Symbol	Description
Upper/lower limit control		- Processes the value specified at (S3) to a data in the range defined by the upper and lower limits set at (S1) and (S2), and stores it to the word device specified at (D). - When $S3 < S1$ The value at (S1) is stored to (D). - When $S1 \leq S3 \leq S2$ The value at (S3) is stored to (D). - When $S2 < S3$ The value at (S2) is stored to (D).
		- Processes the value specified at (S3+1, S3) to a data in the range defined by the upper and lower limits set at (S1+1, S1) and (S2+1, S2), and stores it to the word device specified at (D+1, D). - When $(S3+1, S3) < (S1+1, S1)$ The value at (S1+1, S1) is stored to (D+1, D). - When $(S1+1, S1) \leq (S3+1, S3) \leq (S2+1, S2)$ The value at (S3+1, S3) is stored to (D+1, D). - When $(S2, S2+1) < (S3, S3+1)$ The value at (S2+1, S2) is stored to (D+1, D).
Dead zone control		- Taking the area set by (S1) and (S2) as the dead band, if the input value specified at (S3) is within the dead band, "0" is stored to the word device specified at (D) and if it is outside the dead band, the value obtained by subtracting the dead band upper/lower limit value from the input value is stored to the word device specified at (D). - When $S1 \leq S3 \leq S2$ $0 \rightarrow D$ - When $S3 < S1$ $S3 - S1 \rightarrow D$ - When $S3 > S2$ $S3 - S2 \rightarrow D$
		- Taking the area set by (S1+1, S1) and (S2+1, S2) as the dead band, if the input value specified at (S3+1, S3) is within the dead band, "0" is stored to the word device specified at (D) and if it is outside the dead band, the value obtained by subtracting the dead band upper/lower limit value from the input value is stored to the word device specified at (D). - When $(S1+1, S1) \leq (S3+1, S3) \leq (S2+1, S2)$ $0 \rightarrow (D+1, D)$ - When $(S3+1, S3) < (S1+1, S1)$ $(S3+1, S3) - (S1+1, S1) \rightarrow (D+1, D)$ - When $(S3+1, S3) > (S2+1, S2)$ $(S3+1, S3) - (S2+1, S2) \rightarrow (D+1, D)$

Classification	Symbol	Description
Zone control		- By setting positive and negative bias values for the input value specified at (S3) with (S1) and (S2), calculates the value for S1 + bias, and stores it to the word device specified at (D). - When $S3 = 0$: $0 \rightarrow D$ - When $S3 > 0$: $S3 + S2 \rightarrow D$ - When $S3 < 0$: $S3 - S1 \rightarrow D$
		- By setting positive and negative bias values for the input value specified at (S3+1, S3) with (S1+1, S1) and (S2+1, S2), calculates the value for S1 + bias, and stores it to the word device specified at (D+1, D). - When $(S3+1, S3) = 0$: $0 \rightarrow (D+1, D)$ - When $(S3+1, S3) > 0$: $(S3+1, S3) - (S2+1, S2) \rightarrow (D+1, D)$ - When $(S3+1, S3) < 0$: $(S3+1, S3) + (S1+1, S1) \rightarrow (D+1, D)$

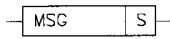
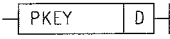
(14) Switching instructions

Classification	Symbol	Description
Block No. setting		Changes the block No. of an extension file register to the number specified at (S).
		Sets the name of a file to be used as a file register.
		Sets the name of a file to be used as a comment register.

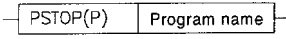
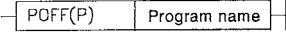
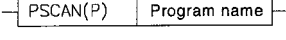
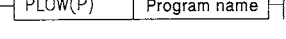
(15) Clock instructions

Classification	Symbol	Description
Clock data read/write	DATE RD(P) D	• (Clock element)→(D) + 0 + 1 + 2 + 3 + 4 + 5 + 6 Year Month Day Hour Minute Second Day of the week
	DATE WR(P) S	• (S) + 0 + 1 + 2 + 3 + 4 + 5 + 6 Year Month Day Hour Minute Second Day of the week → (Clock element)
	DATE +(P) S1 S2 D	(S1) Hour Minute Second + (S2) Hour Minute Second → (D) Hour Minute Second
	DATE -(P) S1 S2 D	(S1) Hour Minute Second - (S2) Hour Minute Second → (D) Hour Minute Second
	SECOND(P) S D	(S) Hour Minute Second → (D) Second (Lower level) Second (Upper level)
	HOUR(P) S D	(S) Second (Lower level) Second (Upper level) → (D) Hour Minute Second

(16) Instructions for peripheral devices

Classification	Symbol	Description
Input/output to peripheral device		Stores the message specified at (S) to the QnACPU. This message is displayed at the peripheral device.
		Stores the data input from a peripheral device to the device specified at (D).

(17) Program instructions

Classification	Symbol	Description
Program execution status switch		Sets the specified program in the standby status.
		Turns OFF the coil of the specified program's OUT instruction and sets the program to the standby status.
		Registers the specified program as a scan execution type program.
		Registers the specified program as a low-speed execution type program.

(18) Other instructions

Classification	Symbol	Description
WDT reset		Resets the WDT in a sequence program.
Timing clock		
Direct read/write in 1 byte unit		
Indirect address set		
Numeral key input from keyboard		Fetches ASCII data to the input module specified at (S) for 8 points, converts the data to hexadecimal values, and stores them in the devices starting with the one specified at (D1).

Appendix 1.4 Data Link Instructions

(1) Link refresh instructions

Classification	Symbol	Description
Specified network refresh	J(P).ZCOM Jn	• Performs link refresh for the network module corresponding to the specified network No. in network n.
	G(P).ZCOM Un	• Refreshes the network module corresponding to the specified I/O number in network n.

(2) QnA link dedicated instructions

Classification	Symbol	Description
Data read/write from/to other stations		• Reads data from word devices of another station.
		• Writes data to word devices of another station.
Data send/receive to/from other stations		• Sends data (message) to another station.
		• Receives data (message) from another station.
Processing request to other stations		Executes remote RUN/STOP for another station.
Data read/write from/to a special function module at a remote I/O station		Reads data from a special function module installed at a remote station in the MELSECNET/10 network.
		Writes data to a special function module at a remote I/O station in the MELSECNET/10 network.

* (The GP. *** instructions can also be used for the AJ71QC24N)

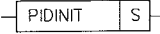
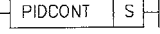
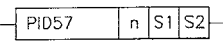
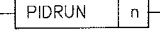
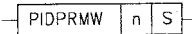
(3) A series link instructions

Classification	Symbol	Description
Word device read from specified station		Reads the data of T, C, D, and W devices of other stations in the MELSECNET(II) or MELSECNET/10 system.
Word device write to specified station		Reads the data of T, C, D, and W devices of other stations on the MELSECNET(II) or MELSECNET/10 network.
Data read/write from a special function module at a remote I/O station		Reads data from the special function module installed at a remote I/O station in the MELSECNET(II) system.
		Writes data to the special function module installed at a remote I/O station in the MELSECNET(II) system.

(4) Routing parameter instructions

Classification	Symbol	Description
Routing information read		Reads the data of the transfer destination network with the number specified by n in the routing parameters and stores the data to the devices starting from (D).
Routing information registration		Registers the routing data in the devices starting from (S) to the area for the transfer destination network with the number specified by n in the parameters.

Appendix 1.5 PID Control Instructions

Classification	Symbol	Description
PID control data set		Registers the PID control data in the devices starting from the one specified at (S) to the PLC CPU.
PID control execution		Performs PID operation on the basis of the set value (SV) and process value (PV) set in the devices starting from the one specified at (S), and stores the operation result in the manipulated value (MV) area.
PID control status monitor		Displays, in the form of a bar graph, the PID control status of the loop with the number specified at (S1) on the display for the AD57 specified at n. At the start of execution of PID control monitor, static image elements of other than the bar graph and numerical data are displayed by issuing the initial screen display request specified at (S2).
Specified loop operation stop		Stops operation for the loop whose number is specified at n.
Specified loop operation start		Starts operation for the loop whose number is specified at n.
Specified loop parameter change		Changes the operation parameters of the loop whose number is specified at n to the data set in the devices starting from the one whose number is specified at (S).

Appendix 1.6 Special Function Module Instructions

(1) Instructions compatible with all versions

The following instructions can be used for modules with all versions.

Classification	Function	Instruction Symbol
AD61(S1) control instruction	Preset data setting	RVWR1, PVWR2
	Set value data setting for larger/smaller/ matched judgments	SVWR1, SVWR2
	Present value read	PVRD1, PVRD2
AD59(S1) control instruction	Character outputting for the intended number to a printer	PRN
	Character outputting up to the 00H code to a printer	PR
	Data read from memory card	GET
	Data write to memory card	PUT
AJ71C24 (-S3/S6/S8) control instruction	Data send for the specified number of bytes in no-protocol mode	PRN
	Data send up to the 00H code in no-protocol mode	PR
	Data receive in no-protocol mode	INPUT
	Communications status read	SPBUSY
	Send/receive processing forced interruption	SPCLR
AJ71C21(S1) control instruction	Data send for the specified number of bytes	PRN2, PRN4
	Data send up to the 00H code	PR2, PR4
	Data receive	INPUT2, INPUT4
	Data read from RAM memory	GET
	Data write to RAM memory	PUT
	Communication processing forced interruption	SPBUSY

Classification	Function	Instruction Symbol
AJ71PT32-S3 control instruction	Key input from operation box	INPUT
	Data send for the specified number of bytes in no-protocol mode	PRN
	Data send up to the 00H code in no-protocol mode	PR
	Data receive in no-protocol mode	INPUT
	Communications with remote terminal modules	MINI, MINIEND
	Error reset for remote terminal module	MINIERR
	Communications status read	SPBUSY
	Communication processing forced interruption	SPCLR

Classification	Function	Instruction Symbol
AD75 control instruction	Display mode setting	CMODE
	Canvas screen display	CPS1
	VRAM display address change	CPS2
	Canvas data transfer to the VRAM area	CMOV
	Display area clear	CLS
	VRAM area clear	CLV
	Screen scrolling	CSCRU, CSCRD
	Cursor display	CON1, CON2
	Cursor erase	COFF
	Cursor position setting	LOCATE
	Forward/reverse rotation specification for characters	CNOR, CREV
	Forward/reverse rotation switching for characters	CRDSP, SRDSPV
	Character display color specification	COLOR
	Character color change	CCDSP, CCDSPV
	ASCII character display	PR, PRN
	ASCII character write to VRAM	PRV, PRNV
	Character display	EPR, EPRN
	Character write to VRAM	EPRV, EPRNV
	Concatenated display of same character	CR1, CR2, CC1, CC2
	- (minus) display	CINMP
	- (hyphen) display	CINHP
	. (period, decimal point) display	CINPT
	Numeric character display	CIN0 to CIN9
	Alphabet character display	CINA to CINZ
	Space display	CINSP
	Specified column clear display	CINCLR
	ASCII code conversion of specified character strings	INPUT
	VRAM data read	GET
	VRAM data write	PUT
	Display status read	STAT

Classification	Function	Instruction Symbol
AJ71ID□-R4 control instruction	ID controller initial setting	IDINIT1, IDINIT2
	Data read from ID data carrier	IDRD1, IDRD2
	Data write to ID data carrier	IDWD1, IDWD2
	Continuous read from ID data carrier	IDARD1, IDARD2
	Continuous write to ID data carrier	IDAWD1, IDAWD2
	Data compare with ID data carrier	IDCMP1, IDCMP2
	Same data batch write to ID data carrier	IDFILL1, IDFILL2
	Copy between ID data carriers	IDCOPY1, IDCOPY2
	ID data carrier clear	IDCLR1, IDCLR2
	ID data carrier use end	IDOFF1, IDOFF2
	ID data carrier use start	IDON1, IDON2
AJ71QC24 control instruction*	Writes the user registration frame to the E ² PROM for the AJ71QC24N.	PUTE
	Reads the user registration frame from the E ² PROM for the AJ71QC24N.	GETE
	Data send with the dedicated protocol using the "on demand" function	ONDEMAND
	Data send for the specified number of bytes in no-protocol mode	OUTPUT
	Data send in accordance with the send schedule table in no-protocol mode	PRR
	Data receive in no-protocol mode	INPUT
	Data send with the bi-directional protocol	BIDOUT
	Data receive with the bi-directional protocol	BIDIN
	Communication status read	SPBUSY
	Device read from other stations	READ
	Device write to other stations	SWRITE
	Data send to other stations	SEND
	Data receive from other stations	RECV
	Transient transmission request to other stations	REQ

* The AJ71QC24N can be used with QnA link instructions designated for use with special function modules (G(P). ***).

(2) Instructions added after function version B

With function version B, the following instructions can be used in addition to the instructions in (1).

Refer to Section 2.2 for the function version.

Classification	Function	Instruction Symbol
AJ71ID□-R4 control instruction	Comparison read from ID data carrier	IDCRD1, IDCRD2
	Comparison write to ID data carrier	IDCWD1, IDCWD2
	Continuous comparison read from ID data carrier	IDSRD1, IDSRD2
	Continuous comparison write to ID data carrier	IDSWD1, IDSWD2
	Continuous high-speed read from ID data carrier	IDFRD1, IDFRD2
	Continuous high-speed write to ID data carrier	IDFWD1, IDFWD2
CC-Link control instruction	Read from the buffer memory of the intelligent device station	RIRD
	Write to the buffer memory of the intelligent device station	RIWT
	Write to the buffer memory of the intelligent device station(with handshake)	RISEND
	Read from the buffer memory of the intelligent device station (with handshake)	RIRCV
	Read from master station buffer memory for automatic update	RIFR
	Write to master station buffer memory for automatic update	RITO
	Intelligent device station communication	CCL, CCLEND
	Intelligent device station communication status read	SPCBUSY
	Intelligent device station communication processing interrupt	SPCCLR
	Remote register (RWr) read	RDGET
	Remote register (RWw) write	RDPUT
	Remote register (RWr) monitor	RDMON

Classification	Function		Instruction Symbol
AD75 control instruction	1 axis positioning start		PSTART
	Interpolation positioning start		PHOSTA
	OPR start		PZPR
	Current value change request		PADCH
	Forward JOG start/stop		PJOG+
	Reverse JOG start/stop		PJOG-
	Manual pulse generator operation enable/disable		PMPG
	Speed change request		PSPCH
	Axis error reset		PERRST
	Basic parameter setting		PBPSET
	Detail parameter setting		PEPSET
	OPR data setting		POPSET
	Positioning data setting		PPOSET
	Positioning start data setting		PSDSET
	Positioning special start data setting		PSPSET
	Condition data setting		PCTSET
	Error/warning number read		PEWR
	Monitor data read		PMDRD
	Positioning data I/F setting		PIFSET
AJ71QE71 control instruction	Parameter setting		EPRSET
	QnA compatible transmission/receiving instruction	Other station device read	READ SREAD
		Other station device write	WRITE SWRITE
		Data send	SEND
		Data receive	RECV
		Other station transient request	REQ
	A compatible send/receive instruction	Other station device read	ZNRD
		Other station device write	ZNWR

APPENDIX 2 Special Relay List

Special relays, SM, are internal relays whose applications are fixed in the PLC.

For this reason, they cannot be used by sequence programs in the same way as the normal internal relays.

However, they can be turned ON or OFF as needed in order to control the CPU module and remote I/O modules.

The heading descriptions in the following special relay lists are shown in Table App. 2.1.

Table App. 2.1. Explanation of special relay list

Item	Function of Item
Number	• Indicates special register number
Name	• Indicates name of special register
Meaning	• Indicates contents of special register
Explanation	• Discusses contents of special register in more detail
Set by (When set)	• Indicates whether the relay is set by the system or user, and, if it is set by the system, when setting is performed. <Set by> S : Set by system U : Set by user (sequence programs or test operations from GX Developer) S/U : Set by both system and user <When set> Indicated only for registers set by system Each END : Set during each END processing Initial : Set only during initial processing (when power supply is turned ON, or when going from STOP to RUN) Status change : Set only when there is a change in status Error : Set when error occurs Instruction execution : Set when instruction is executed Request : Set only when there is a user request (through SM, etc.) System switching : Set when system switching is executed.
Corresponding ACPU M9□□□	• Indicates the corresponding special relay (M9□□□) of the ACPUs. (When the contents are changed, the special relay is represented M9□□□ format change. Incompatible with the Q00J/Q00/Q01 and QnPRH.) • New indicates the special relay newly added to the QnACPU or Q series CPU module.
Corresponding CPU	Indicates the corresponding CPU module type name. ○ : Indicates all the QnACPU and QCPU. QCPU : Indicates all the Q series CPU modules. Q00J/Q00/Q01 : Indicates the Basic model QCPU. Qn(H) : Indicates the High Performance model QCPU. QnPH : Indicates the Process CPU. QnPRH : Indicates the Redundant CPU. QnU : Indicates the Universal model QCPU QnA : Indicates the QnA series and Q2ASCPU series. Rem : Indicates the MELSECNET/H remote I/O modules. Each CPU module model name: Indicates the relevant specific CPU module. (Example: Q4AR, Q3A)

For details on the following items, refer to the following manuals:

- Networks → Manual of the corresponding network module
- SFC → QCPU(Q mode)/QnACPU Programming Manual (SFC)

POINT

- (1)SD1200 to SD1255 are used for QnACPU.
These relays are vacant with QCPU.

(1) Diagnostic Information

Table App. 2.2. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM0	Diagnostic errors	OFF : No error ON : Error	• Turns ON if an error occurs as a result of diagnosis. (Includes when an annunciator is ON, and when an error is detected with CHK instruction) • Remains ON even if the condition is restored to normal thereafter.	S (Error)	New	QnA Qn(H) QnPH QnPRH Rem
			• Turns ON if an error occurs as a result of diagnosis. (Includes when an annunciator is ON) • Remains ON even if the condition is restored to normal thereafter.	S (Error)	New	Q00J/Q00/Q01 QnU
SM1	Self-diagnostic error	OFF : No self-diagnosis errors ON : Self-diagnosis	• Turns ON if an error occurs as a result of diagnosis. (Does not include when an annunciator is ON or when an error is detected by the CHK instruction) • Remains ON even if the condition is restored to normal thereafter.	S (Error)	M9008	QnA Qn(H) QnPH QnPRH Rem
			• Turns ON if an error occurs as a result of diagnosis. (Does not include when an annunciator is ON) • Remains ON even if the condition is restored to normal thereafter.	S (Error)	New	Q00J/Q00/Q01 QnU
SM5	Error common information	OFF : No error common information ON : Error common information	• When SM0 is ON, turns ON if there is error common information	S (Error)	New	○ Rem
SM16	Error individual information	OFF : No error individual information ON : Error individual information	• When SM0 is ON, turns ON if there is error individual information	S (Error)	New	
SM50	Error reset	OFF → ON: Error reset	• Conducts error reset operation	U	New	
SM51	Battery low latch	OFF : Normal ON : Battery low	• Turns ON if battery voltage at CPU module or memory card drops below rated value. • Remains ON even if the battery voltage returns to normal thereafter. • Synchronizes with the BAT. ALARM/BAT. LED.	S (Error)	M9007	QnA Qn(H) QnPH QnPRH QnU
			• Turns ON if battery voltage at CPU module or memory card drops below rated value. • Remains ON even if the battery voltage returns to normal thereafter. • Synchronous with BAT. LED	S (Error)	New	Q00J/Q00/Q01
SM52	Battery low	OFF : Normal ON : Battery low	• Same as SM51, but turns OFF subsequently when battery voltage returns to normal.	S (Error)	M9006	○ QCPU QnA
SM53	AC/DC DOWN detection	OFF : AC/DC DOWN not detected ON : AC/DC DOWN detected	• Turns ON if an instantaneous power failure of within 20ms occurs during use of the AC power supply module. Reset when the power supply is switched OFF, then ON.	S (Error)	M9005	
			• Turns ON if an instantaneous power failure of within 10ms occurs during use of the DC power supply module. Reset when the power supply is switched OFF, then ON.			
			• Turns ON if an instantaneous power failure of within 1ms occurs during use of the DC power supply module. Reset when the power supply is switched OFF, then ON.			
SM54	MINI link error	OFF : Normal ON : Error	• Turns ON if MINI (S3) link error is detected at even one of the installed AJ71PT32 (S3) modules. • Remains ON even if the condition is restored to normal thereafter.	S (Error)	M9004	

Table App. 2.2. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM56	Operation error	OFF : Normal ON : Operation error	- ON when operation error is generated - Remains ON if the condition is restored to normal thereafter.	S (Error)	M9011	○
SM60	Blown fuse detection	OFF : Normal ON : Module with blown fuse	- Turns ON if there is at least one output module whose fuse has blown. - Remains ON if the condition is restored to normal thereafter. - Blown fuse status is checked even for remote I/O station output modules.	S (Error)	M9000	○ Rem
SM61	I/O module verify error	OFF : Normal ON : Error	- Turns ON if the I/O module differs from the status registered at power on. - Remains ON if the condition is restored to normal thereafter. - I/O module verification is also conducted for remote I/O station modules.	S (Error)	M9002	
SM62	Annunciator detection	OFF : Not detected ON : Detected	Goes ON if even one annunciator F goes ON.	S (Instruction execution)	M9009	○
SM80	CHK detection	OFF : Not detected ON : Detected	- Goes ON if error is detected by CHK instruction. - Remains ON if the condition is restored to normal thereafter.	S (Instruction execution)	New	QnA Qn(H) QnPH QnPRH
SM90	Startup of monitoring timer for step transition (Enabled only when SFC program exists)	OFF : Not started (monitoring timer reset) ON : Started (monitoring timer started)	Corresponds to SD90	U	M9108	QnA Qn(H) QnPH QnPRH
SM91			Corresponds to SD91		M9109	
SM92			Corresponds to SD92		M9110	
SM93			Corresponds to SD93		M9111	
SM94			Corresponds to SD94		M9112	
SM95			Corresponds to SD95		M9113	
SM96			Corresponds to SD96		M9114	
SM97			Corresponds to SD97		New	
SM98			Corresponds to SD98		New	
SM99			Corresponds to SD99		New	
SM100	Serial communication function using flag	OFF : Serial communication function is not used. ON : Serial communication function is used.	Stores the setting of whether the serial communication function is used or not in the serial communication setting parameter	S (Power-ON or reset)	New	Q00J/Q00/Q01
SM101	Communication protocol status flag	OFF : GX Developer ON : MC protocol communication device	Stores whether the device that is communicating via the RS-232 interface is GX Developer or MC protocol communication device	S (RS232 communication)		
SM110	Protocol error	OFF : Normal ON : Abnormal	- Turns ON when an abnormal protocol was used to make communication in the serial communication function. - Remains ON if the condition is restored to normal thereafter	S (Error)		
SM111	Communication status	OFF : Normal ON : Abnormal	- Turns ON when the mode used to make communication was different from the setting in the serial communication function. - Remains ON if the condition is restored to normal thereafter.	S (Error)		
SM112	Error information clear	ON : Cleared	Turns ON when the error codes stored in SM110, SM111, SD110 and SD111 are cleared. (Activated when turned from OFF to ON)	U		
SM113	Overrun error	OFF : Normal ON : Abnormal	Turns ON when an overrun error occurred in the serial communication error.	S (Error)		
SM114	Parity error	OFF : Normal ON : Abnormal	Turns ON when a parity error occurred in the serial communication error.	S (Error)		
SM115	Framing error	OFF : Normal ON : Abnormal	Turns ON when a framing error occurred in the serial communication error.	S (Error)		

(2) System information

Table App. 2.3. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM202	LED OFF command	OFF → ON : LED OFF	When this relay goes from OFF to ON, the LEDs corresponding to the individual bits at SD202 go off	U	New	QnA Qn(H) QnPH QnPRH QnU
SM203	STOP contact	STOP status	Goes ON at STOP status	S (Status change)	M9042	○
SM204	PAUSE contact	PAUSE status	Goes ON at PAUSE status	S (Status change)	M9041	
SM205	STEP-RUN contact	STEP-RUN status	Goes ON at STEP-RUN status	S (Status change)	M9054	
SM206	PAUSE enable coil	OFF : PAUSE disabled ON : PAUSE enabled	PAUSE status is entered if this relay is ON when the PAUSE contact goes ON	U	M9040	○
	Device test request acceptance status	OFF : Device test not yet executed ON : Device test executed	Comes ON when the device test mode is executed on GX Developer.	S (Request)	New	Rem
SM210	Clock data set request	OFF : Ignored ON : Set request	When this relay goes from OFF to ON and after END instruction execution of subsequent scan, clock data stored in SD210 to SD213 are written to the CPU module.	U	M9025	○
SM211	Clock data error	OFF : No error ON : Error	ON when error is generated in clock data (SD210 to SD213) value, and OFF if no error is detected.	S (Request)	M9026	
SM212	Clock data display	OFF : Ignored ON : Display	Displays clock data as month, day, hour, minute, and second at the LED display at front of CPU module.(Enabled only for Q3ACPU and Q4ACPU)	U	M9027	Q3A Q4A Q4AR
SM213	Clock data read request	OFF : Ignored ON : Read request	When this relay is ON, clock data is read to SD210 to SD213 as BCD values.	U	M9028	○ Rem
SM220	CPU No.1 preparation completed	OFF : CPU No.1 preparation uncompleted ON : CPU No.1 preparation completed	Turned ON when access can be made to the CPU module No.1 from the other CPU module at power-on or reset operation. SM220 is used as interlock for accessing the CPU module No.1 when the multiple CPU synchronous setting is asynchronous.	S (When status changed)	New	QnU
SM221	CPU No.2 preparation completed	OFF : CPU No.2 preparation uncompleted ON : CPU No.2 preparation completed	Turned ON when access can be made to the CPU module No.2 from the other CPU module at power-on or reset operation. SM221 is used as interlock for accessing the CPU module No.2 when the multiple CPU synchronous setting is asynchronous.			
SM222	CPU No.3 preparation completed	OFF : CPU No.3 preparation uncompleted ON : CPU No.3 preparation completed	Turned ON when access can be made to the CPU module No.3 from the other CPU module at power-on or reset operation. SM222 is used as interlock for accessing the CPU module No.3 when the multiple CPU synchronous setting is asynchronous.			
SM223	CPU No.4 preparation completed	OFF : CPU No.4 preparation uncompleted ON : CPU No.4 preparation completed	Turned ON when access can be made to the CPU module No.4 from the other CPU module at power-on or reset operation. SM223 is used as interlock for accessing the CPU module No.4 when the multiple CPU synchronous setting is asynchronous.			QnU ^{*5}
SM235	Online module change flag	OFF : Online module change is not in progress ON : Online module change in progress	Turns on during online module change. (for host PLC)	S (During online module change)	New	QnPH
SM236	Online module change complete flag	OFF : Online module change incomplete ON : Online module change complete	- Turns ON for one scan after online module change is complete. - This contact point can only be used by the scan program. (for host PLC)	S (When online module change is complete)	New	

*5: The Universal model QCPU except the Q02UCPU.

Table App. 2.3. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM240	No. 1 CPU reset flag	OFF : No. 1 CPU reset cancel ON : No. 1 CPU resetting	- Goes OFF when reset of the No. 1 CPU is canceled. - Comes ON when the No. 1 CPU is resetting (including the case where the PLC is removed from the base). The other PLCs are also put in reset status.	S (Status change)	New	Q00/Q01*1 Qn(H)*1 QnPH QnU
SM241	No. 2 CPU reset flag	OFF : No. 2 CPU reset cancel ON : No. 2 CPU resetting	- Goes OFF when reset of the No. 2 CPU is canceled. - Comes ON when the No. 2 CPU is resetting (including the case where the PLC is removed from the base). The other PLCs result in "MULTI CPU DOWN" (error code: 7000).			
SM242	No. 3 CPU reset flag	OFF : No. 3 CPU reset cancel ON : No. 3 CPU resetting	- Goes OFF when reset of the No. 3 CPU is canceled. - Comes ON when the No. 3 CPU is resetting (including the case where the PLC is removed from the base). The other PLCs result in "MULTI CPU DOWN" (error code: 7000).			
SM243	No. 4 CPU reset flag	OFF : No. 4 CPU reset cancel ON : No. 4 CPU resetting	- Goes OFF when reset of the No. 4 CPU is canceled. - Comes ON when the No. 4 CPU is resetting (including the case where the PLC is removed from the base). The other PLCs result in "MULTI CPU DOWN" (error code: 7000).			Qn(H)*1 QnPH QnU*5
SM244	No. 1 CPU error flag	OFF : No. 1 CPU normal ON : No. 1 CPU during stop error	- Goes OFF when the No. 1 CPU is normal (including a continuation error). - Comes ON when the No. 1 CPU is during a stop error.			Q00/Q01*1 Qn(H)*1 QnPH QnU
SM245	No. 2 CPU error flag	OFF : No. 2 CPU normal ON : No. 2 CPU during stop error	- Goes OFF when the No. 2 CPU is normal (including a continuation error). - Comes ON when the No. 2 CPU is during a stop error.			
SM246	No. 3 CPU error flag	OFF : No. 3 CPU normal ON : No. 3 CPU during stop error	- Goes OFF when the No. 3 CPU is normal (including a continuation error). - Comes ON when the No. 3 CPU is during a stop error.			
SM247	No. 4 CPU error flag	OFF : No. 4 CPU normal ON : No. 4 CPU during stop error	- Goes OFF when the No. 4 CPU is normal (including a continuation error). - Comes ON when the No. 4 CPU is during a stop error.	S (Status change)	New	Qn(H)*1 QnPH QnU*5
SM250	Max. loaded I/O read	OFF : Ignored ON : Read	When this relay goes from OFF to ON, maximum loaded I/O number is read to SD250.	U	New	QnA Qn(H) QnPH QnPRH Rem
SM251	I/O change flag	OFF : No replacement ON : Replacement	- By turning this relay ON after setting the head I/O number of the replaced I/O module to SD251, the I/O module can be replaced online (with power on). (Only one module can be replaced for each setting.) - Turn this relay ON in the test mode of the program or peripheral device for an I/O module change during RUN, or in the test mode of the peripheral device for an I/O change during STOP. - Do not execute a RUN/STOP mode change until I/O module change is finished.	U	M9094	Q2A(S1) Q3A Q4A Q4AR
SM252	I/O change OK	OFF : Replacement prohibited ON : Replacement enabled	Goes ON when I/O replacement is OK.	S (END)	New	
SM254	All stations refresh command	OFF : Refresh arrival station ON : Refresh all stations	- Effective for the batch refresh (also effective for the low speed cyclic) - Designate whether to receive arrival stations only or to receive all slave stations in the MELSECNET/H.	U	New	Qn(H) QnPH QnPRH
			Designate whether to receive arrival stations only or to receive all slave stations in the MELSECNET/G.			Qn(H)*2
			- Effective for the batch refresh (also effective for the low speed cyclic) - Designate whether to receive arrival stations only or to receive all slave stations.			QnU

*1: This applies to the CPU of function version B or later.

*2: The module whose first 5 digits of serial No. is 09012 or later.

*5: The Universal model QCPU except the Q02UCPU.

Table App. 2.3. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM255	MELSECNET/10, MELSECNET/H module 1 information	OFF : Operative network ON : Standby network	• Goes ON for standby network (If no designation has been made concerning active or standby, active is assumed.)	S (Initial)	New	QnA Qn(H) QnPH QnPRH
SM256		OFF : Reads ON : Does not read	• For refresh from link to CPU module (B, W, etc.) indicate whether to read from the link module.	U	New	
SM257		OFF : Writes ON : Does not write	• For refresh from CPU module to link (B, W, etc.), designate whether to write to the link module.	U	New	
SM260	MELSECNET/10, MELSECNET/H module 2 information	OFF : Operative network ON : Standby network	• Goes ON for standby network (If no designation has been made concerning active or standby, active is assumed.)	S (Initial)	New	
SM261		OFF : Reads ON : Does not read	• For refresh from link to CPU module (B, W, etc.) indicate whether to read from the link module.	U	New	
SM262		OFF : Writes ON : Does not write	• For refresh from CPU module to link (B, W, etc.), designate whether to write to the link module.	U	New	
SM265	MELSECNET/10, MELSECNET/H module 3 information	OFF : Operative network ON : Standby network	• Goes ON for standby network (If no designation has been made concerning active or standby, active is assumed.)	S (Initial)	New	
SM266		OFF : Reads ON : Does not read	• For refresh from link to CPU module (B, W, etc.) indicate whether to read from the link module.	U	New	
SM267		OFF : Writes ON : Does not write	• For refresh from CPU module to link (B, W, etc.), designate whether to write to the link module.	U	New	
SM270	MELSECNET/10, MELSECNET/H module 4 information	OFF : Operative network ON : Standby network	• Goes ON for standby network (If no designation has been made concerning active or standby, active is assumed.)	S (Initial)	New	
SM271		OFF : Reads ON : Does not read	• For refresh from link to CPU module (B, W, etc.) indicate whether to read from the link module.	U	New	
SM272		OFF : Writes ON : Does not write	• For refresh from CPU module to link (B, W, etc.), designate whether to write to the link module.	U	New	
SM280	CC-Link error	OFF : Normal ON : Error	• Goes ON when a CC-Link error is detected in any of the installed CC-Link module. Goes OFF when normal operation is restored.	S (Status change)	New	Qn(H) QnPH QnPRH Rem
			• Goes ON when a CC-Link error is detected in any of the installed CC-Link module. Remains ON if the condition is restored to normal thereafter.	S (Error)	New	QnA
SM315	Communication reserved time delay enable/disable flag	OFF : Without delay ON : With delay	- This flag is enabled when the time reserved for communication processing is set in SD315. - Turns ON to delay the END processing by the time set in SD315 in order to perform communication processing. (The scan time increases by the period set in SD315.) - Turns OFF to perform the END processing without a delay of the time set in SD315 when there is no communication processing. (Defaults to OFF)	U	New	Q00J/Q00/Q01
SM320	Presence/absence of SFC program	OFF : SFC program absent ON : SFC program present	- Turns ON when an SFC program is registered. - OFF when an SFC program is not registered.	S (Initial)	M9100	QnA Q00J/Q00/Q01*1 Qn(H) QnPH QnPRH QnU
SM321	Start/stop SFC program	OFF : SFC program not executed (stop) ON : SFC program executed (start)	- Initial value is set at the same value as SM320. (Goes ON automatically if SFC program is present.) - Turn this relay from ON to OFF to stop program execution. - Turn this relay from OFF to ON to resume program execution.	S (Initial)/U	M9101form at change	

*1: This applies to the CPU of function version B or later.

Table App. 2.3. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM322	SFC program start status	OFF : Initial start ON : Resume start	- The SFC program starting mode in the SFC setting of the PLC parameter dialog box is set as the initial value. - AT initial start: OFF - At continued start: ON	S (Initial)/U	M9102form at change	QnA Q00J/Q00/Q01*1 Qn(H) QnPH QnPRH QnU
SM323	Presence/absence of continuous transition for entire block	OFF : Continuous transition not effective ON : Continuous transition effective	Set the presence/absence of continuous transition for the block where "Continuous transition bit" of the SFC data device has not been set.	U	M9103	
SM324	Continuous transition prevention flag	OFF : When transition is executed ON : When no transition	- OFF during operation in the continuous transition mode or during continuous transition, and ON when continuous transition is not executed. - Always ON during operation in the no continuous transition mode.	S (Instruction execution)	M9104	
				S (Status change)	New	
SM325	Output mode at block stop	OFF : OFF ON : Preserves	- Select whether the coil outputs of the active steps are held or not at the time of a block stop. - As the initial value, the output mode at a block stop in the parameter is OFF when the coil outputs are OFF, and ON when the coil outputs are held. - All coil outputs go OFF when this relay is OFF. - Coil outputs are preserved when this relay is ON.	S (Initial)/U	M9196	
SM326	SFC device clear mode	OFF : Clear device ON : Preserves device	Selects the device status when the stopped CPU is run after the sequence program or SFC program has been modified when the SFC program exists.	U	New	
SM327	Output during end step execution	OFF : Hold step output turned OFF (cleared) ON : Hold step output held	Select the device status at the time of switching from STOP to program write to RUN.(All devices except the step relay)	S (Initial)/U	New	QnA Qn(H) QnPH QnPRH QnU
				U		Q00J/Q00/Q01*1
SM328	Clear processing mode when end step is reached	OFF : Clear processing is performed. ON : Clear processing is not performed.	- Select whether clear processing will be performed or not if active steps other than the ones being held exist in the block when the end step is reached.? - When this relay turns OFF, all active steps are forcibly terminated to terminate the block. - When this relay is ON, the execution of the block is continued as-is. - If active steps other than the ones being held do not exist when the end step is reached, the steps being held are terminated to terminate the block.	U	New	Q00J/Q00/Q01*1 QnU
SM330	Operation mode for low speed execution type program	OFF : Asynchronous mode ON : Synchronous mode	- Select whether the low speed execution type program will be executed in the asynchronous mode or in the synchronous mode. - Asynchronous mode (this relay is turned OFF.) Mode in which the operation of the low speed execution type program is performed continuously within the excess time. - Synchronous mode (this relay is turned ON.) Mode in which the operation of the low speed execution type program is not performed continuously and operation is performed from the next scan if there is excess time.	U	New	QnA Qn(H) QnPH
SM331	Normal SFC program execution status	OFF : Not executed ON : Being executed	- Indicates whether the normal SFC program is being executed or not. - Used as an SFC control instruction execution interlock.	S (Status change)	New	Qn(H)*3 QnPH*4 QnPRH
SM332	Program execution management SFC program execution status	OFF : Not executed ON : Being executed	- Indicates whether the program execution management SFC program is being executed or not. - Used as an SFC control instruction execution interlock.			
SM390	Access execution flag	ON indicates completion of intelligent function module access	- The status of the intelligent function module access instruction executed immediately before is stored. (This data is overwritten when the intelligent function module access instruction is executed again.) - Used by the user in a program as a completion bit.	S (Status change)	New	Qn(H) QnPH QnPRH
SM391	GINT instruction execution completion flag	OFF : Not executed ON : Execution completed	- Indicates execution status of the S(P).GINT instruction. - Turned OFF before the instruction is executed. - Turned ON after the instruction is completed.	S (Instruction execution)	New	QnU

*1: This applies to the CPU of function version B or later.

*3: The module whose first 5 digits of serial No. is 04122 or later.

*4: The module whose first 5 digits of serial No. is 07032 or later.

(3) System clocks/counters

Table App. 2.4. Special relay

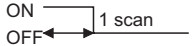
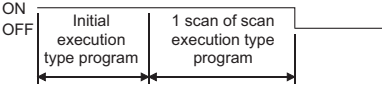
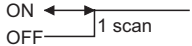
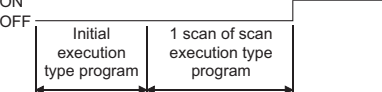
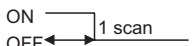
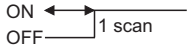
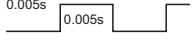
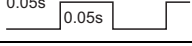
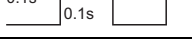
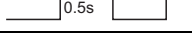
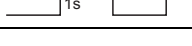
Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM400	Always ON	ON 	• Normally is ON	S (Every END processing)	M9036	○
SM401	Always OFF	OFF 	• Normally is OFF	S (Every END processing)	M9037	
SM402	After RUN, ON for 1 scan only	ON 	- After RUN, ON for 1 scan only. - This connection can be used for scan execution type programs only. - When an initial execution type program is used, this relay turns OFF at the END processing of the scan execution type program in the first scan after RUN. 	S (Every END processing)	M9038	QnA Qn(H) QnPH QnPRH QnU
			• After RUN, ON for 1 scan only.	S (Every END processing)	New	Q00J/Q00/Q01
SM403	After RUN, OFF for 1 scan only	OFF 	- After RUN, OFF for 1 scan only. - This connection can be used for scan execution type programs only. - When an initial execution type program is used, this relay turns OFF at the END processing of the scan execution type program in the first scan after RUN. 	S (Every END processing)	M9039	QnA Qn(H) QnPH QnPRH QnU
			• After RUN, OFF for 1 scan only.	S (Every END processing)	New	Q00J/Q00/Q01
SM404	Low speed execution type program ON for 1 scan only after RUN	ON 	- After RUN, ON for 1 scan only. - This connection can be used for low speed execution type programs only.	S (Every END processing)	New	QnA Qn(H) QnPH
SM405	Low speed execution type program After RUN, OFF for 1 scan only	OFF 	- After RUN, OFF for 1 scan only. - This connection can be used for low speed execution type programs only.	S (Every END processing)	New	
SM409	0.01 second clock		- Repeatedly changes between ON and OFF at 5-ms interval. - When PLC power supply is turned OFF or a CPU module reset is performed, goes from OFF to start. (Note that the ON-OFF status changes when the designated time has elapsed during the execution of the program.)	S (Status change)	New	Qn(H) QnPH QnPRH QnU
SM410	0.1 second clock		- Repeatedly changes between ON and OFF at each designated time interval. - When PLC power supply is turned OFF or a CPU module reset is performed, goes from OFF to start. (Note that the ON-OFF status changes when the designated time has elapsed during the execution of the program.)	S (Status change)	M9030	○
SM411	0.2 second clock				M9031	
SM412	1 second clock				M9032	
SM413	2 second clock				M9033	
SM414	2n second clock		- This relay alternates between ON and OFF at intervals of the time (unit: s) specified in SD414. - When PLC power supply is turned OFF or a CPU module reset is performed, goes from OFF to start. (Note that the ON-OFF status changes when the designated time has elapsed during the execution of the program.)	S (Status change)	M9034form at change	

Table App. 2.4. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM415	2n (ms) clock		- This relay alternates between ON and OFF at intervals of the time (unit: ms) specified in SD415. - When PLC power supply is turned OFF or a CPU module reset is performed, goes from OFF to start. (Note that the ON-OFF status changes when the designated time has elapsed during the execution of the program.)	S (Status change)	New	Qn(H) QnPH QnPRH QnU
SM420	User timing clock No.0	n1: ON scan interval n2: OFF scan interval	- Relay repeats ON/OFF switching at fixed scan intervals. - When PLC power supply is turned ON or a CPU module reset is performed, goes from OFF to start. (For the redundant CPU, however, this relay is always OFF after system switching.) - The ON/OFF intervals are set with the DUTY instruction	S (Every END processing)	M9020	○
SM421	User timing clock No.1				M9021	
SM422	User timing clock No.2				M9022	
SM423	User timing clock No.3				M9023	
SM424	User timing clock No.4				M9024	
SM430	User timing clock No.5		For use with SM420 to SM424 low speed programs	S (Every END processing)	New	QnA Qn(H) QnPH
SM431	User timing clock No.6					
SM432	User timing clock No.7					
SM433	User timing clock No.8					
SM434	User timing clock No.9					

(4) Scan information

Table App. 2.5. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM510	Low speed program execution flag	OFF : Completed or not executed ON : Execution under way.	Goes ON when low speed execution type program is executed.	S (Every END processing)	New	QnA Qn(H) QnPH
SM551	Reads module service interval	OFF : Ignored ON : Read	When this relay goes from OFF to ON, the module service interval designated by SD550 is read to SD551 to SD552.	U	New	QnA Qn(H) QnPH QnPRH Rem

(5) I/O refresh

Table App. 2.6. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM580	Program to program I/O refresh	OFF : Not refreshed ON : Refreshed	When this special relay is turned ON, I/O refresh is performed after execution of the first program, and the next program is then executed. When a sequence program and an SFC program are to be executed, the sequence program is executed, I/O refresh is performed, and the SFC program is then executed.	U	New	Q00J/Q00/Q01*1

*1: This applies to the CPU of function version B or later.

(6) Drive information

Table App. 2.7. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9 □ □ □	Corresponding CPU
SM600	Memory card (A) usable flags	OFF : Unusable ON : Use enabled	• ON when memory card (A) is ready for use by user	S (Status change)	New	QnA Qn(H) QnPH QnPRH QnU
SM601	Memory card (A) protect flag	OFF : No protect ON : Protect	• Goes ON when memory card (A) protect switch is ON	S (Status change)	New	
SM602	Drive 1 flag	OFF : No drive 1 ON : Drive 1 present	• Turns ON when the mounted memory card (A) is RAM	S (Status change)	New	
SM603	Drive 2 flag	OFF : No drive 2 ON : Drive 2 present	• Turns ON when the mounted memory card (A) is ROM	S (Status change)	New	
SM604	Memory card (A) in-use flag	OFF : Not used ON : In use	• Goes ON when memory card (A) is in use	S (Status change)	New	
SM605	Memory card (A) remove/insert prohibit flag	OFF : Remove/insert enabled ON : Remove/insert prohibited	• Goes ON when memory card (A) cannot be inserted or removed	U	New	
SM609	Memory card remove/insert enable flag	OFF : Remove/insert prohibited ON : Remove/insert enabled	• Turned ON by user to enable the removal/insertion of memory card. • Turned OFF by the system after the memory card is removed. • This contact can be used only when SM604 and SM605 are OFF.	S/U	New	Qn(H) QnPH QnPRH QnU
SM620	Drive 3/4 usable flags	OFF : Unusable ON : Use enabled	• Always ON	S (Initial)	New	QCPU
	Memory card B usable flags	OFF : Unusable ON : Use enabled	• ON when memory card B is ready for use by user	S (Initial)	New	Q2A(S1) Q3A Q4A Q4AR
SM621	Drive 3/4 protect flag	OFF : No protect ON : Protect	• Always OFF	S (Initial)	New	QCPU
	Memory card B protect flag	OFF : No protect ON : Protect	• Goes ON when memory card B protect switch is ON	S (Initial)	New	Q2A(S1) Q3A Q4A Q4AR
SM622	Drive 3 flag	OFF : No drive 3 ON : Drive 3 present	• Always ON	S (Initial)	New	QCPU
			• Goes ON when drive 3 (card 2 RAM area) is present	S (Initial)	New	Q2A(S1) Q3A Q4A Q4AR
SM623	Drive 4 flag	OFF : No drive 4 ON : Drive 4 present	• Always ON	S (Initial)	New	QCPU
			• Goes ON when drive 4 (card 2 ROM area) is present	S (Initial)	New	Q2A(S1) Q3A Q4A Q4AR
SM624	Memory card B in-use flag	OFF : Not used ON : In use	• Goes ON when the file within Drive 3 (standard RAM) or Drive 4 (standard ROM) is used.	S (Status change)	New	Q00J/Q00/Q01*1 Qn(H) QnPH QnPRH
			• Goes ON when memory card B is in use	S (Status change)	New	Q2A(S1) Q3A Q4A Q4AR
	Drive 3/4 in-use flag	OFF : Not used ON : In use	• Goes ON when the file within Drive 3 (standard RAM) or Drive 4 (standard ROM) is used.	S (Status change)	New	QnU
SM625	Memory card B remove/insert prohibit flag	OFF : Remove/insert enabled ON : Remove/insert prohibited	• Goes ON when memory card B cannot be inserted or removed	U	New	Q2A(S1) Q3A Q4A Q4AR
SM640	File register use	OFF : File register not used ON : File register in use	• Goes ON when file register is in use	S (Status change)	New	○

Table App. 2.7. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM650	Comment use	OFF : File register not used ON : File register in use	• Goes ON when comment file is in use	S (Status change)	New	QnA Qn(H) QnPH QnPRH QnU
SM660	Boot operation	OFF : Internal memory execution ON : Boot operation in progress	• Goes ON while boot operation is in process • Goes OFF if boot designation switch is OFF	S (Status change)	New	QnA Qn(H) QnPH QnPRH
		OFF : Program memory execution ON : Boot operation in progress	• Goes ON while boot operation is in process	S (Status change)	New	Q00J/Q00/Q01 QnU
SM671	Latch data backup to standard ROM completion flag	OFF : Not completed ON : Completed	• Turned ON when latch data backup to the standard ROM is completed. • Time when the latch data backup to the standard ROM was performed is stored in SD672 or later.	S (Status change)	New	QnU
SM672	Memory card A file register access range flag	OFF : Within access range ON : Outside access range	• Goes ON when access is made to area outside the range of file register R of memory card A.(Set within END processing.) • Reset at user program	S/U	New	QnA Qn(H) QnPH QnPRH
SM673	Memory card B file register access range flag	OFF : Within access range ON : Outside access range	• Goes ON when access is made outside the range of file registers, R. of memory card B.(Set within END processing.) • Reset at user program	S/U	New	Q2A(S1) Q3A Q4A Q4AR
SM675	Error completion of latch data backup to standard ROM	OFF : No Error ON : Error	• Turned ON when data cannot be backed up to the standard ROM by the latch data backup normally. • Turned OFF when data is backed up to the standard ROM by the latch data backup normally.	S	New	QnU
SM676	Specification of restore repeated execution	OFF : Not specified ON : Specified	• If latch data backup is performed when SM676 is ON, restore the data every time turning ON from OFF the power supply from the next power-on. • Delete the backed up latch data, or restore the data every time turning ON from OFF the power supply until the latch data backup operation will be executed again.	U	New	QnU
SM680	Program memory write error	OFF : Write error ON : Write not executed/normal	• Turns ON if a write error is detected at writing to program memory (flash ROM). Turns OFF by the write direction.	S (At write)	New	QnU
SM681	Program memory writing flag	OFF : During writing ON : Write not executed	• Turns ON when writing to the program memory (flash ROM) is in progress, and turns OFF when writing is completed.	S (At write)	New	QnU
SM682	Program memory overwrite count error flag	OFF : Overwrite count is 100,000 or more ON : Overwrite count is less than 100,000	• Turns ON when the overwrite count of program memory (flash ROM) reaches 100,000.	S (At write)	New	QnU
SM685	Standard ROM write error	OFF : Write error ON : Write not executed/normal	• Turns ON when write error is detected at writing to standard ROM (flash ROM). • Turns OFF by the write direction.	S (At write)	New	QnU
SM686	Standard ROM writing flag	OFF : During overwriting ON : Overwrite not executed	• Turns ON when writing to the standard ROM (flash ROM) is in progress, and turns OFF when writing is completed.	S (At write)	New	QnU
SM687	Standard ROM overwrite count error flag	OFF : Overwrite count is 100,000 or more ON : Overwrite count is less than 100,000	• Turns ON when the overwrite count of standard ROM (flash ROM) reaches 100,000. (It is necessary to change CPU module.)	S (At write)	New	QnU

(7) Instruction-Related Special Relays

Table App. 2.8. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM700	Carry flag	OFF : Carry OFF ON : Carry ON	• Carry flag used in application instruction	S (Instruction execution)	M9012	○
SM701	Number of output characters selection	Switching the number of output characters and the output pattern	• Used for the PR, PRC, BINDA, DBINDA, BINHA, DBINHA, BCDDA, DBCDDA, or COMRD instruction • For details, refer to the QCPU (Q Mode)/QnACPU Programming Manual (Common Instructions).	U	M9049	QnA Qn(H) QnPH QnPRH QnU
SM702	Search method	OFF : Search next ON : 2-part search	• Designates method to be used by search instruction. • Data must be arranged for 2-part search.	U	New	○
SM703	Sort order	OFF : Ascending order ON : Descending order	• The sort instruction is used to designate whether data should be sorted in ascending order or in descending order.	U	New	
SM704	Block comparison	OFF : Non-match found ON : All match	• Goes ON when all data conditions have been met for the BKCMP instruction.	S (Instruction execution)	New	
SM707	Selection of real number instruction processing type	OFF : Speed oriented ON : Accuracy oriented	• When SM707 is OFF, real number instructions are processed at high speed. • When it is ON, real number instructions are processed with high accuracy.	U	New	Q4AR
SM710	CHK instruction priority ranking flag	OFF : Conditions priority ON : Pattern priority	• Remains as originally set when OFF. • CHK priorities updated when ON.	S (Instruction execution)	New	QnA Qn(H) QnPH QnPRH
SM711	Divided transmission status	OFF : Other than during divided processing ON : During divided processing	• In processing of AD57(S1), goes ON when screen is split for transfer, and goes OFF when split processing is completed	S (Instruction execution)	M9065	QnA
SM712	Transmission processing selection	OFF : Batch processing ON : Divided processing	• In processing of AD57(S1), goes ON when canvas screen is divided for transfer.	S (Instruction execution)	M9066	
SM714	Communication request registration area BUSY signal	OFF : Communication request to remote terminal module enabled ON : Communication request to remote terminal module disabled	• Used to determine whether communications requests to remote terminal modules connected to the AJ71PT32-S3 can be executed or not.	S (Instruction execution)	M9081	
SM715	EI flag	OFF : During DI ON : During EI	• ON when EI instruction is being executed.	S (Instruction execution)	New	○
SM720	Comment read completion flag	OFF : Comment read not completed	• Turns on only during one scan when the processing of the COMRD or PRC instruction is completed.	S (Status change)	New	Qn(H) QnPH
		ON : Comment read completed	• Turns on only during one scan when the processing of the COMRD instruction is completed.			QnPRH QnU
SM721	File being accessed	OFF : File not accessed ON : File being accessed	• Switches ON while a file is being accessed by the S. FWRITE, S. FREAD, COMRD, PRC, or LEDC instruction.	S (Status change)	New	Qn(H) QnPH
			• Switches ON while a file is being accessed by the S. FWRITE, S. FREAD, COMRD or LEDC instruction.			Qn(H) QnPH QnPRH
			• Switches ON while a file is being accessed by the S. FWRITE, S. FREAD, COMRD or SP.DEVST instruction.			QnU
SM722	BIN/DBIN instruction error disabling flag	OFF : Error detection performed ON : Error detection not performed	• Turned ON when "OPERATION ERROR" is suppressed for BIN or DBIN instruction.	U	New	QCPU
SM730	BUSY signal for CC-Link communication request registration area	OFF : Request for communication with intelligent device station enabled ON : Request for communication with intelligent device station disabled	• Used for determination whether to enable or disable the communication request for the intelligent device station connected with CC-Link module.	S (Instruction execution)	New	QnA
SM734	XCALL instruction execution condition designation	OFF : Not executed by execution condition risen ON : Executed by execution condition risen	• During OFF, XCALL instructions will not be executed even if execution condition is risen. • During ON, XCALL instructions will be executed when execution condition is risen.	U	New	Qn(H)*1

*1: The module whose first 5 digits of serial No. is 06082 or later.

Table App. 2.8. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM735	SFC comment readout instruction in execution flag	OFF : SFC comment readout instruction is inactivated. ON : SFC comment readout instruction is activating.	• Turns on the instructions, (S(P).SFCSOMR) to read the SFC step comments and (S(P).SFCTCOMR) to read the SFC transition condition comments.	S (status change)	New	Qn(H) ^{*2} QnPH ^{*3} QnPRH ^{*3}
SM736	PKEY instruction execution in progress flag	OFF : Instruction not executed ON : Instruction execution	• ON when PKEY instruction is being executed. Goes OFF when CR is input, or when input character string reaches 32 characters.	S (Instruction execution)	New	QnA
SM737	Keyboard input reception flag for PKEY instruction	OFF : Keyboard input reception enabled ON : Keyboard input reception disabled	• Goes ON when keyboard input is being conducted. Goes when keyboard input has been stored at the CPU.	S (Instruction execution)	New	
SM738	MSG instruction reception flag	OFF : Instruction not executed ON : Instruction execution	• Goes ON when MSG instruction is executed	S (Instruction execution)	New	Qn(H) QnPRH
SM774	PID bumpless processing (for complete derivative)	OFF : Matched ON : Not matched	• Specifies whether to match the set value (SV) with the process value (PV) or not in the manual mode.	U	New	QnA Q00J/Q00/Q01 ^{*4} Qn(H) QnPRH QnU
SM775	Selection of refresh processing during COM instruction execution	OFF : Performs link refresh ON : Performs no link refresh	• Select whether link refresh processing will be performed or not when only communication with the CPU module is made at the execution of the COM instruction.	U	New	QnA Q00J/Q00/Q01 Qn(H) QnPH
		OFF : Performs all refresh processes ON : Performs refresh set by SD778	• Select whether to perform all refreshes or the refresh processing set by SD778 when the COM instruction is executed.	U	New	Q00J/Q00/Q01 ^{*4} Qn(H) ^{*5} QnPH ^{*3} QnPRH QnU
SM776	Enable/disable local device at CALL	OFF : Local device disabled ON : Local device enabled	• Set whether the local device of the subroutine program called at execution of the CALL instruction is valid or invalid.	U	New	QnA Qn(H) QnPH QnPRH QnU
SM777	Enable/disable local device in interrupt program	OFF : Local device disabled ON : Local device enabled	• Set whether the local device at execution of the interrupt program is valid or invalid.	U	New	
SM780	CC-Link dedicated instruction executable	OFF : CC-Link dedicated instruction executable ON : CC-Link dedicated instruction not executable	• Switches ON when the number of the CC-Link dedicated instructions that can be executed simultaneously reaches 32. Switches OFF when the number goes below 32.	U	New	QnA
SM794	PID bumpless processing(for incomplete derivative)	OFF : Matched ON : Not matched	• Specifies whether to match the set value (SV) with the process value (PV) or not in the manual mode.	U	New	Q00J/Q00/Q01 ^{*4} Qn(H) ^{*6} QnPRH QnU

*1: The module whose first 5 digits of serial No. is 06082 or later.

*2: The module whose first 5 digits of serial No. is 07012 or later.

*3: The module whose first 5 digits of serial No. is 07032 or later.

*4: This applies to the CPU module of function version B or later.

*5: The module whose first 5 digits of serial No. is 04012 or later.

*6: The module whose first 5 digits of serial No. is 05032 or later.

Table App. 2.8. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9 □ □ □	Corresponding CPU
SM796	Block information using dedicated instruction of Multiple CPU high speed bus (for CPU No.1)	OFF : Block is secured ON : Block set by SD796 cannot be secured	- Turns ON when the number of the remaining blocks of the dedicated instruction transmission area used for the dedicated instruction of Multiple CPU high speed bus (target CPU= CPU No.1) is less than the number of blocks specified by SD796. - Turns ON at instruction execution. Turns OFF when the empty area exists at END processing.	S (When instruction/END processing executed)	New	QnU*7
SM797	Block information using dedicated instruction of Multiple CPU high speed bus (for CPU No.2)	OFF : Block is secured ON : Block set by SD797 cannot be secured	- Turns ON when the number of the remaining blocks of the dedicated instruction transmission area used for the dedicated instruction of Multiple CPU high speed bus (target CPU= CPU No.2) is less than the number of blocks specified by SD797. - Turns ON at instruction execution. Turns OFF when the empty area exists at END processing.	S (When instruction/END processing executed)	New	QnU*7
SM798	Block information using dedicated instruction of Multiple CPU high speed bus (for CPU No.3)	OFF : Block is secured ON : Block set by SD798 cannot be secured	- Turns ON when the number of the remaining blocks of the dedicated instruction transmission area used for the dedicated instruction of Multiple CPU high speed bus (target CPU= CPU No.3) is less than the number of blocks specified by SD798. - Turns ON at instruction execution. Turns OFF when the empty area exists at END processing.	S (When instruction/END processing executed)	New	QnU*7
SM799	Block information using dedicated instruction of Multiple CPU high speed bus (for CPU No.4)	OFF : Block is secured ON : Block set by SD799 cannot be secured	- Turns ON when the number of the remaining blocks of the dedicated instruction transmission area used for the dedicated instruction of Multiple CPU high speed bus (target CPU= CPU No.4) is less than the number of blocks specified by SD799. - Turns ON at instruction execution. Turns OFF when the empty area exists at END processing.	S (When instruction/END processing executed)	New	QnU*7

*7: The Universal model QCPU except the Q02UCPU.

(8) Debug

Table App. 2.9. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9 □ □ □	Corresponding CPU
SM800	Trace preparation	OFF : Not ready ON : Ready	• Switches ON when the trace preparation is completed	S (Status change)	New	Qn(H) QnPH QnPRH QnU
	Sampling trace preparation		• Goes ON when sampling trace is ready	S (Status change)	New	QnA
SM801	Trace start	OFF : Suspend ON : Start	• Trace is started when this relay switches ON. • Trace is suspended when this relay switches OFF. (All related special Ms switches OFF.)	U	M9047	Qn(H) QnPH QnPRH QnU
	Sampling trace start		• Sampling trace started when this goes ON • Suspended when OFF (Related special M all OFF)	U	M9047	QnA
SM802	Trace execution in progress	OFF : Suspend ON : Start	• Switches ON during execution of trace.	S (Status change)	M9046	Qn(H) QnPH QnPRH QnU
	Sampling trace execution in progress		• Goes ON during execution of sampling trace	S (Status change)	M9046	QnA
SM803	Trace trigger	OFF → ON: Start	• Trace is triggered when this relay switches from OFF to ON. (Identical to TRACE instruction execution status)	U	M9044	Qn(H) QnPH QnPRH QnU
	Sampling trace trigger		• Sampling trace trigger goes ON when this goes from OFF to ON (Identical to STRA instruction execution status)	U	M9044	QnA
SM804	After trace trigger	OFF : Not after trigger ON : After trigger	• Switches ON after trace is triggered.	S (Status change)	New	Qn(H) QnPH QnPRH QnU
	After sampling trace trigger		• Goes ON after sampling trace trigger	S (Status change)	New	QnA
SM805	Trace completed	OFF : Not completed ON : End	• Switches ON at completion of trace	S (Status change)	M9043	Qn(H) QnPH QnPRH QnU
	Sampling trace completed		• Goes ON at completion of sampling trace	S (Status change)	M9043	QnA
SM806	Status latch preparation	OFF : Not ready ON : Ready	• Goes ON when status latch is ready	S (Status change)	New	
SM807	Status latch command	OFF → ON: Latch	• Runs status latch command	U	New	
SM808	Status latch completion	OFF : Latch not completed ON : Latch completed	• Comes ON when status latch is completed.	S (Status change)	M9055	
SM809	Status latch clear	OFF → ON: Clear	• Enable next status latch	U	New	
SM810	Program trace preparation	OFF : Not ready ON : Ready	• Goes ON when program trace is ready	S (Status change)	New	
SM811	Start program trace	OFF : Suspend ON : Start	• Program trace started when this goes ON • Suspended when OFF (Related special M all OFF)	S (Status change)	New	
SM812	Program trace execution under way	OFF : Suspend ON : Start	• ON when program trace execution is underway	U	New	
SM813	Program trace trigger	OFF → ON: Start	• Program trace trigger goes ON when this goes from OFF to ON (Identical to PTRS instruction execution status)	S (Status change)	New	
SM814	After program trace trigger	OFF : Not after trigger ON : After trigger	• Goes ON after program trace trigger	S (Status change)	New	
SM815	Program trace completion	OFF : Not completed ON : End	• Goes ON at completion of program trace	S (Status change)	New	

Table App. 2.9. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM820	Step trace preparation	OFF : Not ready ON : Ready	• Goes ON after program trace registration, at ready	S (Status change)	New	QnA
SM821	Step trace starts	OFF : Suspend ON : Start	• Select whether execution of step trace is started or suspended. • When this goes ON, step trace is started • Suspended when OFF (Related special M all OFF)	U	M9182form at change	
SM822	Step trace execution underway	OFF : Suspend ON : Start	• Goes ON when step trace execution is underway • Goes OFF at completion or suspension	S (Status change)	M9181	
SM823	After step trace trigger	OFF : Not after trigger ON : Is after first trigger	• Goes ON if even 1 block within the step trace being executed is triggered. • Goes OFF when step trace is commenced.	S (Status change)	New	
SM824	After Step trace trigger	OFF : Is not after all triggers ON : Is after all triggers	• Goes ON if all blocks within the step trace being executed are triggered. • Goes OFF when step trace is commenced.	S (Status change)	New	
SM825	Step trace completed	OFF : Not completed ON : End	• Goes ON at step trace completion. • Goes OFF when step trace is commenced.	S (Status change)	M9180	
SM826	Trace error	OFF : Normal ON : Errors	• Switches ON if error occurs during execution of trace	S (Status change)	New	Qn(H) QnPH QnPRH QnU
	Sampling trace error		• Goes ON if error occurs during execution of sampling trace.	S (Status change)	New	QnA
SM827	Status latch error	OFF : Normal ON : Errors	• Goes ON if error occurs during execution of status latch.	S (Status change)	New	
SM828	Program trace error	OFF : Normal ON : Errors	• Goes ON if error occurs during execution of program trace.	S (Status change)	New	
SM829	Forced registration specification of trace setting	ON : Forced registration enabled OFF : Forced registration disabled	• Even when the trace condition or the trigger condition is established, the sampling trace setting can be set to the QnUCPU by turning SM829 ON and registering the sampling trace setting by GX Developer.	U	New	QnU

(9) Latch area

Table App. 2.10. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM900	Power off file	OFF : No power off file ON : Power off file present	• Goes ON if a file is present during access when power is interrupted.	S (Status change)/ U	New	QnA
SM910	RKEY registration flag	OFF : Keyboard input notregistered ON : Keyboard input registered	• Goes ON at registration of keyboard input. • OFF if keyboard input is not registered.	S (Instruction execution)	New	

(10)A to Q/QnA conversion correspondences

Special relays SM1000 to SM1255 are the relays which correspond to ACPU special relays M9000 to M9255 after A to Q/QnA conversion.

(However, the Basic model QCPU, Redundant CPU, and Universal model QCPU do not support the A to Q/QnA conversion.)

These special relays are all set by the system, and cannot be set by the user program.

To turn them ON/OFF by the user program, change the special relays in the program into those of QCPU/QnACPU.

However, some of SM1084 and SM1200 to SM1255 (corresponding to M9084 and M9200 to M9255 before conversion) can be turned ON/OFF by the user program, if they could be turned ON/OFF by the user program before conversion. For details on the ACPU special relays, see the user's manuals for the individual CPUs, and MELSECNET or MELSECNET/B Data Link System Reference Manuals

POINT	
	The processing time may be longer when converted special relays are used with the High Performance model QCPU and Process CPU. Uncheck "Compatibility with A-PLC" within the PC system setting in GX Developer parameters when converted special relays are not used.

The following are additional explanations about the Special Relay for Modification column.

- ① When a special relay for modification is provided, the device number should be changed to the provided QCPU/QnACPU special relay.
- ② When ☐ is provided, the converted special relay can be used for the device number.
- ③ When ☒ is provided, the device number does not work with QCPU/QnACPU.

Table App. 2.11. Special relay

ACPU Special Relay	Special Relay after Conversion	Special Relay for Modification	Name	Meaning	Details	Corresponding CPU
M9000	SM1000	—	Fuse blown	OFF : Normal ON : Module with blown fuse	- Turned on when there is one or more output modules of which fuse has been blown. - Remains ON if the condition is restored to normal thereafter. - Output modules of remote I/O stations are also checked for fuse condition.	QnA Qn(H) QnPH
M9002	SM1002	—	I/O module verify error	OFF : Normal ON : Error	- Turned on if the status of I/O module is different from entered status when power is turned on. - Remains ON if the condition is restored to normal thereafter. - I/O module verification is done also to remote I/O station modules. - Reset is enabled only when special registers SD1116 to SD1123 are reset.	
M9004	SM1004	—	NIM link master module error	OFF : Normal ON : Error	- Goes ON if MINI (S3) link error is detected at even one of the installed AJ71PT32 (S3) modules. - Remains ON if the condition is restored to normal thereafter.	QnA

Table App. 2.11. Special relay

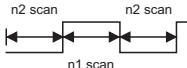
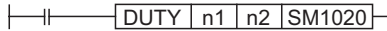
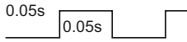
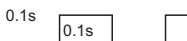
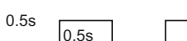
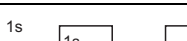
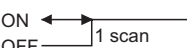
ACPU Special Relay	Special Relay after Conversion	Special Relay for Modification	Name	Meaning	Details	Corresponding CPU	
M9005	SM1005	—	AC DOWN detection	OFF : AC DOWN not detected ON : AC DOWN detected	• Turns ON if an instantaneous power failure of within 20ms occurs during use of the AC power supply module. • Reset when the power supply is switched OFF, then ON.	QnA Qn(H) QnPH	
					• Turns ON if an instantaneous power failure of within 10ms occurs during use of the DC power supply module. • Reset when the power supply is switched OFF, then ON.	Qn(H) QnPH	
					• Turns ON if an instantaneous power failure of within 1ms occurs during use of the DC power supply module. • Reset when the power supply is switched OFF, then ON.	QnA	
M9006	SM1006	—	Battery low	OFF : Normal ON : Battery low	• Turns ON when the battery voltage drops to or below the specified. • Turns OFF when the battery voltage returns to normal thereafter.	QnA Qn(H) QnPH	
M9007	SM1007	—	Battery low latch	OFF : Normal ON : Battery low	• Turns ON when the battery voltage drops to or below the specified. • Remains ON if the battery voltage returns to normal thereafter.		
M9008	SM1008	SM1	Self-diagnosis error	OFF : No error ON : Error	• Turned on when error is found as a result of self-diagnosis.		
M9009	SM1009	SM62	Annunciator detection	OFF : No F number detected ON : F number detected	• Turned on when OUT F of SET F instruction is executed. • Switched off when SD1124 data is cleared to zero.		
M9011	SM1011	SM56	Operation error flag	OFF : No error ON : Error	• Turned on when operation error occurs during execution of application instruction. • Remains ON if the condition is restored to normal thereafter.		
M9012	SM1012	SM700	Carry flag	OFF : Carry OFF ON : Carry ON	• Carry flag used in application instruction.		
M9016	SM1016	×	Data memory clear flag	OFF : Ignored ON : Output claired	• Clears the data memory including the latch range (other than special relays and special registers) in remote run mode from computer, etc. when SM1016 is on.		
M9017	SM1017	×	Data memory clear flag	OFF : Ignored ON : Output claired	• Clears the unlatched data memory (other than special relays and special egisters) in remote run mode from computer, etc. when SM1017 is on.		
M9020	SM1020	—	User timing clock No.0		• Relay which repeats on/off at intervals of predetermined scan. • When power is turned on or reset is per-formed, the clock starts with off. Set the intervals of on/off by DUTY instruction. 		
M9021	SM1021	—	User timing clock No.1				
M9022	SM1022	—	User timing clock No.2				
M9023	SM1023	—	User timing clock No.3				
M9024	SM1024	—	User timing clock No.4				
M9025	SM1025	—	Clock data set request	OFF : Ignored ON : Set request present used	• Writes the clock data stored in SD1025 to SD1028 to the CPU module after the END instruction is executed in the scan in which SM1025 turned from OFF to ON.	Q3A Q4A Q4AR	
M9026	SM1026	—	Clock data error	OFF : No error ON : Error	• Switched on by clock data (SD1025 to SD1028) error		
M9027	SM1027	—	Clock data display	OFF : Ignored ON : Display	• Clock data is read from SD1025 to SD1028 and month, day, hour, minute and minute are indicated on the CPU module front LED display.	QnA Qn(H) QnPH	
M9028	SM1028	—	Clock data read request	OFF : Ignored ON : Read request	• Reads clock data to SD1025 to SD1028 in BCD when SD1028 is on.		
M9029	SM1029	×	Batch processing of data communications requests	OFF : Batch processing not conducted ON : Batch processing conducted	• The SM1029 relay is turned on using a sequence program to process all data communication requests accepted during one scan in the END processing of that scan. • The batch processing of the data communication requests can be turned on and off during running. • The default is OFF (processed one at a time for each END processing in the order in which data communication requests are accepted).		
M9030	SM1030	—	0.1 second clock		• 0.1 second, 0.2 second, 1 second and 2 second, clocks are generated. • Not turned on or off per scan but turned on and off even during scan if corresponding time has elapsed. • Starts with off when PLC power supply is turned on or CPU module reset is performed.		
M9031	SM1031	—	0.2 second clock				
M9032	SM1032	—	1 second clock				
M9033	SM1033	—	2 second clock				

Table App. 2.11. Special relay

ACPU Special Relay	Special Relay after Conversion	Special Relay for Modification	Name	Meaning	Details	Corresponding CPU
M9034	SM1034	—	2n minute clock(1 minute clock)*		• Alternates between ON and OFF according to the seconds specified at SD414. (Default: n = 30) • Not turned on or off per scan but turned on and off even during scan if corresponding time has elapsed. • Starts with off when PLC power supply is turned on or CPU module reset is performed..	QnA Qn(H) QnPH
M9036	SM1036	—	Always ON	ON  OFF	• Used as dummy contacts of initialization and application instruction in sequence program. • SM1038 and SM1037 are turned on and off without regard to position of key switch on CPU module front. SM1038 and SM1039 are under the same condition as RUN status except when the key switch is at STOP position, and turned off and on. Switched off if the key switch is in STOP position. SM1038 is on for one scan only and SM1039 is off for one scan only if the key switch is not in STOP position.	
M9037	SM1037	—	Always OFF	ON  OFF		
M9038	SM1038	—	ON for 1 scan only after RUN	ON  OFF		
M9039	SM1039	—	RUN flag(After RUN, OFF for 1 scan only)	ON  OFF		
M9040	SM1040	SM206	PAUSE enable coil	OFF : PAUSE disabled ON : PAUSE enabled	• When RUN key switch is at PAUSE position or pause contact has turned on and if SM204 is on, PAUSE mode is set and SM206 is turned on.	
M9041	SM1041	SM204	PAUSE status contact	OFF : PAUSE not in effect ON : PAUSE in effect		
M9042	SM1042	SM203	STOP status contact	OFF : STOP not in effect ON : STOP in effect	• Switched on when the RUN key switch or RUN/STOP switch is in STOP position.	
M9043	SM1043	SM805	Sampling trace completed	OFF : Sampling trace in progress ON : Sampling trace completed	• Turned on upon completion of sampling trace performed the number of times preset by parameter after [STRA] instruction is executed. - Reset when [STRAR] instruction is executed.	
M9044	SM1044	SM803	Sampling trace	OFF → ON [STRA] Same as execution ON → OFF [STRAR] Same as execution	• Turning on/off SM803 can execute [STRA] / [STRAR] instruction. (SM803 is forcibly turned on/off by a peripheral device.) - When switched from OFF to ON: [STRA] instruction - When switched from ON to OFF: [STRAR] instruction - The value stored in SD1044 is used as the condition for the sampling trace. - At scanning, at time → Time (10 ms unit)	
M9045	SM1045	×	Watchdog timer (WDT) reset	OFF : Does not reset WDT ON : Resets WDT	• The SM1015 relay is turned on to reset the WDT when the ZCOM instruction and data communication request batch processing are executed (used when the scan time exceeds 200 ms).	
M9046	SM1046	SM802	Sampling trace	OFF : Trace not in progress ON : Trace in progress	• Switched on during sampling trace.	
M9047	SM1047	SM801	Sampling trace preparations	OFF : Sampling trace suspended ON : Sampling trace started	• Sampling trace is not executed unless SM801 is turned ON. - Sampling trace is suspended when SM801 goes OFF.	
M9049	SM1049	SM701	Switching the number of output characters	OFF : Output until NULL code encountered ON : 16 characters output	• When SM701 is OFF, characters up to NULL (00H) code are output. • When SM701 is ON, ASCII codes of 16 characters are output.	
M9051	SM1051	×	CHG instruction execution disable	OFF : Enabled ON : Disable	• Switched ON to disable the CHG instruction. • Switched ON when program transfer is requested. - Automatically switched OFF when transfer is complete.	
M9052	SM1052	×	SEG instruction switch	OFF : 7SEG segment display ON : I/O partial refresh	• When SM1052 is ON, the SEG instruction is executed as an I/O partial refresh instruction. - When SM1052 is OFF, the SEG instruction is executed as a 7-SEG display instruction.	
M9054	SM1054	SM205	STEP RUN flag	OFF : STEP RUN not in effect ON : STEP RUN in effect	• Switched on when the RUN key switch is in STEP RUN position.	QnA
M9055	SM1055	SM808	Status latch completion flag	OFF : Not completed ON : Completed	• Turned on when status latch is completed. • Turned off by reset instruction.	

*: 1 minute clock indicates the name of the special relay (M9034) of the ACPU.

Table App. 2.11. Special relay

ACPU Special Relay	Special Relay after Conversion	Special Relay for Modification	Name	Meaning	Details	Corresponding CPU
M9056	SM1056	×	Main side P, I set request	OFF : Other than when P, I set being requested ON : P, I set being requested	• Provides P, I set request after transfer of the other program (for example subprogram when main program is being run) is complete during run. Automatically switched off when P, I setting is complete.	QnA Qn(H) QnPH
M9057	SM1057	×	Sub side P, I set request	OFF : Other than when P, I set being requested ON : P, I set being requested		
M9058	SM1058	×	Main side P, I set completion	Momentarily ON at P, I set completion	• Turned ON once when the P, I set has been completed, and then turned OFF again.	
M9059	SM1059	×	Sub program P, I set completion	Momentarily ON at P, I set completion		
M9060	SM1060	×	Sub program 2 P, I set request	OFF : Other than when P, I set being requested ON : P, I set being requested	• Provides P, I set request after transfer of the other program (for example subprogram when main program is being run) is complete during run. Automatically switched off when P, I setting is complete.	
M9061	SM1061	×	Sub program 3 P, I set request	OFF : Other than when P, I set being requested ON : P, I set being requested		
M9065	SM1065	SM711	Divided transfer status	OFF : Divided processing not underway ON : During divided processing	• Turned on when canvas screen transfer to AD57(S1)/AD58 is done by divided processing, and turned off at completion of divided processing	QnA
M9066	SM1066	SM712	Transfer processing switch	OFF : Batch transfer ON : Divided transfer	• Turned on when canvas screen transfer to AD57(S1)/AD58 is done by divided processing.	
M9070	SM1070	×	A8UPU/ A8PUJrequired search time*	OFF : Read time not shortened ON : Read time shortened	• Turned ON to shorten the search time in the A8UPU/A8PUJ. (In this case, the scan time is extended by 10 %.)	QnA Qn(H) QnPH
M9081	SM1081	SM714	Communication request registration area BUSY signal	OFF : Empty spaces in communication request registration area ON : No empty spaces in communication request registration area	• Indication of communication enable/disable to remote terminal modules connected to the AJ71PT32-S3, A2C or A52G.	QnA
M9084	SM1084	×	Error check	OFF : Error check executed ON : No error check	It is set whether the error checks below are performed or not when the END instruction is processed (to set the END instruction processing time). • Check for fuse blown. • Check of battery • Collation check of I/O module	QnA Qn(H) QnPH
M9091	SM1091	×	Operation error details flag	OFF : No error ON : Error	• Turns ON when the detail factor of the operation error is stored into SD1091. • Remains ON if the condition is restored to normal thereafter.	
M9094	SM1094	SM251	I/O exchange flag	OFF : Exchanged ON : Not exchanged	• The I/O module can be changed online (with power on) when SM251 is turned ON after the head I/O number of the I/O module is set to SD251. (One module only is allowed to be changed by one setting.) • To be switched on in the program or peripheral device test mode to change the module during CPU RUN. To be switched on in peripheral device test mode to change the module during CPU STOP. • RUN/STOP mode must not be changed until I/O module change is complete.	QnA
M9100	SM1100	SM320	Presence/absence of SFC program	OFF : SFC programs not used ON : SFC programs used	• Turned on if the SFC program is registered. • Turned off if the SFC program is not registered.	QnA Qn(H) QnPH
M9101	SM1101	SM321	Start/stop SFC program	OFF : SFC programs stop ON : SFC programs start	• The value in SM320 is set as the initial value. (The relay automatically turns ON when the SFC program is present.) • When this relay turns from ON to OFF, execution of the SFC program stops. • When this relay turns from OFF to ON, execution of the SFC program resumes.	
M9102	SM1102	SM322	SFC program start status	OFF : Initial start ON : Resume start	• The SFC program start mode in the SFC setting of the PLC parameter dialog box is set as the initial value. At initial start: OFF At continue start: ON	

*: The A8UPU/A8PUJ is not available for the QCPU/QnACPU.

Table App. 2.11. Special relay

ACPU Special Relay	Special Relay after Conversion	Special Relay for Modification	Name	Meaning			Details	Corresponding CPU
M9103	SM1103	SM323	Presence/absence of continuous transition	OFF : Continuous transition not effective ON : Continuous transition effective			• Set whether continuous transition will be performed for the block where the "continuous transition bit" of the SFC information device is not set.	QnA Qn(H) QnPH
M9104	SM1104	SM324	Continuous transition suspension flag	OFF : When transition is completed ON : When no transition			• OFF during operation in the continuous transition mode or during continuous transition, and ON when continuous transition is not executed. • Always ON during operation in the no continuous transition mode.	
M9108	SM1108	SM90	Step transition monitoring timer start (equivalent of SD90)	OFF : Monitoring timer reset ON : Monitoring timer reset start			• Turns ON when the measurement of the step transition monitoring timer is started. Turning this relay OFF resets the step transition monitoring timer.	
M9109	SM1109	SM91	Step transition monitoring timer start (equivalent of SD91)					
M9110	SM1110	SM92	Step transition monitoring timer start (equivalent of SD92)					
M9111	SM1111	SM93	Step transition monitoring timer start (equivalent of SD93)					
M9112	SM1112	SM94	Step transition monitoring timer start (equivalent of SD94)					
M9113	SM1113	SM95	Step transition monitoring timer start (equivalent of SD95)					
M9114	SM1114	SM96	Step transition monitoring timer start (equivalent of SD96)					
M9180	SM1180	SM825	Active step sampling trace completion flag	OFF : Trace started ON : Trace completed			• Set when sampling trace of all specified blocks is completed. Reset when sampling trace is started.	QnA
M9181	SM1181	SM822	Active step sampling trace execution flag	OFF : Trace not being executed ON : Trace execution under way			• Set when sampling trace is being executed.Reset when sampling trace is completed or suspended	
M9182	SM1182	SM821	Active step sampling trace permission	OFF : Trace disable/suspend ON : Trace enable			• Selects sampling trace execution enable/disable. ON: Sampling trace execution is enabled. OFF: Sampling trace execution is disabled. If turned off during sampling trace execution, trace is suspended.	
M9196	SM1196	SM325	Operation output at block stop	OFF : Coil output OFF ON : Coil output ON			• Selects the operation output when block stop is executed. ON: Retains the ON/OFF status of the coil being used by using operation output of the step being executed at block stop. OFF: All coil outputs are turned off. (Operation output by the SET instruction is retained regardless of the ON/OFF status of M9196.)	QnA Qn(H) QnPH
M9197	SM1197	×	Switch between blown fuse and I/O verify error display	SM 1197	SM 1198	I/O numbers to be displayed	Switches I/O numbers in the fuse blow module storage registers (SD1100 to SD1107) and I/O module verify error storage registers (SD1116 to SD1123) according to the combination of ON/OFF of the SM1197 and SM1198.	
				OFF	OFF	X/Y0 to 7F0		
				ON	OFF	X/Y800 to FF0		
M9198	SM1198	×		OFF	ON	X/Y1000 to 17F0		
			ON	ON	X/Y1800 to 1FF0			
M9199	SM1199	×	Data recovery of online sampling trace/status latch	OFF : Data recovery disabled ON : Data recovery enabled			• Recovers the setting data stored in the CPU module at restart when sampling trace/status latch is executed. • SM1199 should be ON to execute again. (Unnecessary when writing the data again from peripheral devices.)	

Table App. 2.11. Special relay

ACPU Special Relay	Special Relay after Conversion	Special Relay for Modification	Name	Meaning	Details	Corresponding CPU
M9200	SM1200	—	ZNRD instruction (LRDP instruction for ACPU) reception (for master station)	OFF : Not accepted ON : Accepted	- Depends on whether or not the ZNRD (word device read) instruction has been received. - Used in the program as an interlock for the ZNRD instruction. - Use the RST instruction to reset.	QnA
M9201	SM1201	—	ZNRD instruction (LRDP instruction for ACPU) completion (for master station)	OFF : Not completed ON : End	- Depends on whether or not the ZNRD (word device read) instruction execution is complete. - Used as a condition contact for resetting M9200 and M9201 after the ZNRD instruction is complete. - Use the RST instruction to reset.	
M9202	SM1202	—	ZNWR instruction (LWTP instruction for ACPU) reception (for master station)	OFF : Not accepted ON : Accepted	- Depends on whether or not the ZNWR (word device write) instruction has been received. - Used in the program as an interlock for the ZNWR instruction. - Use the RST instruction to reset.	
M9203	SM1203	—	ZNWR instruction (LWTP instruction for ACPU) completion (for master station)	OFF : Not completed ON : End	- Depends on whether or not the ZNWR (word device write) instruction execution is complete. - Used as a condition contact to reset M9202 and M9203 after the ZNWR instruction is complete. - Use the RST instruction to reset.	
M9204	SM1204	—	ZNRD instruction (LRDP instruction for ACPU) reception (for local station)	OFF : Not completed ON : End	On indicates that the ZNRD instruction is complete at the local station.	
M9205	SM1205	—	ZNWR instruction (LWTP instruction for ACPU) reception (for local station)	OFF : Not completed ON : End	On indicates that the ZNWR instruction is complete at the local station.	
M9206	SM1206	—	Host station link parameter error	OFF : Normal ON : Abnormal	Depends on whether or not the link parameter setting of the host is valid.	
M9207	SM1207	—	Link parameter check results	OFF : Match ON : Mismatch	Depends on whether or not the link parameter setting of the master station in tier two matches that of the master station in tier three in a three-tier system. (Valid for only the master station in a three-tier system.)	
M9208	SM1208	—	Sets master station B and W transmission range (for lower link master stations only)	OFF : Transmits to tier2 and tier 3 ON : Transmits to tier2 only	Depends on whether or not the B and W data controlled by higher-link master station (host station) is sent to lower-link local stations (tertiary stations). When SM1208 is OFFB and W of host station is sent to tertiary stations. When SM1208 is ONB and W of host station is not sent to tertiary stations.	
M9209	SM1209	—	Link parameter check command (for lower link master stations only)	OFF : Executing the check function ON : Check non-execution	- Set to ON not to match B and W of the higher and lower links. - When SM1209 is ON, the link parameters of the higher and lower link are not checked. - When SM1209 is OFF, the link parameters of the higher and lower link are checked.	
M9210	SM1210	—	Link card error (for master station)	OFF : Normal ON : Abnormal	Control is performed depending on whether the link card hardware is faulty or not.	
M9211	SM1211	—	Link module error (for local station use)	OFF : Normal ON : Abnormal	Control is performed depending on whether the link card hardware is faulty or not.	
M9224	SM1224	—	Link status	OFF : Online ON : Offline, station-to-station test, or self-loopback test	Depends on whether the master station is online or offline or is in station-to-station test or self-loopback test mode.	
M9225	SM1225	—	Forward loop error	OFF : Normal ON : Abnormal	Depends on the error condition of the forward loop line.	
M9226	SM1226	—	Reverse loop error	OFF : Normal ON : Abnormal	Depends on the error condition of the reverse loop line.	
M9227	SM1227	—	Loop test status	OFF : Not being executed ON : Forward or reverse loop test execution underway	Depends on whether or not the master station is executing a forward or a reverse loop test.	
M9232	SM1232	—	Local station operation status	OFF : RUN or STEP RUN status ON : STOP or PAUSE status	Control is performed depending on whether a local station is in the STOP or PAUSE mode.	
M9233	SM1233	—	Local station error detect status	OFF : No errors ON : Error detection	Depends on whether or not a local station has detected an error in another station.	

Table App. 2.11. Special relay

ACPU Special Relay	Special Relay after Conversion	Special Relay for Modification	Name	Meaning	Details	Corresponding CPU
M9235	SM1235	—	Local station, remote I/O station parameter error detect status	OFF : No errors ON : Error detection	Depends on whether or not a local or a remote I/O station has detected any link parameter error in the master station	QnA
M9236	SM1236	—	Local station, remote I/O station initial communications status	OFF : No communications ON : Communications underway	Depends on the results of initial communication between a local or remote I/O station and the master station. (Parameter communication, etc.)	
M9237	SM1237	—	Local station, remote I/O station error	OFF : Normal ON : Abnormal	Depends on the error condition of a local or remote I/O station.	
M9238	SM1238	—	Local station, remote I/O station forward or reverse loop error	OFF : Normal ON : Abnormal	Depends on the error condition of the forward and reverse loop lines of a local or a remote I/O station.	
M9240	SM1240	—	Link status	OFF : Online ON : Offline, station-to- station test, or self- loopback test	Depends on whether the local station is online or offline, or is in station-to-station test or self-loopback test mode.	
M9241	SM1241	—	Forward loop line error	OFF : Normal ON : Abnormal	Depends on the error condition of the forward loop line.	
M9242	SM1242	—	Reverse loop line error	OFF : Normal ON : Abnormal	Depends on the error condition of the reverse loop line.	
M9243	SM1243	—	Loopback implementation	OFF : Loopback not being conducted ON : Loopback implementation	Depends on whether or not loopback is occurring at the local station.	
M9246	SM1246	—	Data not received	OFF : Reception ON : No reception	Depends on whether or not data has been received from the master station.	
M9247	SM1247	—	Data not received	OFF : Reception ON : No reception	Depends on whether or not a tier three station has received data from its master station in a three-tier system.	
M9250	SM1250	—	Parameters not received	OFF : Reception ON : No reception	Depends on whether or not link parameters have been received from the master station.	
M9251	SM1251	—	Link relay	OFF : Normal ON : Abnormal	Depends on the data link condition at the local station.	
M9252	SM1252	—	Loop test status	OFF : Not being executed ON : Forward or reverse loop test execution underway	Depends on whether or not the local station is executing a forward or a reverse loop test.	
M9253	SM1253	—	Master station operation status	OFF : RUN or STEP RUN status ON : STOP or PAUSE status	Control is performed depending on whether the master station is in the STOP or PAUSE mode.	
M9254	SM1254	—	Local station other than host station operation status	OFF : RUN or STEP RUN status ON : STOP or PAUSE status	Control is performed depending on whether a local station other than the host is in the STOP or PAUSE mode.	
M9255	SM1255	—	Local station other than host station error	OFF : Normal ON : Abnormal	Depends on whether or not a local station other than the host is in error.	

(11) Process control instructions

Table App. 2.12. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9 □ □ □	Corresponding CPU
SM1500	Hold mode	OFF : No-hold ON : Hold	• Specifies whether or not to hold the output value when a range over occurs for the S.IN instruction range check.	U	New	Q4AR QnPH QnPRH
SM1501	Hold mode	OFF : No-hold ON : Hold	• Specifies whether or not the output value is held when a range over occurs for the S.OUT instruction range check.	U	New	

(12) For redundant systems (Host system CPU information *1)

SM1510 to SM1599 are only valid for redundant systems.

All off for standalone systems.

Table App. 2.13. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9 □ □ □	Corresponding CPU
SM1510	Operation mode	OFF : Redundant system backup mode, stand- alone system ON : Redundant system separate mode	• Turns on when the operating mode is redundant system separate.	S (Each END)	New	Q4AR QnPRH
SM1511	Start mode when power supply is on	OFF : System A fixed mode ON : Previous control system latch mode	• Turns on when the start mode for a redundant system when the power is turned on is the previous control system latch mode.	S (Initial)	New	Q4AR
SM1512	Start mode when CPU is started	OFF : Initial start ON : Hot start	• Turns on when the CPU module operation mode is hot start when the redundant system is started up.	S (Initial)	New	
SM1511	System A identification flag	• Distinguishes between system A and system B. • The flag status does not change even if the tracking cable is disconnected.		S (Initial)	New	QnPRH
SM1512	System B identification flag		When TRK. CABLE ERR. (error code: 6210) occurs (Unknown)			
		SM1511	ON	OFF	OFF	
		SM1512	OFF	ON	OFF	
SM1513	Operation status when CPU is started	OFF : Initial start ON : Hot start	• Turns on when the CPU module operation mode is hot start when the redundant system is actually start up.	S (Initial)	New	Q4AR
	Debug mode status flag	OFF : Not in debug mode ON : Debug mode	• Turns on when the redundant system operating mode is set to debug mode.	S (Initial)	New	QnPRH
SM1514	Operation mode at CPU module change	OFF : Initial start ON : Hot start	• Turns on when the operation is hot start when the CPU module operation is switched for a redundant system.	S (Initial)	New	Q4AR
SM1515	Output hold mode	OFF : Output reset ON : Output hold	• Turns on when the output mode during a stop error is output hold.	S (Each END)	New	
SM1516	Operation system status	OFF : Control system ON : Standby system	• Turns on when the CPU module operation system status is the standby system.	S (Status change)	New	
SM1515	Control system judgment flag	• Indicates operation system status. • The flag status does not change even if the tracking cable is disconnected.		S (Status change)	New	QnPRH
SM1516	Standby system judgment flag		When TRK. CABLE ERR. (error code: 6210) occurs (Unknown)			
		SM1515	ON	OFF	OFF	
		SM1516	OFF	ON	OFF	

*1: The information of the host CPU module is stored.

Table App. 2.13. Special relay

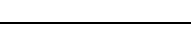
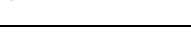
Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU	
SM1517	CPU module startup status	OFF : Power supply on startup ON : Operation system switch start up	- Turns on when the CPU module is started up by the operation system switch. - Reset using the user program.	S (Status change)/ U	New	Q4AR	
			Turns on when the CPU module is started up by the system switching (switching from the standby system to the control system). Remains OFF when the standby system is switched to the control system by a power-ON startup.	S (Status change)	New	QnPRH	
SM1518	Tracking execution mode	OFF : Batch transfer mode ON : Carryover mode	- When this relay is turned OFF, the start of tracking is delayed until it is executable if the tracking memory is being used at END. - When this relay is turned ON, the start of tracking is carried over to next END if the tracking memory is being used at END.	U	New	Q4AR	
	Standby system to control system switching status flag	ON  OFF 	- Turns ON once switch between standby system to control system, (ON for 1 scan only) occurs. - This status flag can only be used for scan execution type programs.	S (Each END)	New	QnPRH	
SM1519	Previous Control System Identification Flag	ON  OFF 	On the last operation Control System was System B, if power supply is supplied, or reset is released on both SYSTEM together, After RUN, ON for 1 scan only by System A side.	S (Each END)	New		
SM1520	Data tracking transfer trigger specification	OFF : No trigger ON : Trigger	SM1520 Block 1	<In the case of Q4AR> - When data is transferred by the data tracking instruction S. TRUCK, the target block is specified as trigger. <In the case of QnPRH> - When data is transferred based on the tracking setting of the redundant parameter dialog box, the target block is specified as trigger. - When "Auto Tracking block No.1" is enabled in the tracking setting, SM1520 is turned ON by the system at power ON/ STOP to RUN. In other cases, SM1520 to SM1583 are turned ON by the user.	<In the case of Q4AR> U <In the case of QnPRH> S (initial)/U	New	Q4AR QnPRH
SM1521			SM1521 Block 2				
SM1522			SM1522 Block 3				
SM1523			SM1523 Block 4				
SM1524			SM1524 Block 5				
SM1525			SM1525 Block 6				
SM1526			SM1526 Block 7				
SM1527			SM1527 Block 8				
SM1528			SM1528 Block 9				
SM1529			SM1529 Block 10				
SM1530			SM1530 Block 11				
SM1531			SM1531 Block 12				
SM1532			SM1532 Block 13				
SM1533			SM1533 Block 14				
SM1534			SM1534 Block 15				
SM1535			SM1535 Block 16				
SM1536			SM1536 Block 17				
SM1537			SM1537 Block 18				
SM1538			SM1538 Block 19				
SM1539			SM1539 Block 20				
SM1540			SM1540 Block 21				
SM1541			SM1541 Block 22				
SM1542			SM1542 Block 23				
SM1543			SM1543 Block 24				
SM1544			SM1544 Block 25				
SM1545			SM1545 Block 26				
SM1546			SM1546 Block 27				
SM1547			SM1547 Block 28				
SM1548			SM1548 Block 29				

Table App. 2.13. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9 □ □ □	Corresponding CPU
SM1549	Data tracking transmission link specification	OFF : No trigger ON : Trigger	SM1549 Block 30	<In the case of Q4AR> U <In the case of QnPRH> S (initial)/U	New	Q4AR QnPRH
SM1550			SM1550 Block 31			
SM1551			SM1551 Block 32			
SM1552			SM1552 Block 33			
SM1553			SM1553 Block 34			
SM1554			SM1554 Block 35			
SM1555			SM1555 Block 36			
SM1556			SM1556 Block 37			
SM1557			SM1557 Block 38			
SM1558			SM1558 Block 39			
SM1559			SM1559 Block 40			
SM1560			SM1560 Block 41			
SM1561			SM1561 Block 42			
SM1562			SM1562 Block 43			
SM1563			SM1563 Block 44			
SM1564			SM1564 Block 45			
SM1565			SM1565 Block 46			
SM1566			SM1566 Block 47			
SM1567			SM1567 Block 48			
SM1568			SM1568 Block 49			
SM1569			SM1569 Block 50			
SM1570			SM1570 Block 51			
SM1571			SM1571 Block 52			
SM1572			SM1572 Block 53			
SM1573			SM1573 Block 54			
SM1574			SM1574 Block 55			
SM1575			SM1575 Block 56			
SM1576			SM1576 Block 57			
SM1577			SM1577 Block 58			
SM1578			SM1578 Block 59			
SM1579			SM1579 Block 60			
SM1580			SM1580 Block 61			
SM1581			SM1581 Block 62			
SM1582			SM1582 Block 63			
SM1583			SM1583 Block 64			
SM1590	Switching status from the network module	OFF : Normal ON : Switching unsuccessful	• Turns ON when switching could not be executed normally if the network module had detected a network fault and issued a switching request to the host CPU module.	S (Error occurs)	New	Q4AR
	System switching enable/disable flag from network module	OFF : System switching request issuing module absent ON : System switching request issuing module present	• Turns ON when a system switching request is issued from the network module. The module No. that issued system switching can be checked by SD1590. • Turns OFF when all bits of SD1590 are OFF.	S (Each END)		QnPRH
SM1591	Standby system error detection disable flag at system switching	ON : Error is not detected by new standby system at system switching ON : Error is detected by new standby system at system switching	This flag is used to determine if the new standby station detects 6210:STANDBY during system switching. This applies to the following switching methods: • System switching from GX Developer • System switching using dedicated instruction • System switching by the intelligent function module	U	New	
SM1592	Enable/disable user system switching	OFF : Disable user system switching ON : Enable user system switching	• This flag enables system switching by the user from GX Developer or by dedicated instruction. (SP.CONTSW).	U	New	

Table App. 2.13. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM1593	Setting to access extension base unit of standby system CPU	OFF : Error ON : Ignored	Sets the operation for the case accessing buffer memory of the intelligent function module mounted on the extension base unit from the standby system CPU in separate mode. OFF : "OPERATION ERROR" (error code: 4112) will be returned when accessing buffer memory of the intelligent function module on the extension base unit from the standby system CPU. ON : No processing is performed when accessing buffer memory of intelligent function module on the extension base unit from the standby system CPU.	U	New	QnPRH ^{*2}
SM1595	Memory copy to other system start flag	OFF : Start memory copy ON : No memory copy initiated	• When SM1595 is turned from OFF to ON, memory copy from control system to standby system starts. Note that when SM1595 is turned from OFF to ON, memory copy does not start if the I/O No. of the copy destination (standby system CPU module: 3D1H) is not stored in SD1595.			QnPRH
SM1596	Memory copy to other system status flag	OFF : Memory copy not executed ON : Memory copy executed	• Turns on while memory is copied to other system. • Turns off when memory copy execution has completed.	S (Starting to copy/finish)		
SM1597	Memory copy to other system completion flag	OFF : Memory copy not completed ON : Memory copy completed	• Turns on once the memory copying to the other system has completed.	S (finish)/U	New	QnPRH
SM1598	Copy contents of standard ROM during memory copy	OFF : Copy standard ROM data ON : Standard ROM data is not copied	• If set to on by user, the standard ROM data is not copied to the other system while memory copy is executing.	U		

*2: The module whose first 5 digits of serial No. is 09012 or later.

(13)For redundant system (Other system CPU information *1)

SM1600 to SM1650 only valid for the CPU redundant system backup mode, so they cannot be refreshed during the separate mode.

Either the backup mode or the separate mode is valid for the SM4651 to SM1699.

SM1600 to SM1699 are all turned off for stand-alone system.

Table App. 2.14. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding Host SM□□ *2	Corresponding CPU
SM1600	Diagnosis error	OFF : No error ON : Error	• Turns on if a error occurs in the diagnosis results. (Including external diagnosis) • Remains on even if returns to normal thereafter.	S (Each END)	SM0	Q4AR
	Other system error flag	OFF : No error ON : Error	• Turns on when an error occurs during redundant system. Error check (Turns on single bit of SD1600.) • Is off when no errors are present	S (Each END)	—	QnPRH
SM1601	Self diagnosis error	OFF : No self diagnosis error ON : Self diagnosis error	• Turns on when an error occurs in the self-diagnosis results. • Remains on even if returns to normal thereafter.	S (Each END)	SM1	Q4AR
SM1605	Error common information	OFF : No error common information ON : Error common information	• Turns on when there is error common information and the SM1600 is on.	S (Each END)	SM5	

*1 Stores other system CPU diagnostic information and system information.

*2 This shows the special relay(SM□□) for the host system CPU.

Table App. 2.14. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corresponding Host SM□□ *2	Corresponding CPU
SM1610	Other system diagnostics error	OFF : No error ON : Error	- Turns on when a diagnostics error occurs. (Includes error detection when annunciator is ON, and by CHK instruction) - Corresponds to status of SM0 at other system	S (Each END)	SM0	QnPRH
SM1611	Other systems self diagnostics error.	OFF : No self diagnostics error occurred ON : Self diagnostics error occurred	- Turns on when a self diagnostics error occurs. (Does not include error detection when annunciator is ON, and by CHK instruction) - Corresponds to status of SM1 at other system	S (Each END)	SM1	
SM1615	Other system common error information	OFF : No common error information present ON : Common error information present	- Turns on when there is common error information at other system - Corresponds to status of SM5 at other system	S (Each END)	SM5	
SM1616	Error individual information	OFF : No error individual information ON : Error individual information	Turns on when there is error individual information and the SM1600 is on.	S (Each END)	SM16	Q4AR
SM1626	Error individual information for other systems	OFF : No individual error information present ON : Individual error information present	- Turns on when there is individual error information at other system - Corresponds to status of SM16 at other system	S (Each END)	SM16	QnPRH
SM1649	Standby system cancel error flag	OFF to ON: Cancels error of standby system	By turning this relay from OFF to ON, the continue error that occurred in the standby system CPU module can be canceled. Use SD1649 to specify the error code of the error to be canceled.	U	—	
SM1653	STOP contact	STOP status	Turns on when in the STOP status.	S (Each END)	SM203	Q4AR
SM1654	PAUSE contact	PAUSE status	Turns on when in the PAUSE status.	S (Each END)	SM204	
SM1655	STEP-RUN contact	STEP-RUN status	Turns on when in the STEP-RUN status.	S (Each END)	SM205	

*2 This shows the special relay(SM□□) for the host system CPU.

(14)For redundant system (tracking)

Either the backup mode or the separate mode is valid for SM1700 to SM1799.

All is turned off for stand-alone system.

Table App. 2.15. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9 □ □ □	Corresponding CPU
SM1700	Tracking execution flag	OFF : Execution not possible ON : Execution possible	• Turns on when tracking can be normally executed.	S (status change)	New	Q4AR
	Transfer trigger completion flag	OFF : Transfer not completed ON : Transfer completed	• Turns on for one scan, once transfer of block 1 to block 64 is completed.	S (status change)	New	QnPRH
SM1709	Manual system switching disable/enable setting during online program change redundant tracking	ON : Manual system switching enabled (Disable canceled) OFF : Manual system switching disabled	(1) Turning this relay from OFF to ON enables manual system switching during online program change redundant tracking. After the manual system switching disable status is canceled, the system automatically turns off SM1709. (2) System switching due to any of the following conditions is executed even during online program change redundant tracking, regardless of the status of this relay. •Power off, reset, hardware failure, CPU stop error (3) In either of the following statuses, the system switching disable status can also be canceled by this relay. •Multiple-block online program change redundant tracking execution status •File batch online program change redundant tracking execution status	S (When executed)/U		
SM1710	Transfer tracking data during online program change enable flag	OFF : No device tracking ON : Transfer device memory	(1) Set whether the tracking of the following data will be executed or not during online program change redundant tracking. •Device memory (Including SM/SD that will automatically execute tracking) •PIDINIT information, S.PIDINIT information, SFC information (2) SM1710 can be also used to set whether tracking will be executed or not while online change of multiple program blocks or batch of files is being performed to ensure consistency of both systems. (3) This SM is also transferred from control system CPU module to standby system CPU module by tracking data.	U		

Table App. 2.15. Special relay

Number	Name	Meaning	Explanation		Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM1712	Transfer trigger completion flag	OFF : Transfer uncompleted ON : Transfer completed	SM1712	Block 1	S (status change)	New	Q4AR QnPRH
SM1713			SM1713	Block 2			
SM1714			SM1714	Block 3			
SM1715			SM1715	Block 4			
SM1716			SM1716	Block 5			
SM1717			SM1717	Block 6			
SM1718			SM1718	Block 7			
SM1719			SM1719	Block 8			
SM1720			SM1720	Block 9			
SM1721			SM1721	Block 10			
SM1722			SM1722	Block 11			
SM1723			SM1723	Block 12			
SM1724			SM1724	Block 13			
SM1725			SM1725	Block 14			
SM1726			SM1726	Block 15			
SM1727			SM1727	Block 16			
SM1728			SM1728	Block 17			
SM1729			SM1729	Block 18			
SM1730			SM1730	Block 19			
SM1731			SM1731	Block 20			
SM1732			SM1732	Block 21			
SM1733			SM1733	Block 22			
SM1734			SM1734	Block 23			
SM1735			SM1735	Block 24			
SM1736			SM1736	Block 25			
SM1737			SM1737	Block 26			
SM1738			SM1738	Block 27			
SM1739			SM1739	Block 28			
SM1740			SM1740	Block 29			
SM1741			SM1741	Block 30			
SM1742			SM1742	Block 31			
SM1743			SM1743	Block 32			
SM1744			SM1744	Block 33			
SM1745			SM1745	Block 34			
SM1746			SM1746	Block 35			
SM1747			SM1747	Block 36			
SM1748			SM1748	Block 37			
SM1749			SM1749	Block 38			
SM1750			SM1750	Block 39			
SM1751			SM1751	Block 40			
SM1752			SM1752	Block 41			
SM1753			SM1753	Block 42			
SM1754			SM1754	Block 43			
SM1755			SM1755	Block 44			
SM1756			SM1756	Block 45			
SM1757			SM1757	Block 46			
SM1758			SM1758	Block 47			
SM1759			SM1759	Block 48			

Table App. 2.15. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM1760	Transmission trigger end flag	OFF : Transmission uncompleted ON : Transmission end	SM1760 Block 49	S (status change)	New	Q4AR QnPRH
SM1761			SM1761 Block 50			
SM1762			SM1762 Block 51			
SM1763			SM1763 Block 52			
SM1764			SM1764 Block 53			
SM1765			SM1765 Block 54			
SM1766			SM1766 Block 55			
SM1767			SM1767 Block 56			
SM1768			SM1768 Block 57			
SM1769			SM1769 Block 58			
SM1770			SM1770 Block 59			
SM1771			SM1771 Block 60			
SM1772			SM1772 Block 61			
SM1773			SM1773 Block 62			
SM1774			SM1774 Block 63			
SM1775			SM1775 Block 64			

(15) Redundant power supply module information

Table App. 2.16. Special relay

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU M9□□□	Corresponding CPU
SM1780	Power supply off detection flag	OFF : No redundant power supply module with input power OFF detected ON : Redundant power supply module with input power OFF detected	• Turns ON when one or more redundant power supply modules with input power OFF are detected. • Turns on if any of SD1780 bits is on. • Turns off if all bits of SD1780 are off. • Turns OFF when the main base unit is not the redundant main base unit (Q38RB). 0: communication with peripheral device is executed 1: communication with peripheral device is nonexecuted	S (Each END)	New	Qn(H)*2 QnPH*2 QnPRH Rem
SM1781	Power supply failure detection flag	OFF : No faulty redundant power supply module detected ON : Faulty redundant power supply module detected	• Turns ON when one or more faulty redundant power supply modules are detected. • Turns on if any of SD1781 bits is on. • Turns off if all bits of SD1781 are off. • Turns OFF when the main base unit is not the redundant main base unit (Q38RB). 0: communication with peripheral device is executed 1: communication with peripheral device is nonexecuted	S (Each END)		
SM1782	Momentary power failure detection flag for power supply 1 *1	OFF : No momentary power failure detected ON : Momentary power failure detected	• Turns ON when a momentary power failure of the input power supply to the power supply 1 or 2 is detected one or more times. After turning ON, remains ON even if the power supply recovers from the momentary power failure. • Turns OFF the flag (SM1782, SM1783) of the power supply 1/2 when the CPU module starts. • When the input power to one of the redundant power supply modules turns OFF the corresponding flag turns OFF. • Turns OFF when the main base unit is not the redundant main base unit (Q38RB). 0: communication with peripheral device is executed 1: communication with peripheral device is nonexecuted	S (Each END)		
SM1783	Momentary power failure detection flag for power supply 2 *1					

*1: The "power supply 1" indicates the redundant power supply module (Q64RP) mounted on the POWER 1 slot of the redundant base unit (Q38RB/Q68RB/Q65WRB).

The "power supply 2" indicates the redundant power supply module (Q64RP) mounted on the POWER 2 slot of the redundant base unit (Q38RB/Q68RB/Q65WRB).

*2: The module whose first 5 digits of serial No. is 04012 or later.

However, for the multiple CPU system configuration, this applies to all CPU modules whose first 5 digits of serial No. are 07032 or later.

APPENDIX 3 Special Register List

The special registers, SD, are internal registers with fixed applications in the PLC.

For this reason, it is not possible to use these registers in sequence programs in the same way that normal registers are used.

However, data can be written as needed in order to control the CPU modules and remote I/O modules.

Data stored in the special registers are stored as BIN values if no special designation has been made to the contrary.

The heading descriptions in the following special register lists are shown in Table App. 3.1.

Table App. 3.1. Special register

Item	Function of Item
Number	• Indicates special register number
Name	• Indicates name of special register
Meaning	• Indicates contents of special register
Explanation	• Discusses contents of special register in more detail
Set by (When set)	• Indicates whether the relay is set by the system or user, and, if it is set by the system, when setting is performed. <Set by> S : Set by system U : Set by user (sequence programs or test operations from GX Developer) S/U : Set by both system and user <When set> Indicated only for registers set by system Each END : Set during each END processing Initial : Set only during initial processing (when power supply is turned ON, or when going from STOP to RUN) Status change : Set only when there is a change in status Error : Set when error occurs Instruction execution : Set when instruction is executed Request : Set only when there is a user request (through SM, etc.) System switching : Set when system switching is executed.
Corresponding ACPU M9□□□	• Indicates corresponding special register in ACPU (When the contents are changed, the special register is represented D9□□□ format change. Incompatible with the Q00J/Q00/Q01 and QnPRH.) • New indicates the special register newly added to the QnACPU or Q series CPU module.
Corresponding CPU	Indicates the relevant CPU module. ○ : Indicates all the QnACPU and QCPU. QCPU : Indicates all the Q series CPU modules. Q00J/Q00/Q01 : Indicates the Basic model QCPU. Qn(H) : Indicates the High Performance model QCPU. QnPH : Indicates the Process CPU. QnPRH : Indicates the Redundant CPU. QnU : Indicates the Universal model QCPU QnA : Can be applied to QnA series and Q2ASCPU series Rem : Can be applied to the MELSECNET/H remote I/O modules. Each CPU type name : Can be applied only to the specific CPU. (e.g. Q4AR, Q3A)

For details on the following items, refer to the following manuals:

- Networks → Manual of the corresponding network module
- SFC → QCPU(Q mode)/QnACPU Programming Manual (SFC)

POINT

(1)SD1200 to SD1255 are used for the QnACPU.
These relays are empty for the QCPU.

(1) Diagnostic Information

Table App. 3.2. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD0	Diagnostic errors	Diagnosis error code	- Error codes for errors found by diagnosis are stored as BIN data. - Contents identical to latest fault history information.	S (Error)	D9008 format change	
SD1	Clock time for diagnosis error occurrence	Clock time for diagnosis error occurrence	Year (last two digits) and month that SD0 data was updated is stored as BCD 2-digit code. b15 to b8 b7 to b0 (Example) October, 1995 Year (0 to 99) Month (1 to 12) H9510	S (Error)	New	
SD2			The day and hour that SD0 was updated is stored as BCD 2-digit code. b15 to b8 b7 to b0 (Example) 10 a.m. on 25th Day (1 to 31) Hour (0 to 23) H2510			
SD3			The minute and second that SD0 data was updated is stored as BCD 2-digit code. b15 to b8 b7 to b0 (Example) 35 min. 48 sec. Minutes (0 to 59) Seconds (0 to 59) H3548			
SD4	Error information categories	Error information category code	Category codes which help indicate what type of information is being stored in the common information areas (SD5 through SD15) and the individual information areas (SD16 through SD26) are stored here. The category code for judging the error information type is stored. b15 to b8 b7 to b0 Individual information category codes Common information category codes - The common information category codes store the following codes: 0: No error 1: Unit/module No./ PLC No./Base No.* 2: File name/Drive name 3: Time (value set) 4: Program error location 5: System switching cause (for Q4ARCPU, Redundant CPU only) 6: Reason(s) for tracking capacity excess error (specific to Redundant CPU) 7: Power supply No. 8: Tracking transmission data classification (specific to Redundant CPU) *: For a multiple CPU system that consists of the Basic model QCPU, High Performance model QCPU, Process CPU, Universal model QCPU the module number or CPU number is stored depending on the error that occurred. (Refer to the corresponding error code for which number has been stored.) PLC No. 1: 1, PLC No. 2: 2, PLC No. 3: 3, PLC No. 4: 4 - The individual information category codes store the following codes: 0: No error 1: (Empty) 2: File name/Drive name 3: Time (value actually measured) 4: Program error location 5: Parameter number 6: Annunciator number 7: CHK instruction failure No. (except for the Basic model QCPU and the Universal model QCPU) 8: Reason(s) for system switching failure (specific to Redundant CPU) 12: File diagnostic information (specific to the Universal model QCPU) 13: Parameter No./CPU No. (specific to the Universal model QCPU)	S (Error)	New	○ Rem

Table App. 3.2. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU																																								
SD5	Error common information	Error common information	- Common information corresponding to the error codes (SD0) is stored here. - The following ten types of information are stored here: - The error common information type can be judged by the "common information category code" in SD4. (The values of the "common information category code" stored in SD4 correspond to following 1 to 8, 12,13.) 1) Slot No. <table><tr><th>Number</th><th>Meaning</th></tr><tr><td>SD5</td><td>Slot No./PLC No./Base No. *1, *2, *3, *4</td></tr><tr><td>SD6</td><td>I/O No. *5</td></tr><tr><td>SD7</td><td rowspan="9">(Empty)</td></tr><tr><td>SD8</td></tr><tr><td>SD9</td></tr><tr><td>SD10</td></tr><tr><td>SD11</td></tr><tr><td>SD12</td></tr><tr><td>SD13</td></tr><tr><td>SD14</td></tr><tr><td>SD15</td></tr></table> *1: For a multiple CPU system that consists of the Basic model QCPU, High Performance model QCPU, Process CPU, Universal model QCPU, the slot number or CPU number is stored depending on the error that occurred. Slot 0 in the multiple CPU system is the one on the slot on the right of the rightmost CPU module. (Refer to the corresponding error code for which number has been stored.) No. 1 CPU: 1, No. 2 CPU: 2, No. 3 CPU: 3, No. 4 CPU: 4 *2: If a fuse blown or I/O verify error occurred in the module loaded in the MELSECNET/H remote I/O station, the network number is stored into the upper 8 bits and the station number into the lower 8 bits. Use the I/O No. to check the module where the fuse blown or I/O verify error occurred. *3: 255 is stored into SD5 of the Basic model QCPU when an instruction, etc. has been executed for the module later than the one on the last slot where a module can be mounted. *4: Definitions of base No. and slot No. <Base No.> Value used to identify the base unit on which the CPU module has been mounted. The following shows the definition of the base No. <table><tr><th>Base No.</th><th>Definition</th></tr><tr><td>0</td><td>Indicates the main base unit mounted with the CPU module.</td></tr><tr><td>1 to 7</td><td>Indicates the extension base unit. The stage number setting made by the stage number setting connector on the extension base unit is the base No. When stage number setting is extension 1: Base No. = 1 when stage number setting is extension 7: Base No. = 7</td></tr></table> <Slot No.> Value used to identify the slot of each base unit and the module mounted on that slot. - The I/O slot 0 (slot on the right side of the CPU slot) of the main base unit is defined as the slot of "Slot No. = 0". - The slot Nos. are consecutively assigned to the slots of the base units in order of the main base unit and extension base units 1 to 7. - When the number of base unit slots has been set in the I/O assignment setting of the PLC parameter dialog box, the slot Nos. are assigned for only the number of set slots. *5: When 0FFFFH is stored into SD6 (I/O No.), the I/O No. cannot be identified due to overlapping I/O No., etc. in the I/O assignment setting of the PLC parameter dialog box. Therefore, identify the error location using SD5. 2) File name/Drive name <table><tr><th>Number</th><th>Meaning</th></tr><tr><td>SD5</td><td>Drive</td></tr><tr><td>SD6</td><td rowspan="4">File name (ASCII code: 8 characters)</td></tr><tr><td>SD7</td></tr><tr><td>SD8</td></tr><tr><td>SD9</td></tr><tr><td>SD10</td><td>Extension *6 2EH(.)</td></tr><tr><td>SD11</td><td>(ASCII code: 3 characters)</td></tr><tr><td>SD12</td><td rowspan="4">(Empty)</td></tr><tr><td>SD13</td></tr><tr><td>SD14</td></tr><tr><td>SD15</td></tr></table> (Example) File name = ABCDEFGHI. IJK b15 to b8 b7 to b0 42H(B) 41H(A) 44H(D) 43H(C) 46H(F) 45H(E) 48H(H) 47H(G) 49H(I) 2EH(.) 4BH(K) 4AH(J)	Number	Meaning	SD5	Slot No./PLC No./Base No. *1, *2, *3, *4	SD6	I/O No. *5	SD7	(Empty)	SD8	SD9	SD10	SD11	SD12	SD13	SD14	SD15	Base No.	Definition	0	Indicates the main base unit mounted with the CPU module.	1 to 7	Indicates the extension base unit. The stage number setting made by the stage number setting connector on the extension base unit is the base No. When stage number setting is extension 1: Base No. = 1 when stage number setting is extension 7: Base No. = 7	Number	Meaning	SD5	Drive	SD6	File name (ASCII code: 8 characters)	SD7	SD8	SD9	SD10	Extension *6 2EH(.)	SD11	(ASCII code: 3 characters)	SD12	(Empty)	SD13	SD14	SD15	S (Error)	New	○ Rem
Number			Meaning																																											
SD5			Slot No./PLC No./Base No. *1, *2, *3, *4																																											
SD6			I/O No. *5																																											
SD7			(Empty)																																											
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Number	Meaning																																													
SD5	Drive																																													
SD6	File name (ASCII code: 8 characters)																																													
SD7																																														
SD8																																														
SD9																																														
SD10	Extension *6 2EH(.)																																													
SD11	(ASCII code: 3 characters)																																													
SD12	(Empty)																																													
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Table App. 3.2. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU																
SD5	Error common information	Error common information	3) Time (value set) <table><tr><th>Number</th><th>Meaning</th></tr><tr><td>SD5</td><td>Time : 1μs units (0 to 999μs)</td></tr><tr><td>SD6</td><td>Time : 1ms units (0 to 65535ms)</td></tr><tr><td>SD7</td><td rowspan="9">(Empty)</td></tr><tr><td>SD8</td></tr><tr><td>SD9</td></tr><tr><td>SD10</td></tr><tr><td>SD11</td></tr><tr><td>SD12</td></tr><tr><td>SD13</td></tr><tr><td>SD14</td></tr><tr><td>SD15</td></tr></table>	Number	Meaning	SD5	Time : 1μs units (0 to 999μs)	SD6	Time : 1ms units (0 to 65535ms)	SD7	(Empty)	SD8	SD9	SD10	SD11	SD12	SD13	SD14	SD15	S (Error)	New	○ Rem
Number			Meaning																			
SD5			Time : 1μs units (0 to 999μs)																			
SD6			Time : 1ms units (0 to 65535ms)																			
SD7			(Empty)																			
SD8																						
SD9																						
SD10																						
SD11																						
SD12																						
SD13																						
SD14																						
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Table App. 3.2. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU																																																																																																																							
SD5	Error common information	Error common information	5) Reason(s) for system switching <table><tr><th>Number</th><th>Meaning</th></tr><tr><td>SD5</td><td>System switching condition *13</td></tr><tr><td>SD6</td><td>Control system switching instruction argument</td></tr><tr><td>SD7</td><td rowspan="9">(Empty)</td></tr><tr><td>SD8</td></tr><tr><td>SD9</td></tr><tr><td>SD10</td></tr><tr><td>SD11</td></tr><tr><td>SD12</td></tr><tr><td>SD13</td></tr><tr><td>SD14</td></tr><tr><td>SD15</td></tr></table> *13: Details of reason(s) for system switching 0 : No system switching condition (default) 1 : Power-OFF, reset, hardware failure, watchdog timer error 2 : Stop error (except watchdog timer error) 3 : System switching request by network module 16 : Control system switching instruction 17 : Control system switching request from GX Developer	Number	Meaning	SD5	System switching condition *13	SD6	Control system switching instruction argument	SD7	(Empty)	SD8	SD9	SD10	SD11	SD12	SD13	SD14	SD15	S (Error)	New	QnPRH																																																																																																							
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SD16	Error common information	Error common information	6) Reason(s) for tracking capacity excess error The block No. when the data amount that can be tracked (100k) is exceeded is indicated by the bit pattern of the corresponding special relay. <table><tr><th></th><th>b15</th><th>b14</th><th>b13</th><th>b12</th><th>b11</th><th>b10</th><th>b9</th><th>b8</th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th></tr><tr><td>SD5</td><td>1 (SM1535) (Block16)</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1 (SM1528) (Block9)</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1 (SM1520) (Block1)</td></tr><tr><td>SD6</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>SD7</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>SD8</td><td>1 (SM1583) (Block64)</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1 (SM1568) (Block49)</td></tr><tr><td>SD9</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>SD15</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	SD5	1 (SM1535) (Block16)	0	0	0	0	0	0	1 (SM1528) (Block9)	0	0	0	0	0	0	0	1 (SM1520) (Block1)	SD6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SD7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SD8	1 (SM1583) (Block64)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1 (SM1568) (Block49)	SD9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SD15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	S (Error)	New	Qn(H)*1 QnPH*1 QnPRH
			b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0																																																																																																											
SD5			1 (SM1535) (Block16)	0	0	0	0	0	0	1 (SM1528) (Block9)	0	0	0	0	0	0	0	1 (SM1520) (Block1)																																																																																																											
SD6			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																																																																																																											
SD7			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																																																																																																											
SD8			1 (SM1583) (Block64)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1 (SM1568) (Block49)																																																																																																											
SD9			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																																																																																																											
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SD26	Error common information	Error common information	7) Power supply No. <table><tr><th>Number</th><th>Meaning</th></tr><tr><td>SD5</td><td>Base No.</td></tr><tr><td>SD6</td><td>Power supply No.</td></tr><tr><td>SD7</td><td rowspan="9">(Empty)</td></tr><tr><td>SD8</td></tr><tr><td>SD9</td></tr><tr><td>SD10</td></tr><tr><td>SD11</td></tr><tr><td>SD12</td></tr><tr><td>SD13</td></tr><tr><td>SD14</td></tr><tr><td>SD15</td></tr></table> 1: Power supply 1 fault 2: Power supply 2 fault "Power supply module 1": Redundant power supply module mounted on POWER 1 slot of redundant module 1": base unit (Q38RB, Q68RB) "Power supply module 2": Redundant power supply module mounted on POWER 2 slot of redundant module 2": base unit (Q38RB, Q68RB)	Number	Meaning	SD5	Base No.	SD6	Power supply No.	SD7	(Empty)	SD8	SD9	SD10	SD11	SD12	SD13	SD14	SD15	S (Error)	New	Qn(H)*1 QnPH*1 QnPRH																																																																																																							
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*1: The module whose first 5 digits of serial No. is 07032 or later.

Table App. 3.2. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU															
SD5	Error common information	Error common information	8) Tracking transmission data classification Stores the data classification during tracking. <table><tr><th>Number</th><th>Meaning</th></tr><tr><td>SD5</td><td>Data type *15</td></tr><tr><td>SD6</td><td rowspan="10">(Empty)</td></tr><tr><td>SD7</td></tr><tr><td>SD8</td></tr><tr><td>SD9</td></tr><tr><td>SD10</td></tr><tr><td>SD11</td></tr><tr><td>SD12</td></tr><tr><td>SD13</td></tr><tr><td>SD14</td></tr><tr><td>SD15</td></tr></table> *15: Details of data classification b15 b14 to b6 b5 b4 b3 b2 b1 b0 Each bit 0: Not sent 1: Being sent → Device data → Signal flow → PIDINIT/S. PIDINIT instruction data → SFC execution data → System switching request → Operation mode change request → System data	Number	Meaning	SD5	Data type *15	SD6	(Empty)	SD7	SD8	SD9	SD10	SD11	SD12	SD13	SD14	SD15	S (Error)	New	QnPRH
Number				Meaning																	
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Table App. 3.2. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU																									
SD16	Error common information	Error common information	- Individual information corresponding to error codes (SD0) is stored here. - There are the following eight different types of information are stored. - The error individual information type can be judged by the "individual information category code" in SD4. (The values of the "individual information category code" stored in SD4 correspond to following 1) to 8).)	S (Error)	New	○ Rem																									
SD17			1) (Empty) 2) File name/Drive name (Example) File name = ABCDEFGH. IJK b15 to b8 b7 to b0 <table><tr><th>Number</th><th>Meaning</th></tr><tr><td>SD16</td><td>Drive</td></tr><tr><td>SD17</td><td rowspan="4">File name (ASCII code: 8 characters)</td></tr><tr><td>SD18</td></tr><tr><td>SD19</td></tr><tr><td>SD20</td></tr><tr><td>SD21</td><td>Extension *6</td><td>2EH(.)</td></tr><tr><td>SD22</td><td>(ASCII code: 3 characters)</td><td></td></tr><tr><td>SD23</td><td rowspan="4">(Empty)</td></tr><tr><td>SD24</td></tr><tr><td>SD25</td></tr><tr><td>SD26</td></tr></table>				Number	Meaning	SD16	Drive	SD17	File name (ASCII code: 8 characters)	SD18	SD19	SD20	SD21	Extension *6	2EH(.)	SD22	(ASCII code: 3 characters)		SD23	(Empty)	SD24	SD25	SD26					
Number			Meaning																												
SD16			Drive																												
SD17			File name (ASCII code: 8 characters)																												
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SD21			Extension *6				2EH(.)																								
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SD26																															
SD18																															
SD19			3) Time (value actually measured) <table><tr><th>Number</th><th>Meaning</th></tr><tr><td>SD16</td><td>Time : 1μs units (0 to 999μs)</td></tr><tr><td>SD17</td><td>Time : 1ms units (0 to 65535ms)</td></tr><tr><td>SD18</td><td rowspan="8">(Empty)</td></tr><tr><td>SD19</td></tr><tr><td>SD20</td></tr><tr><td>SD21</td></tr><tr><td>SD22</td></tr><tr><td>SD23</td></tr><tr><td>SD24</td></tr><tr><td>SD25</td></tr><tr><td>SD26</td></tr></table>				Number	Meaning	SD16	Time : 1μs units (0 to 999μs)	SD17	Time : 1ms units (0 to 65535ms)	SD18	(Empty)	SD19	SD20	SD21	SD22	SD23	SD24	SD25	SD26									
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SD23																															
SD24																															
SD25																															
SD26																															
SD20																															
SD21	4) Program error location <table><tr><th>Number</th><th>Meaning</th></tr><tr><td>SD16</td><td rowspan="4">File name (ASCII code: 8 characters)</td></tr><tr><td>SD17</td></tr><tr><td>SD18</td></tr><tr><td>SD19</td></tr><tr><td>SD20</td><td>Extension *6</td><td>2EH(.)</td></tr><tr><td>SD21</td><td>(ASCII code: 3 characters)</td><td></td></tr><tr><td>SD22</td><td>Pattern *7</td><td></td></tr><tr><td>SD23</td><td>Block No.</td><td></td></tr><tr><td>SD24</td><td>Step No./transition No.</td><td></td></tr><tr><td>SD25</td><td>Sequence step No. (L)</td><td></td></tr><tr><td>SD26</td><td>Sequence step No. (H)</td><td></td></tr></table>	Number	Meaning	SD16	File name (ASCII code: 8 characters)	SD17	SD18	SD19	SD20	Extension *6	2EH(.)	SD21	(ASCII code: 3 characters)		SD22	Pattern *7		SD23	Block No.		SD24	Step No./transition No.		SD25	Sequence step No. (L)		SD26	Sequence step No. (H)			
Number	Meaning																														
SD16	File name (ASCII code: 8 characters)																														
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SD25	Sequence step No. (L)																														
SD26	Sequence step No. (H)																														
SD22																															
SD23	*7 : Contents of pattern data <table><tr><td>15</td><td>14</td><td>to</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>←(Bit number)</td></tr><tr><td>0</td><td>0</td><td>to</td><td>0</td><td>0</td><td>*</td><td>*</td><td>*</td><td></td></tr></table> (Not used) SFC block designation present (1)/absent (0) SFC step designation present (1)/absent (0) SFC transition designation present (1)/absent (0)	15	14	to	4	3	2	1	0	←(Bit number)	0	0	to	0	0	*	*	*													
15	14	to	4	3	2	1	0	←(Bit number)																							
0	0	to	0	0	*	*	*																								
SD24																															
SD25	5) Parameter No. 6) Annunciator number / 7) CHK instruction malfunction number <table><tr><th>Number</th><th>Meaning</th></tr><tr><td>SD16</td><td>Parameter No. *16</td></tr><tr><td>SD17</td><td rowspan="10">(Empty)</td></tr><tr><td>SD18</td></tr><tr><td>SD19</td></tr><tr><td>SD20</td></tr><tr><td>SD21</td></tr><tr><td>SD22</td></tr><tr><td>SD23</td></tr><tr><td>SD24</td></tr><tr><td>SD25</td></tr><tr><td>SD26</td></tr></table><table><tr><th>Number</th><th>Meaning</th></tr><tr><td>SD16</td><td>No.</td></tr><tr><td>SD17</td><td rowspan="10">(Empty)</td></tr><tr><td>SD18</td></tr><tr><td>SD19</td></tr><tr><td>SD20</td></tr><tr><td>SD21</td></tr><tr><td>SD22</td></tr><tr><td>SD23</td></tr><tr><td>SD24</td></tr><tr><td>SD25</td></tr><tr><td>SD26</td></tr></table>	Number	Meaning	SD16	Parameter No. *16	SD17	(Empty)	SD18	SD19	SD20	SD21	SD22	SD23	SD24	SD25	SD26	Number	Meaning	SD16	No.	SD17	(Empty)	SD18	SD19	SD20	SD21	SD22	SD23	SD24	SD25	SD26
Number	Meaning																														
SD16	Parameter No. *16																														
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SD25																															
SD26																															
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SD21																															
SD22																															
SD23																															
SD24																															
SD25																															
SD26																															
SD26	*16: For details of the parameter No., refer to the QCPU User's Manual (Function Explanation・Program Fundamentals) or to the User's Manual of the CPU module used.																														

REMARK

*6 : Extensions are shown below.

Table App. 3.3. Extension name

SDn	SDn+1		Extension Name	File Type
	Lower 8 bits	Higher 8 bits		
51H	50H	41H	QPA	Parameters
51H	50H	47H	QPG	• Sequence program • SFC program
51H	43H	44H	QCD	Device comment
51H	44H	49H	QDI	Initial device value
51H	44H	52H	QDR	File register
51H	44H	53H	QDS	Simulation data (For QnA)
51H	44H	4CH	QDL	Local device (Other than the Basic model QCPU)
51H	54H	44H	QTD	Sampling trace data (Other than the Basic model QCPU)
51H	54H	4CH	QTL	Status latch data (For QnA)
51H	54H	50H	QTP	Program trace data (For QnA)
51H	54H	52H	QTR	SFC trace file (For QnA)
51H	46H	44H	QFD	Breakdown history data (Other than the Basic model QCPU and the Universal model QCPU)
51H	46H	44H	QST	SP.DEVST/S.DEVLD instruction file (For Universal model QCPU only)

Table App. 3.2. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU																		
SD26	Error common information	Error common information	8) Reason(s) for system switching failure <table><tr><th>Number</th><th>Meaning</th></tr><tr><td>SD16</td><td>System switching prohibition condition *14</td></tr><tr><td>SD17</td><td rowspan="10">(Empty)</td></tr><tr><td>SD18</td></tr><tr><td>SD19</td></tr><tr><td>SD20</td></tr><tr><td>SD21</td></tr><tr><td>SD22</td></tr><tr><td>SD23</td></tr><tr><td>SD24</td></tr><tr><td>SD25</td></tr><tr><td>SD26</td></tr></table> *14: Details of reason(s) for system switching failure 0 : Normal switching completion (default) 1 : Tracking cable fault (cable removal, cable fault, internal circuit fault, hardware fault) 2 : Hardware failure, power OFF, reset or watchdog timer error occurring in standby system 3 : Hardware failure, power OFF, reset or watchdog timer error occurring in control system 4 : Preparing for tracking 5 : Time limit exceeded 6 : Standby system is in stop error (except watchdog timer error) 7 : Operation differs between two systems (in backup mode only) 8 : During memory copy from control system to standby system 9 : Online program change 10 : Error detected by network module of standby system 11 : System switching being executed 12 : Online module change in progress	Number	Meaning	SD16	System switching prohibition condition *14	SD17	(Empty)	SD18	SD19	SD20	SD21	SD22	SD23	SD24	SD25	SD26	S (Error)	New	QnPRH			
			Number	Meaning																				
			SD16	System switching prohibition condition *14																				
SD17	(Empty)																							
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SD23																								
SD24																								
SD25																								
SD26																								
12) File diagnostic information <table><tr><td>SD16</td><td>Failuer information (H)</td><td>drive No.(L)</td></tr><tr><td>SD17</td><td colspan="2" rowspan="4">File name (ASCII: 8 characters)</td></tr><tr><td>SD18</td></tr><tr><td>SD19</td></tr><tr><td>SD20</td></tr><tr><td>SD21</td><td>EXtension *6</td><td>2EH(.)</td></tr><tr><td>SD22</td><td colspan="2">(ASCII; 3 characters)</td></tr><tr><td>SD23</td><td colspan="2">Failure information 2 (CRC value that is read)</td></tr><tr><td>SD24</td><td colspan="2" rowspan="3">Failure information 3 (CRC value that is calculated)</td></tr><tr><td>SD25</td></tr><tr><td>SD26</td></tr></table>	SD16	Failuer information (H)	drive No.(L)	SD17	File name (ASCII: 8 characters)		SD18	SD19	SD20	SD21	EXtension *6	2EH(.)	SD22	(ASCII; 3 characters)		SD23	Failure information 2 (CRC value that is read)		SD24	Failure information 3 (CRC value that is calculated)		SD25	SD26	QnU
SD16	Failuer information (H)	drive No.(L)																						
SD17	File name (ASCII: 8 characters)																							
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SD19																								
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SD21	EXtension *6	2EH(.)																						
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SD23	Failure information 2 (CRC value that is read)																							
SD24	Failure information 3 (CRC value that is calculated)																							
SD25																								
SD26																								
13) Parameter No./CPU No. <table><tr><th>Number</th><th>Meaning</th></tr><tr><td>SD16</td><td>Parameter No.*16</td></tr><tr><td>SD17</td><td>CPU No. (1 to 4)</td></tr><tr><td>SD18</td><td rowspan="10">(Empty)</td></tr><tr><td>SD19</td></tr><tr><td>SD20</td></tr><tr><td>SD21</td></tr><tr><td>SD22</td></tr><tr><td>SD23</td></tr><tr><td>SD24</td></tr><tr><td>SD25</td></tr><tr><td>SD26</td></tr></table>	Number	Meaning	SD16	Parameter No.*16	SD17	CPU No. (1 to 4)	SD18	(Empty)	SD19	SD20	SD21	SD22	SD23	SD24	SD25	SD26								
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SD26																								

Table App. 3.2. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD50	Error reset	Error number that performs error reset	Stores error number that performs error reset	U	New	○ Rem
SD51	Battery low latch	Bit pattern indicating where battery voltage drop occurred	- All corresponding bits go 1(ON) when battery voltage drops. - Subsequently, these remain 1(ON) even after battery voltage has been returned to normal. *: This does not apply to Basic model QCPU. - In the alarm, data can be held within the time specified for battery low. - The error indicates the complete discharge of the battery. - When the High Performance model QCPU, Process CPU, Redundant CPU or Universal model QCPU is used, the corresponding bits always remain OFF since the memory card B is a standard memory.	S (Error)	New	○
SD52	Battery low	Bit pattern indicating where battery voltage drop occurred	- Same configuration as SD51 above - After the alarm is detected (ON), the alarm turns OFF by error detection (ON). (For the Universal model QCPU only) - Turns to 0 (OFF) when the battery voltage returns to normal thereafter. - When the High Performance model QCPU, Process CPU, Redundant CPU or Universal model QCPU is used, the corresponding bits always remain OFF since the memory card B is a standard memory..	S (Error)	New	
SD53	AC/DC DOWN detection	Number of times for AC/DC DOWN detection	Every time the input voltage falls to or below 85% (AC power)/65% (DC power) of the rating during operation of the CPU module, the value is incremented by 1 and stored in BIN code.	S (Error)	D9005	○ Rem
SD54	MINI link errors	Error detection state	- When any of $X(n+0)/X(n+20)$, $X(n+6)/X(n+26)$, $X(n+7)/X(n+27)$ and $X(n+8)/X(n+28)$ of the mounted MINI(-S3) turns ON, the bit of the corresponding station turns to 1 (ON). - Turns to 1 (ON) when communication between the mounted MINI(-S3) and CPU module cannot be made.	S (Error)		QnA
SD60	Number of module with blown fuse	Number of module with blown fuse	Value stored here is the lowest station I/O number of the module with the blown fuse.	S (Error)		○ Rem
SD61	I/O module verify error number	I/O module verify error module number	The lowest I/O number of the module where the I/O module verification number took place.	S (Error)		

Table App. 3.2. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD62	Annunciator number	Annunciator number	• The first annunciator number (F number) to be detected is stored here.	S (Instruction execution)	D9009	○
SD63	Number of annunciators	Number of annunciators	• Stores the number of annunciators searched.	S (Instruction execution)	D9124	
SD64	Table of detected annunciator numbers	Annunciator detection number	When F goes ON due to OUT F or SET F , the F numbers which go progressively ON from SD64 through SD79 are registered.	S (Instruction execution)	D9125	
SD65			The F numbers turned OFF by RST F are deleted from SD64 - SD79, and the F numbers stored after the deleted F numbers are shifted to the preceding registers.		D9126	
SD66			Execution of the LEDR instruction shifts the contents of SD64 to SD79 up by one. (This can also be done by using the INDICATOR RESET switch on the of the Q3A/Q4ACPU.)		D9127	
SD67			After 16 annunciators have been detected, detection of the 17th will not be stored from SD64 through SD79.		D9128	
SD68					D9129	
SD69					D9130	
SD70					D9131	
SD71					D9132	
SD72					New	
SD73					New	
SD74					New	
SD75					New	
SD76					New	
SD77					New	
SD78					New	
SD79					New	
SD80	CHK number	CHK number	• Error codes detected by the CHK instruction are stored as BCD code.	S (Instruction execution)	New	QnA Qn(H) QnPH QnPRH
SD90	Step transition monitoring timer setting value (Enabled only when SFC program exists)	F number for timer set value and time over error	Corresponds to SM90	U	D9108	QnA Qn(H) QnPH QnPRH
SD91			Corresponds to SM91		D9109	
SD92			Corresponds to SM92		D9110	
SD93			Corresponds to SM93		D9111	
SD94			Corresponds to SM94		D9112	
SD95			Corresponds to SM95		D9113	
SD96			Corresponds to SM96		D9114	
SD97			Corresponds to SM97		New	
SD98			Corresponds to SM98		New	
SD99			Corresponds to SM99		New	

Table App. 3.2. Special register

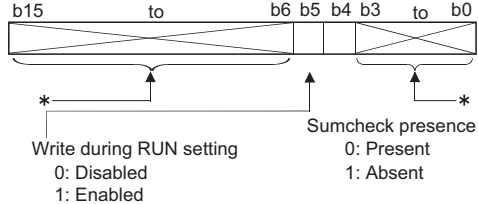
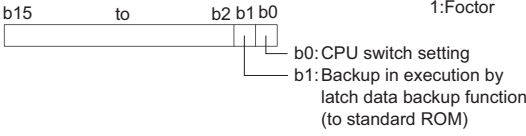
Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD100	Transmission speed storage area	Stores the transmission speed specified in the serial communication setting.	96 : 9.6kbps, 192 : 19.2kbps, 384 : 38.4kbps, 576 : 57.6kbps, 1152 : 115.2kbps	S (Power-ON or reset)	New	Q00/Q01
SD101	Communication setting storage area	Stores the communication setting specified in the serial communication setting.	 * : Since the data is used by the system, it is undefined.	S (Power-ON or reset)	New	
SD102	Transmission wait time storage area	Stores the transmission wait time specified in the serial communication setting.	0: No waiting time 1 to FH: Waiting time (unit: 10ms) Defaults to 0.	S (Power-ON or reset)	New	
SD105	CH1 transmission speed setting (RS-232)	Stores the preset transmission speed when GX Developer is used.	96 : 9600bps, 192 : 19.2kbps, 384 : 38.4kbps, 576 : 57.6kbps, 1152 : 115.2kbps *: Other than RS-232 connection holds the data at RS-232 connection. (When disconnected, the default value is 1152.)	S	New	Qn(H) QnPH QnPRH QnU Rem
SD110	Data sending result storage area	Stores the data sending result when the serial communication function is used.	Stores the error code at the timeout sending data.	S (Error)	New	Q00/Q01
SD111	Data receiving result storage area	Stores the data receiving result when the serial communication function is used.	Stores the error code at the time of receiving data.	S (Error)		
SD119	Battery life-prolonging factor	Battery life-prolonging factor	Stores the factor which makes the battery life-prolonging function valid. When SD119 is other than 0, the battery life-prolonging function is valid. 	S (Status change)	New	QnU

Table App. 3.2. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU																																																																				
SD130	Fuse blown module	Bit pattern in units of 16 points, indicating the modules whose fuses have blown 0: No blown fuse 1: Blown fuse present	- The numbers of output modules whose fuses have blown are input as a bit pattern (in units of 16 points). (If the module numbers are set by parameter, the parameter-set numbers are stored.) b15b14b13b12b11b10b9b8b7b6b5b4b3b2b1b0 <table><tr><td>SD130</td><td>0</td><td>0</td><td>0</td><td>1 (Y_{C0})</td><td>0</td><td>0</td><td>0</td><td>1 (Y₈₀)</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>SD131</td><td>1 (Y_{1F0})</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1 (Y_{1A0})</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td colspan="17">~~~~~</td></tr><tr><td>SD137</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1 (Y_{7B0})</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1 (Y₇₃₀)</td><td>0</td><td>0</td><td>0</td></tr></table> ↑ Indicates fuse blow. - Not cleared even if the blown fuse is replaced with a new one.	SD130	0	0	0	1 (Y _{C0})	0	0	0	1 (Y ₈₀)	0	0	0	0	0	0	0	0	SD131	1 (Y _{1F0})	0	0	0	0	1 (Y _{1A0})	0	0	0	0	0	0	0	0	0	0	~~~~~																	SD137	0	0	0	0	1 (Y _{7B0})	0	0	0	0	0	0	0	1 (Y ₇₃₀)	0	0	0	S (Error)	New	Q00J/Q00/Q01
SD130			0	0	0	1 (Y _{C0})	0	0	0	1 (Y ₈₀)	0	0	0	0	0	0	0	0																																																								
SD131			1 (Y _{1F0})	0	0	0	0	1 (Y _{1A0})	0	0	0	0	0	0	0	0	0	0																																																								
~~																																																																										
SD137			0	0	0	0	1 (Y _{7B0})	0	0	0	0	0	0	0	1 (Y ₇₃₀)	0	0	0																																																								
SD131																																																																										
SD132																																																																										
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SD135																																																																										
SD136																																																																										
SD137																																																																										
SD150	I/O module verify error	Bit pattern, in units of 16 points, indicating the modules with verify errors. 0: No I/O verify errors 1: I/O verify error present	- When I/O modules, of which data are different from those entered at power-ON, have been detected, the I/O module numbers (in units of 16 points) are entered in bit pattern. (Preset I/O module numbers set in parameters when parameter setting has been performed.) b15b14b13b12b11b10b9b8b7b6b5b4b3b2b1b0 <table><tr><td>SD150</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1 (X₀^Y)</td></tr><tr><td>SD151</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1 (X₁₉₀^Y)</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td colspan="17">~~~~~</td></tr><tr><td>SD157</td><td>0</td><td>1 (X_{7E0}^Y)</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> ↑ Indicates an I/O module verify error. - Not cleared even if the blown fuse is replaced with a new one. This flag is cleared by error resetting operation.	SD150	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1 (X ₀ ^Y)	SD151	0	0	0	0	0	0	1 (X ₁₉₀ ^Y)	0	0	0	0	0	0	0	0	0	~~~~~																	SD157	0	1 (X _{7E0} ^Y)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	S (Error)	New	Q00J/Q00/Q01
SD150			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1 (X ₀ ^Y)																																																								
SD151			0	0	0	0	0	0	1 (X ₁₉₀ ^Y)	0	0	0	0	0	0	0	0	0																																																								
~~																																																																										
SD157			0	1 (X _{7E0} ^Y)	0	0	0	0	0	0	0	0	0	0	0	0	0	0																																																								
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SD154																																																																										
SD155																																																																										
SD156																																																																										
SD157																																																																										

(2) System information

Table App. 3.4. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD200	Status of switch	Status of CPU switch	The switch status of the remote I/O module is stored in the following format. b15 to b4 b3 to b0 Empty 1) 1) Remote I/O module switch statusAlways 1: STOP	S (Always)	New	Rem
			The CPU switch status is stored in the following format: b15 to b12 b11 to b8 b7 to b4 b3 to b0 3) Empty 2) 1) 1): CPU switch status0: RUN 1: STOP 2: L.CLR 2): Memory card switchAlways OFF 3): DIP switchb8 through b12 correspond to SW1 through SW5 of system setting switch 1. 0: OFF, 1: ON. b13 through b15 are empty.	S (Every END processing)	New	Qn(H) QnPH QnPRH
			The CPU switch status is stored in the following format: b15 to b8 b7 to b4 b3 to b0 Empty 2) 1) 1): CPU switch status0: RUN 1: STOP 2): Memory card switchAlways OFF	S (Every END processing)	New	Q00J/Q00/Q01
			The CPU switch status is stored in the following format: b15 to b8 b7 to b4 b3 to b0 Empty 2) 1) 1): CPU switch status0: RUN 1: STOP 2): Memory card switchAlways OFF	S (when RUN/STOP/RESET switch changed)	New	QnU
			The CPU switch status is stored in the following format: b15 to b12 b11 to b8 b7 to b4 b3 to b0 3) Empty 2) 1) 1): CPU switch status0: RUN 1: STOP 2: L.CLR 2): Memory card switchb4 corresponds to memory card A, and b5 corresponds to memory card B. 0: OFF, 1: ON 3): DIP switchb8 through b12 correspond to SW1 through SW5 of system setting switch 1. b14 and b15 correspond to SW1 and SW2 of system setting switch 2, respectively. OFF at 0; ON at 1	S (Every END processing)	New	QnA

Table App. 3.4. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD201	LED status	Status of CPU-LED	- The following bit patterns store the status of the LEDs on the CPU module: 0 is off, 1 is on, and 2 is flicker. 1): RUN5): BOOT 2): ERR.6): EmptyMode bit pattern 3): USER7): Empty0: OFF 1: Green 4): BAT.8): MODE2: Orange (The Basic model QCPU does not include 3) to 8).)	S (Status change)	New	Q00J/Q00/Q01 Qn(H) QnPH QnPRH
			- The following bit patterns store the status of the LEDs on the CPU module: 0 is off, 1 is on, and 2 is flicker. 1): RUN 5): BOOT 2): ERROR 6): Empty 3): USER 7): Empty 4): BAT. 8): MODE	S (Status change)	New	QnU
			- The following bit patterns store the status of the LEDs on the CPU module: 0 is off, 1 is on, and 2 is flicker 1): RUN 5): BOOT 2): ERROR 6): CARD A (memory card A) 3): USER 7): CARD B (memory card B) 4): BAT.ALARM 8): Empty	S (Status change)	New	QnA
SD202	LED off command	Bit pattern of LED that is turned off	- Stores bit patterns of LEDs turned off (Only USER and BOOT enabled) - Turned off at 1, not turned off at 0	U	New	
			- Specify the LEDs to be turned off using this register, and turn SM202 from OFF to ON to turn off the specified LEDs. USER and BOOT can be specified as the LEDs to be turned off. - Specify the LEDs to be turned off in the following bit pattern. (Turned off at 1, not be turned off at 0.)	U	New	Qn(H) QnPH QnPRH QnU

Table App. 3.4. Special register

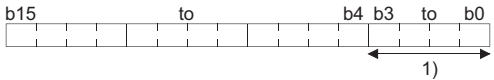
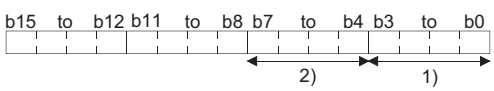
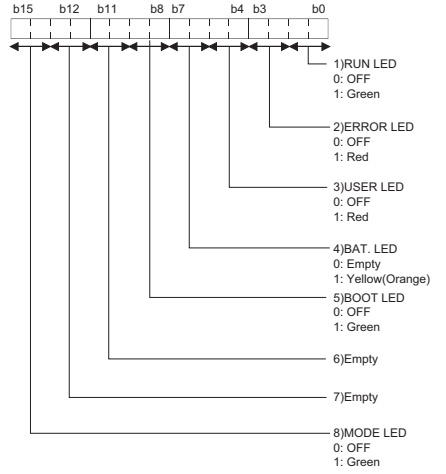
Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD203	Operating status of CPU	Operating status of CPU	The operating status of the remote I/O module is stored in the following format.  1) Remote I/O module operating status Always 2: STOP	S (Always)	New	Rem
			The CPU operating status is stored as indicated in the following figure:  1): Operating status of CPU 0: RUN 1: STEP-RUN (For the QnACPU only) 2: STOP 3: PAUSE 2): STOP/PAUSE cause 0: Instruction in remote operation program from RUN/STOP switch ("RUN/STOP/RESET switch" for Basic model QCPU) 1: Remote contact 2: Remote operation from GX Developer/serial communication, etc. 3: Internal program instruction Note: Priority is earliest first 4: Error	S (Every END processing)	D9015 format change	○
SD204	LED display color	CPU-LED display color	The LED display color of the LED status shown in SD201 1) to 8).  1) RUN LED 0: OFF 1: Green 2) ERROR LED 0: OFF 1: Red 3) USER LED 0: OFF 1: Red 4) BAT. LED 0: Empty 1: Yellow(Orange) 5) BOOT LED 0: OFF 1: Green 6) Empty 7) Empty 8) MODE LED 0: OFF 1: Green	S (status change)	New	QnU

Table App. 3.4. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU																
SD206	Device test execution type	0: Test not yet executed 1: During X device test 2: During Y device test 3: During X/Y device test	Set when the device test mode is executed on GX Developer.	S (Request)	New	Rem																
SD207	LED display priority ranking	Priorities 1 to 4	- When error is generated, the LED display (flicker) is made according to the error number setting priorities. (The Basic model QCPU supports only the annunciator (error item No. 7). - The Universal model QCPU sets execution/non-execution of LED display of the error corresponding to the each priority ranking when the error occurs. - The setting areas for priorities are as follows: b15 to b12 b11 to b8 b7 to b4 b3 to b0 <table><tr><td>SD207</td><td>Priority 4</td><td>Priority 3</td><td>Priority 2</td><td>Priority 1</td></tr><tr><td>SD208</td><td>Priority 8</td><td>Priority 7</td><td>Priority 6</td><td>Priority 5</td></tr><tr><td>SD209</td><td>Priority 11</td><td>Priority 10</td><td>Priority 9</td><td></td></tr></table> (Priority 11 is valid when Redundant CPU is used.) Default Value SD207 = 4321H(0000H for Basic model QCPU) SD208 = 8765H(0700H for Basic model QCPU) (0765H for Redundant CPU) SD209 = 00A9H(0000H for Basic model QCPU) (0B09H for Redundant CPU) - No display is made if "0" is set. - In case of the Basic model QCPU, the ERR. LED turns ON when the annunciator turns ON, if "7" has been set to either of priorities 1 to 11. - In case of the Basic model QCPU, the ERR. LED does not turn ON when the annunciator turns ON, if "7" has not been set to either of priorities 1 to 11. However, even if "0" has been set, information concerning CPU module operation stop (including parameter settings) errors will be indicated by the LEDs without conditions.	SD207	Priority 4	Priority 3	Priority 2	Priority 1	SD208	Priority 8	Priority 7	Priority 6	Priority 5	SD209	Priority 11	Priority 10	Priority 9		U	D9038	QnA Q00J/ Q00/Q01 ⁹ Qn(H) QnPH QnPRH QnU	
SD207		Priority 4	Priority 3	Priority 2	Priority 1																	
SD208		Priority 8	Priority 7	Priority 6	Priority 5																	
SD209	Priority 11	Priority 10	Priority 9																			
SD208	Priorities 5 to 8	D9039 format change																				
SD209	Priorities 9 to 11	New																				
SD210	Clock data	Clock data (year, month)	The year (last two digits) and month are stored as BCD code as shown below: b15 to b12 b11 to b8 b7 to b4 b3 to b0 <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> Year Month Example: July, 1993 9307_H																	S (Request)/U	D9025	○ Rem
SD211	Clock data	Clock data (day, hour)	The day and hour are stored as BCD code as shown below: b15 to b12 b11 to b8 b7 to b4 b3 to b0 <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> Day Hour Example: 31st, 10 a.m. 3110_H																	D9026		
SD212	Clock data	Clock data (minute, second)	The minutes and seconds (after the hour) are stored as BCD code as shown below: b15 to b12 b11 to b8 b7 to b4 b3 to b0 <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> Minute Second Example: 35 min, 48 s 3548_H																	D9027		

*9: Function version is B or later.

Table App. 3.4. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU																								
SD213	Clock data	Clock data (later digits of year, day of week)	The year (first two digits) and the day of the week are stored as BCD code as shown below. b15 to b12 b11 to b8 b7 to b4 b3 to b0 Example: 1993, Friday 1905_H <table><tr><td>Day of the week</td></tr><tr><td>0 Sunday</td></tr><tr><td>1 Monday</td></tr><tr><td>2 Tuesday</td></tr><tr><td>3 Wednesday</td></tr><tr><td>4 Thursday</td></tr><tr><td>5 Friday</td></tr><tr><td>6 Saturday</td></tr></table> Higher digits of year (0 to 99) <td rowspan="2">S (Request)/U</td> <td rowspan="2">D9028</td> <td>QCPU Rem</td>	Day of the week	0 Sunday	1 Monday	2 Tuesday	3 Wednesday	4 Thursday	5 Friday	6 Saturday	S (Request)/U	D9028	QCPU Rem																
		Day of the week																												
0 Sunday																														
1 Monday																														
2 Tuesday																														
3 Wednesday																														
4 Thursday																														
5 Friday																														
6 Saturday																														
Clock data (day of week)	The day of the week is stored as BCD code as shown below. b15 to b12 b11 to b8 b7 to b4 b3 to b0 Example: Friday 0005_H <table><tr><td>Day of the week</td></tr><tr><td>0 Sunday</td></tr><tr><td>1 Monday</td></tr><tr><td>2 Tuesday</td></tr><tr><td>3 Wednesday</td></tr><tr><td>4 Thursday</td></tr><tr><td>5 Friday</td></tr><tr><td>6 Saturday</td></tr></table> Always set "0". <td>QnA</td>	Day of the week	0 Sunday	1 Monday	2 Tuesday	3 Wednesday	4 Thursday	5 Friday	6 Saturday	QnA																				
Day of the week																														
0 Sunday																														
1 Monday																														
2 Tuesday																														
3 Wednesday																														
4 Thursday																														
5 Friday																														
6 Saturday																														
SD220	LED display data	LED display data	LED display ASCII data (16 characters) stored here. (On the Basic model QCPU, the registers store the message (16 characters of ASCII data) at error occurrence (including annunciator ON). b15 to b8 b7 to b0 <table><tr><td>SD220</td><td>15th character from the right</td><td>16th character from the right</td></tr><tr><td>SD221</td><td>13th character from the right</td><td>14th character from the right</td></tr><tr><td>SD222</td><td>11th character from the right</td><td>12th character from the right</td></tr><tr><td>SD223</td><td>9th character from the right</td><td>10th character from the right</td></tr><tr><td>SD224</td><td>7th character from the right</td><td>8th character from the right</td></tr><tr><td>SD225</td><td>5th character from the right</td><td>6th character from the right</td></tr><tr><td>SD226</td><td>3rd character from the right</td><td>4th character from the right</td></tr><tr><td>SD227</td><td>1st character from the right</td><td>2nd character from the right</td></tr></table> <td rowspan="8">S (When changed)</td> <td rowspan="8">New</td> <td rowspan="8">○</td>	SD220	15th character from the right	16th character from the right	SD221	13th character from the right	14th character from the right	SD222	11th character from the right	12th character from the right	SD223	9th character from the right	10th character from the right	SD224	7th character from the right	8th character from the right	SD225	5th character from the right	6th character from the right	SD226	3rd character from the right	4th character from the right	SD227	1st character from the right	2nd character from the right	S (When changed)	New	○
SD220			15th character from the right	16th character from the right																										
SD221			13th character from the right	14th character from the right																										
SD222			11th character from the right	12th character from the right																										
SD223			9th character from the right	10th character from the right																										
SD224			7th character from the right	8th character from the right																										
SD225			5th character from the right	6th character from the right																										
SD226			3rd character from the right	4th character from the right																										
SD227	1st character from the right	2nd character from the right																												
SD221																														
SD222																														
SD223																														
SD224																														
SD225																														
SD226																														
SD227	The LED display device data at the time of CHK is not stored in the Basic model QCPU and the Universal model QCPU.																													
SD235	Module to which online module change is being performed	The header I/O number of the module to which online module change is being performed /10H	10H is added to the value of the header I/O number of which the online module change is being performed.	S (During online module change)	New	QnPH QnPRH																								
SD240	Base mode	0: Automatic mode 1: Detail mode	Stores the base mode.	S (Initial)	New	QCPU Rem																								
SD241	Extension stage number	0: Main base only 1 to 7: Extension stage number	Stores the maximum number of the extension bases being installed.	S (Initial)	New																									

Table App. 3.4. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD242	A/Q base differentiation	Base type differentiation 0: QA**B is installed (A mode) 1: Q**B is installed (Q mode)		S (Initial)	New	Qn(H) QnPH QnPRH Rem
	Installed Q base presence/absence	Base type differentiation 0: Base not installed 1: Q**B is installed		S (Initial)	New	Q00J/Q00/Q01 Rem
	Installed Q base presence/absence	Base type differentiation 0: Base not installed 1: Q**B is installed		S (Initial)	New	QnU
SD243	No. of base slots	No. of base slots		S (Initial)	New	Qn(H) QnPH QnPRH QnU Rem
SD244	No. of base slots	No. of base slots		S (Initial)	New	Qn(H) QnPH QnPRH QnU Rem
SD243	No. of base slots (Operation status)	No. of base slots		S (Initial)	New	Q00J/Q00/Q01
SD244	No. of base slots (Operation status)	No. of base slots		S (Initial)	New	Q00J/Q00/Q01 ^{*9}
SD245	No. of base slots (Mounting status)	No. of base slots		S (Initial)	New	Qn(H) QnPH QnPRH Rem
SD246	No. of base slots (Mounting status)	No. of base slots		S (Initial)	New	Q00J/Q00/Q01 ^{*9}
SD250	Loaded maximum I/O	Loaded maximum I/O No.	- When SM250 goes from OFF to ON, the upper 2 digits of the final I/O number plus 1 of the modules loaded are stored as BIN values. - The upper 2 digits of the final I/O number plus 1 of the modules loaded are stored as BIN values.	S (Request END)	New	Qn(H) QnPH QnPRH Rem
SD251	Head I/O number for replacement	Head I/O No. for module replacement	Stores the upper two digits of the head I/O number of an I/O module that is removed/replaced in the online status (with power on). (Default value: 100H).	U	D9094	Q2A(S1) Q3A Q4A Q4AR
SD253	RS422 transmission speed	RS422 transmission speed	Stores transmission speed of RS422. 0 : 9600bps 1 : 19.2kbps 2 : 38.4kbps	S (When changed)	New	QnA

*9: Function version is B or later.

Table App. 3.4. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD254	MELSECNET/ 10. MELSECNET/H information	Number of modules installed	• Indicates the number of mounted MELSECNET/10 modules or MELSECNET/H modules.	S (Initial)	New	○
SD255		Information from 1st module	I/O No.			
SD256			Network No.			
SD257			Group number			
SD258			Station No.			
SD259		Standby information	• In the case of standby stations, the module number of the standby station is stored. (1 to 4)			QnA Qn(H) QnPH QnPRH QnU
SD260 to SD264		Information from 2nd module	• Configuration is identical to that for the first module.			QnA Qn(H) QnPH QnPRH QnU
SD265 to SD269		Information from 3rd module	• Configuration is identical to that for the first module.			QnA Qn(H) QnPH QnPRH QnU ^{*10}
SD270 to SD274		Information from 4th module	• Configuration is identical to that for the first module.			
SD280	CC-Link error	Error detection status	1) When Xn0 of the mounted CC-Link module turns ON, the bit of the corresponding station turns to 1 (ON). 2) When either Xn1 or XnF of the mounted CC-Link module turns OFF, the bit of the corresponding station turns to 1 (ON). 3) Turns to 1 (ON) when communication between the mounted CC-Link module and CPU module cannot be made. The above module Nos. n are in order of the head I/O numbers. (However, the one where parameter setting has not been made is not counted.)	S (Error)	New	Qn(H) QnPH QnPRH Rem
			• When Xn0 of the mounted CC-Link module turns ON, the bit of the corresponding station turns to 1 (ON). • When either Xn1 or XnF of the mounted CC-Link module turns OFF, the bit of the corresponding station turns to 1 (ON). • Turns to 1 (ON) when communication between the mounted CC-Link module and CPU module cannot be made.	S (Error)	New	QnA

*10: The Universal model QCPU except the Q02UCPU.

Table App. 3.4. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD281	CC-Link error	Error detection status	1) When Xn0 of the mounted CC-Link module turns ON, the bit of the corresponding station turns to 1 (ON). 2) When either Xn1 or XnF of the mounted CC-Link module turns OFF, the bit of the corresponding station turns to 1 (ON). 3) Turns to 1 (ON) when communication between the mounted CC-Link module and CPU module cannot be made. The above module Nos. n are in order of the head I/O numbers. (However, the one where parameter setting has not been made is not counted.)	S (Error)	New	Qn(H)*14 QnPH*14
SD290	Device assignment (Same as parameter contents)	Number of points assigned for X	• Stores the number of points currently set for X devices	S (Initial)	New	○ Rem
SD291		Number of points assigned for Y	• Stores the number of points currently set for Y devices			
SD292		Number of points assigned for M	• Stores the number of points currently set for M devices			
SD293		Number of points assigned for L	• Stores the number of points currently set for L devices			○
SD294		Number of points assigned for B	• Stores the number of points currently set for B devices			○ Rem
SD295		Number of points assigned for F	• Stores the number of points currently set for F devices			○
SD296		Number of points assigned for SB	• Stores the number of points currently set for SB devices			○ Rem
SD297	Device assignment (Same as parameter contents)	Number of points assigned for V	• Stores the number of points currently set for V devices	S (Initial)	New	○
SD298		Number of points assigned for S	• Stores the number of points currently set for S devices			
SD299		Number of points assigned for T	• Stores the number of points currently set for T device			
SD300		Number of points assigned for ST	• Stores the number of points currently set for ST devices			
SD301		Number of points assigned for C	• Stores the number of points currently set for C devices			○ Rem
SD302		Number of points assigned for D	• Stores the number of points currently set for D devices			
SD303		Number of points assigned for W	• Stores the number of points currently set for W devices			
SD304		Number of points assigned for SW	• Stores the number of points currently set for SW devices			

*14: The module whose first 5 digits of serial No. is 08032 or later.

Table App. 3.4. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD305	Device assignment (Index register)	16 bit modification Number of points assigned for Z	Stores the number of points of index register (Z) to be modified in the range of 16 bits. (The assignment is set by the ZR device index modification setting parameter.)	S (Initial)	New	QnU
SD315	Time reserved for communication processing	Time reserved for communication processing	- Reserves the designated time for communication processing with GX Developer or other units. - The greater the value is designated, the shorter the response time for communication with other devices (GX Developer, serial communication units) becomes. - If the designated value is out of the range above, it is processed that no setting is made. - Setting range: 1 to 100 ms - Note that the scan time becomes longer by the designated time.	U	New	Q00J/Q00/Q01 Qn(H) QnPH QnPRH Rem
SD340	Ethernet information	No. of modules installed	Indicates the number of mounted Ethernet module.	S (Initial)	New	QCPU Rem
SD341		I/O No.	Indicates I/O No. of mounted Ethernet module			
SD342		Network No.	Indicates network No. of mounted Ethernet module			
SD343		Group No.	Indicates group No. of mounted Ethernet module			Qn(H) QnPH QnPRH QnU Rem
SD344		Station No.	Indicates station No. of mounted Ethernet module			
SD345 to SD346		Empty	Empty (With QCPU, the Ethernet IP address of the 1st module is stored in buffer memory.)			
SD347		Empty	Empty (With QCPU, the Ethernet error code of the 1st module is read with the ERRORRD instruction.)			
SD348 to SD354	Ethernet information	Information from 2nd module	Configuration is identical to that for the first module.	S (Initial)	New	Qn(H) QnPH QnPRH QnU ^{*10} Rem
SD355 to SD361		Information from 3rd module	Configuration is identical to that for the first module.			
SD362 to SD368		Information from 4th module	Configuration is identical to that for the first module.			

*10: The Universal model QCPU except the Q02UCPU.

Table App. 3.4. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU	
SD340	Ethernet information	No. of modules installed	• Indicates the number of mounted Ethernet module.	S (Initial)	New	QnA	
SD341		Information of 1st module	I/O No.				• Indicates I/O No. of mounted Ethernet module
SD342			Network No.				• Indicates network No. of mounted Ethernet module
SD343			Group No.				• Indicates group No. of mounted Ethernet module
SD344			Station No.				• Indicates station No. of mounted Ethernet module
SD345 to SD346			IP address				• Indicates IP address of mounted Ethernet module
SD347			Error code				• Indicates error code of mounted Ethernet module
SD348 to SD354			Information from 2nd module				• Configuration is identical to that for the first module.
SD355 to SD361		Information from 3rd module	• Configuration is identical to that for the first module.				
SD362 to SD368		Information from 4th module	• Configuration is identical to that for the first module.				
SD380	Ethernet instruction reception status	Instruction reception status of 1st module	b15 to b8 b7 b6 b5 b4 b3 b2 b1 b0 0 Not used Instruction reception status of channel 1 Instruction reception status of channel 2 Instruction reception status of channel 3 Instruction reception status of channel 4 Instruction reception status of channel 5 Instruction reception status of channel 6 Instruction reception status of channel 7 Instruction reception status of channel 8 ON: Received (Channel is being used.) OFF: Not received (Channel is not used.)	S (Initial)	New	QnPRH	
SD381	Ethernet instruction reception status	Instruction reception status of 2nd module	• Configuration is identical to that for the first module.	S (Instruction execution)			
SD382		Instruction reception status of 3rd module	• Configuration is identical to that for the first module.				
SD383		Instruction reception status of 4th module	• Configuration is identical to that for the first module.				
SD392	Software version	Internal system software version	• Stores the internal system software version in ASCII code. Higher byte Lower byte Stored into lower byte Stored into higher byte For version "A", for example, "41H" is stored. Note: The internal system software version may differ from the version indicated by the version symbol printed on the case.	S (Initial)	D9060	QnA	

Table App. 3.4. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD393	Multiple CPU system information	Number of multiple CPUs	The number of CPU modules that comprise the multiple PLC system is stored. (1 to 3, Empty also included)	S (Initial)	New	Q00/Q01 ^{*9} QnU
SD394		CPU mounting information	The CPU module types of No. 1 CPU to 3 and whether the CPU modules are mounted or not are stored. b15 to b12b11 to b8b7 to b4b3 to b0 SD394 Empty (0)CPU No.3CPU No.2CPU No.1 CPU module mounted or not mounted 0: Not mounted 1: Mounted CPU module type 0: PLC CPU 1: Motion CPU 2: PC CPU			Q00/Q01 ^{*9}
SD395		Multiple CPU number	In a multiple CPU system configuration, the CPU number of the host CPU is stored. CPU No. 1: 1, CPU No. 2: 2, CPU No. 3: 3, CPU No. 4: 4	S (Initial)	New	Q00/Q01 ^{*9} Qn(H) ^{*9} QnPH QnU
SD396		No. 1 CPU operation status	The operation information of each PLC No. is stored. (The information on the number of multiple PLCs indicated in SD393 is stored.) b15 b14 to b8 b7 to b4 b3 to b0 Vacancy Classification Operation status mounted 0: Not mounted 1: Mounted 0: Normal 1: Minor fault 2: Medium fault 3: Major fault FH: Reset 0: RUN 2: STOP 3: PAUSE 4: Initial FH: Reset	S (Initial/END processing error)	New	Q00/Q01 ^{*9} QnU
SD397		No. 2 CPU operation status				
SD398		No. 3 CPU operation status				
SD399	No. 4 CPU operation statu	QnU				

*9: Function version is B or later.

(3) System clocks/counters

Table App. 3.5. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD412	1 second counter	Number of counts in 1-second units	- Following programmable controller CPU module RUN, 1 is added each second - Count repeats from 0 to 32767 to -32768 to 0	S (Status change)	D9022	○
SD414	2n second clock setting	2n second clock units	- Stores value n of 2n second clock (Default is 30) - Setting can be made between 1 and 32767	U	New	
SD415	2nms clock setting	2nms clock units	- Stores value n of 2nms clock (Default is 30) - Setting can be made between 1 and 32767	U	New	Qn(H) QnPH QnPRH QnU
SD420	Scan counter	Number of counts in each scan	- Incremented by 1 for each scan execution after the CPU module is set to RUN. (Not counted by the scan in an initial execution type program.) - Count repeats from 0 to 32767 to -32768 to 0	S (Every END processing)	New	QnA Qn(H) QnPH QnPRH QnU
			- Incremented by 1 for each scan execution after the CPU module is set to RUN. - Count repeats from 0 to 32767 to -32768 to 0	S (Every END processing)	New	Q00J/Q00/Q01
SD430	Low speed scan counter	Number of counts in each scan	- Incremented by 1 for each scan execution after the CPU module is set to RUN. - Count repeats from 0 to 32767 to -32768 to 0 - Used only for low speed execution type programs	S (Every END processing)	New	QnA Qn(H) QnPH

(4) Scan information

Table App. 3.6. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD500	Execution program No.	Program No. in execution	• Program number of program currently being executed is stored as BIN value.	S (Status change)	New	QnA Qn(H) QnPH QnPRH QnU
SD510	Low speed execution type program No.	Low speed execution type program No. in execution	• Program number of low speed excution type program No. currently being executed is stored as BIN value. • Enabled only when SM510 is ON.	S (Every END processing)	New	QnA Qn(H) QnPH
SD520	Current scan time	Current scan time (in 1 ms units)	• The current scan time is stored into SD520 and SD521. (Measurement is made in 100 μs units. (For the Universal model QCPU, in 1 μbs units.)) SD520: Stores the ms place. (Storage range: 0 to 65535) SD521: Stores the μs place. (Storage range: 0 to 900 (For the Universal model QCPU, storage range is 0 to 999)) (Example) When the current scan time is 23.6ms, the following values are stored. SD520 = 23 SD521 = 600	S (Every END processing)	D9017 format change	QnA Q00J/Q00/Q01 Qn(H) QnPH QnPRH QnU
SD521		Current scan time (in 100 μs units)		S (Every END processing)	New	
SD522	Initial scan time	Initial scan time (in 1 ms units)	• Stores the scan time of an initial execution type program into SD522 and SD523. (Measurement is made in 100 μs units. (For the Universal model QCPU, in 1 μs units.)) SD522: Stores the ms place. (Storage range: 0 to 65535) SD523: Stores the μs place. (Storage range: 0 to 900 (For the Universal model QCPU, storage range is 0 to 999))	S (First END processing)	New	QnA Qn(H) QnPH QnPRH QnU
SD523		Initial scan time (in 100 μs units)				
SD524	Minimum scan time	Minimum scan time (in 1 ms units)	• Stores the minimum value of the scan time except that of an initial execution type program into SD524 and SD525. (Measurement is made in 100 μs units. (For the Universal model QCPU, in 1 μs units.)) SD524: Stores the ms place. (Storage range: 0 to 65535) SD525: Stores the μs place. (Storage range: 0 to 900 (For the Universal model QCPU, storage range is 0 to 999))	S (Every END processing)	D9018 format change	
SD525		Minimum scan time (in 100 μs units)		S (Every END processing)	New	
SD526	Maximum scan time	Maximum scan time (in 1 ms units)	• Stores the maximum value of the scan time except that of an initial execution type program into SD526 and SD527. (Measurement is made in 100 μs units. (For the Universal model QCPU, in 1 μs units.)) SD526: Stores the ms place. (Storage range: 0 to 65535) SD527: Stores the μs place. (Storage range: 0 to 900 (For the Universal model QCPU, storage range is 0 to 999))	S (Every END processing)	D9019 format change	
SD527		Maximum scan time (in 100 μs units)			New	
SD528	Current scan time for low speed execution type programs	Current scan time (in 1 ms units)	• Stores the current scan time of a low speed execution type program into SD528 and SD529. (Measurement is made in 100 μs units.) SD528: Stores the ms place. (Storage range: 0 to 65535) SD529: Stores the μs place. (Storage range: 0 to 900)	S (Every END processing)	New	QnA Qn(H) QnPH
SD529		Current scan time (in 100 μs units)				
SD532	Minimum scan time for low speed execution type programs	Minimum scan time (in 1 ms units)	• Stores the minimum value of the scan time of a low speed execution type program into SD532 and SD533. (Measurement is made in 100 μs units.) SD532: Stores the ms place. (Storage range: 0 to 65535) SD533: Stores the μs place. (Storage range: 0 to 900)	S (Every END processing)	New	
SD533		Minimum scan time (in 100 μs units)				
SD534	Maximum scan time for low speed execution type programs	Maximum scan time (in 1 ms units)	• Stores the maximum value of the scan time except that of the first scan of a low speed execution type program into SD534 and SD535. (Measurement is made in 100 μs units.) SD534: Stores the ms place. (Storage range: 0 to 65535) SD535: Stores the μs place. (Storage range: 0 to 900)	S (Every END processing)	New	
SD535		Maximum scan time (in 100 μs units)				
SD540	END processing time	END processing time (in 1 ms units)	• Stores the time from the end of a scan execution type program to the start of the next scan into SD540 and SD541. (Measurement is made in 100 μs units.(For the Universal model QCPU, in 1 μs units.)) SD540: Stores the ms place. (Storage range: 0 to 65535) SD541: Stores the μs place. (Storage range: 0 to 900) (Storage range: 0 to 900 (For the Universal model QCPU, storage range is 0 to 999))	S (Every END processing)	New	QnA Qn(H) QnPH QnPRH QnU
SD541		END processing time (in 100 μs units)				

Table App. 3.6. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD524	Minimum scan time	Minimum scan time (in 1 ms units)	• Stores the minimum value of the scan time into SD524 and SD525. (Measurement is made in 100 μ s units.) SD524: Stores the ms place. (Storage range: 0 to 65535) SD525: Stores the μ s place. (Storage range: 0 to 900)	S (Every END processing)	New	Q00J/Q00/Q01
SD525		Minimum scan time (in 100 μ s units)				
SD526	Maximum scan time	Maximum scan time (in 1 ms units)	• Stores the maximum value of the scan time into SD526 and SD527. (Measurement is made in 100 μ s units.) SD526: Stores the ms place. (Storage range: 0 to 65535) SD527: Stores the μ s place. (Storage range: 0 to 900)	S (Every END processing)		
SD527		Maximum scan time (in 100 μ s units)				
SD540	END processing time	END processing time (in 1 ms units)	• Stores the time from when the scan program ends until the next scan starts into SD540 and SD541. (Measurement is made in 100 μ s units.) SD540: Stores the ms place. (Storage range: 0 to 65535) SD541: Stores the μ s place. (Storage range: 0 to 900)	S (Every END processing)	New	Q00J/Q00/Q01
SD541		END processing time (in 100 μ s units)				
SD542	Constant scan wait time	Constant scan wait time (in 1 ms units)	• Stores the wait time for constant scan setting into SD542 and SD543. (Measurement is made in 100 μ s units. (For the Universal model QCPU, in 1 μ s units.)) SD542: Stores the ms place. (Storage range: 0 to 65535) SD543: Stores the μ s place. (Storage range: 0 to 900 (For the Universal model QCPU, storage range is 0 to 999))	S (Every END processing)	New	○
SD543		Constant scan wait time (in 100 μ s units)				
SD544	Cumulative execution time for low speed execution type programs	Cumulative execution time for low speed execution type programs (in 1 ms units)	• Stores the cumulative execution time of a low speed execution type program into SD544 and SD545. (Measurement is made in 100 μ s units.) SD544: Stores the ms place. (Storage range: 0 to 65535) SD545: Stores the μ s place. (Storage range: 0 to 900) • Cleared to 0 after the end of one low speed scan.	S (Every END processing)	New	QnA Qn(H) QnPH
SD545		Cumulative execution time for low speed execution type programs (in 100 μ s units)				
SD546	Execution time for low speed execution type programs	Execution time for low speed execution type programs (in 1 ms units)	• Stores the execution time of a low speed execution type program during one scan into SD546 and SD547. (Measurement is made in 100 μ s units.) SD546: Stores the ms place. (Storage range: 0 to 65535) SD547: Stores the μ s place. (Storage range: 0 to 900) • Stored every scan.	S (Every END processing)	New	
SD547		Execution time for low speed execution type programs (in 100 μ s units)				
SD548	Scan execution type program execution time	Scan execution type program execution time (in 1 ms units)	• Stores the execution time of a scan execution type program during one scan into SD548 and SD549. (Measurement is made in 100 μ s units.) SD548: Stores the ms place. (Storage range: 0 to 65535) SD549: Stores the μ s place. (Storage range: 0 to 900) • Stored every scan.	S (Every END processing)	New	QnA Qn(H) QnPH QnPRH
SD549		Scan execution type program execution time (in 100 μ s units)				
SD548	Scan program execution time	Scan program execution time (in 1 ms units)	• Stores the execution time of a scan program during one scan into SD548 and SD549. (Measurement is made in 100 μ s units. (For the Universal model QCPU, in 1 μ s units.)) SD548: Stores the ms place. (Storage range: 0 to 65535) SD549: Stores the μ s place. (Storage range: 0 to 900 (For the Universal model QCPU, storage range is 0 to 999)) • Stored every scan.	S (Every END processing)	New	Q00J/Q00/Q01 QnU
SD549		Scan program execution time (in 100 μ s units)				
SD550	Service interval measurement module	Unit/module No.	• Sets I/O number for module that measures service interval.	U	New	QnA Qn(H) QnPH QnPRH
SD551	Service interval time	Module service interval (in 1 ms units)	• Stores the service interval for the module specified in SD550 into SD551 and SD552 when SM551 is turned ON. (Measurement is made in 100 μ s units.) SD551: Stores the ms place. (Storage range: 0 to 65535) SD552: Stores the μ s place. (Storage range: 0 to 900)	S (Request)	New	
SD552		Module service interval (in 100 μ s units)				

(5) Drive information

Table App. 3.7. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD600	Memory card types	Memory card types	Indicates the type of the memory card installed.	S (Initial and card removal)	New	Qn(H) QnPH QnPRH QnU
	Memory card A types	Memory card A types	Indicates the type of memory card A installed.	S (Initial and card removal)	New	QnA
SD602	Drive 1 (Memory card RAM) capacity	Drive 1 capacity	- Drive 1 capacity is stored in 1 k byte units. (Empty capacity after format is stored.)	S (Initial and card removal)	New	QnA Qn(H) QnPH QnPRH QnU
SD603	Drive 2 (Memory card ROM) capacity	Drive 2 capacity	- Drive 2 capacity is stored in 1 k byte units.*1 (Empty capacity after format is stored.)	S (Initial and card removal)	New	Qn(H) QnPH QnPRH QnU
			Drive 2 capacity is stored in 1 k byte units.	S (Initial and card removal)	New	QnA

*1: When the Q2MEM-8MBA is used, value stored in the special register SD603 differs depending on the combination of the serial number of the High Performance model QCPU and the manufacture control number of the ATA card.
For details, refer to QCPU User's Manual (Hardware Design, Maintenance and Inspection).

Table App. 3.7. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD620	Drive 3/4 types	Drive 3/4 types	• Indicates the drive 3/4 type. b15 to b8 b7 to b4 b3 to b0 0 Drive 3 (Standrd RAM) Fixed to 1 Drive 4 (Standrd ROM) Fixed to 3	S (Initial)	New	Qn(H) QnPH QnPRH QnU
			• Indicates the drive 3/4 type. b15 to b8 b7 to b4 b3 to b0 0 Drive 3 (Standard RAM) 0: Absent 1: Present Drive 4 (Standrd ROM) Fixed to "3 (FLASH ROM)"	S (Initial)	New	Q00J/Q00/Q01
	Memory card B types	Memory card B types	• Indicates memory card B type installed b15 to b8 b7 to b4 b3 to b0 0 Drive 3 (RAM) 0: Does not exist 1: SRAM Drive 4 (ROM) 0: Does not exist 2: E²PROM 3: Flash ROM	S (Initial/Card installation and removal)	New	Q2A(S1) Q3A Q4A Q4AR
SD622	Drive 3 (Standard RAM) capacity	Drive 3 capacity	• Drive 3 capacity is stored in 1 k byte units. (Empty capacity after format is stored.)	S (Initial)	New	Qn(H) QnPH QnPRH QnU
				S (Initial/Card installation and removal)	New	Q2A(S1) Q3A Q4A Q4AR
SD623	Drive 4 (Standard ROM) capacity	Drive 4 capacity	• Drive 4 capacity is stored in 1 k byte units. (Empty capacity after format is stored.)	S (Initial)	New	Qn(H) QnPH QnPRH QnU
				S (Initial/Card installation and removal)	New	Q2A(S1) Q3A Q4A Q4AR

Table App. 3.7. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU		
SD624	Drive 3/4 use conditions	Drive 3/4 use conditions	• The conditions for usage for drive 3/4 are stored as bit patterns. (In use when ON) • The significance of these bit patterns is indicated below: <table><tr><td>b0 : Boot operation (QBT) b1 : Parameters (QPA) b2 : Device comments (QCD) b3 : Device initial value (QDI) b4 : File R (QDR) b5 : Sampling trace (QTD) b6 : Not used b7 : Not used</td><td>b8 : Not used b9 : CPU fault history (QFD) b10 : SFC trace (QTS) b11 : Local device (QDL) b12 : Not used b13 : Not used b14 : Not used b15 : Not used</td></tr></table>	b0 : Boot operation (QBT) b1 : Parameters (QPA) b2 : Device comments (QCD) b3 : Device initial value (QDI) b4 : File R (QDR) b5 : Sampling trace (QTD) b6 : Not used b7 : Not used	b8 : Not used b9 : CPU fault history (QFD) b10 : SFC trace (QTS) b11 : Local device (QDL) b12 : Not used b13 : Not used b14 : Not used b15 : Not used	S (Status change)	New	Qn(H) QnPH QnPRH
	b0 : Boot operation (QBT) b1 : Parameters (QPA) b2 : Device comments (QCD) b3 : Device initial value (QDI) b4 : File R (QDR) b5 : Sampling trace (QTD) b6 : Not used b7 : Not used	b8 : Not used b9 : CPU fault history (QFD) b10 : SFC trace (QTS) b11 : Local device (QDL) b12 : Not used b13 : Not used b14 : Not used b15 : Not used						
	Memory card B use conditions	Memory card B use conditions	• The use conditions for memory card B are stored as bit patterns. (In use when ON) • The significance of these bit patterns is indicated below: <table><tr><td>b0 : Boot operation (QBT) b1 : Parameters (QPA) b2 : Device comments (QCD) b3 : Device initial value (QDI) b4 : File R (QDR) b5 : Sampling trace (QTD) b6 : Status latch (QTL) b7 : Program trace (QTP)</td><td>b8 : Simulation data (QDS) b9 : CPU fault history (QFD) b10 : SFC trace (QTS) b11 : Local device (QDL) b12 : Local device (QDL) b13 : Not used b14 : Not used b15 : Not used</td></tr></table>	b0 : Boot operation (QBT) b1 : Parameters (QPA) b2 : Device comments (QCD) b3 : Device initial value (QDI) b4 : File R (QDR) b5 : Sampling trace (QTD) b6 : Status latch (QTL) b7 : Program trace (QTP)	b8 : Simulation data (QDS) b9 : CPU fault history (QFD) b10 : SFC trace (QTS) b11 : Local device (QDL) b12 : Local device (QDL) b13 : Not used b14 : Not used b15 : Not used	S (Status change)	New	Q2A(S1) Q3A Q4A Q4AR
b0 : Boot operation (QBT) b1 : Parameters (QPA) b2 : Device comments (QCD) b3 : Device initial value (QDI) b4 : File R (QDR) b5 : Sampling trace (QTD) b6 : Status latch (QTL) b7 : Program trace (QTP)	b8 : Simulation data (QDS) b9 : CPU fault history (QFD) b10 : SFC trace (QTS) b11 : Local device (QDL) b12 : Local device (QDL) b13 : Not used b14 : Not used b15 : Not used							
Drive 3/4 use conditions	Drive 3/4 use conditions	• The conditions for usage for drive 3/4 are stored as bit patterns. (In use when ON) • The significance of these bit patterns is indicated below: <table><tr><td>b0 : Not used b1 : Parameters (QPA) b2 : Device comments (QCD) b3 : Device initial value (QDI)*1 b4 : File register R (QDR) b5 : Sampling trace (QTD) b6 : Not used b7 : Not used</td><td>b8 : Not used b9 : Not used b10 : Not used b11 : Local device (QDL) b12 : Not used b13 : Not used b14 : Not used b15 : Not used</td></tr></table> *1: Turned ON at boot start and OFF at boot completion.	b0 : Not used b1 : Parameters (QPA) b2 : Device comments (QCD) b3 : Device initial value (QDI)*1 b4 : File register R (QDR) b5 : Sampling trace (QTD) b6 : Not used b7 : Not used	b8 : Not used b9 : Not used b10 : Not used b11 : Local device (QDL) b12 : Not used b13 : Not used b14 : Not used b15 : Not used	S (Status change)	New	QnU	
b0 : Not used b1 : Parameters (QPA) b2 : Device comments (QCD) b3 : Device initial value (QDI)*1 b4 : File register R (QDR) b5 : Sampling trace (QTD) b6 : Not used b7 : Not used	b8 : Not used b9 : Not used b10 : Not used b11 : Local device (QDL) b12 : Not used b13 : Not used b14 : Not used b15 : Not used							
SD622	Drive 3 (Standard RAM) capacity	Drive 3 capacity	• Drive 3 capacity is stored in 1k byte units.	S (Initial)	New	Q00J/Q00/Q01		
SD623	Drive 4 (Standard ROM) capacity	Drive 4 capacity	• Drive 4 capacity is stored in 1k byte units.	S (Initial)				
SD624	Drive 3 use conditions	Drive 3 use conditions	• Drive 3 use conditions are stored in bit pattern. b15to b5b4to b0 000000 File register (R) 0: Not used 1: In use	S (Status change)				
SD640	File register drive	Drive number:	• Stores drive number being used by file register	S (Status change) *10	New	○		

*10: On the Basic model QCPU, data is set at STOP to RUN or RSET instruction execution after parameter execution.

Table App. 3.7. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU																		
SD641	File register file name	File register file name	Stores file register file name (with extension) selected at parameters or by use of QDRSET instruction as ASCII code. b15to b8b7to b0 <table><tr><td>SD641</td><td>2nd character</td><td>1st character</td></tr><tr><td>SD642</td><td>4th character</td><td>3rd character</td></tr><tr><td>SD643</td><td>6th character</td><td>5th character</td></tr><tr><td>SD644</td><td>8th character</td><td>7th character</td></tr><tr><td>SD645</td><td>1st character of extension</td><td>2EH(.)</td></tr><tr><td>SD646</td><td>3rd character of the extension</td><td>2nd character of the extension</td></tr></table>	SD641	2nd character	1st character	SD642	4th character	3rd character	SD643	6th character	5th character	SD644	8th character	7th character	SD645	1st character of extension	2EH(.)	SD646	3rd character of the extension	2nd character of the extension	S (Status change)	New	QnA Qn(H) QnPH QnPRH QnU
SD641				2nd character	1st character																			
SD642				4th character	3rd character																			
SD643				6th character	5th character																			
SD644				8th character	7th character																			
SD645				1st character of extension	2EH(.)																			
SD646				3rd character of the extension	2nd character of the extension																			
SD642																								
SD643																								
SD644																								
SD645																								
SD646																								
SD646	Stores file register file name (MAIN.QDR) selected at parameters as ASCII code. b15to b8b7to b0 <table><tr><td>SD641</td><td>2nd character (A)</td><td>1st character (M)</td></tr><tr><td>SD642</td><td>4th character (N)</td><td>3rd character (I)</td></tr><tr><td>SD643</td><td>6th character ()</td><td>5th character ()</td></tr><tr><td>SD644</td><td>8th character ()</td><td>7th character ()</td></tr><tr><td>SD645</td><td>1st character of the extension (Q)</td><td>2EH(.)</td></tr><tr><td>SD646</td><td>3rd character of the extension (R)</td><td>2nd character of the extension (D)</td></tr></table>	SD641	2nd character (A)	1st character (M)	SD642	4th character (N)	3rd character (I)	SD643	6th character ()	5th character ()	SD644	8th character ()	7th character ()	SD645	1st character of the extension (Q)	2EH(.)	SD646	3rd character of the extension (R)	2nd character of the extension (D)	S (Initial)	New	Q00J/Q00/Q01		
SD641	2nd character (A)	1st character (M)																						
SD642	4th character (N)	3rd character (I)																						
SD643	6th character ()	5th character ()																						
SD644	8th character ()	7th character ()																						
SD645	1st character of the extension (Q)	2EH(.)																						
SD646	3rd character of the extension (R)	2nd character of the extension (D)																						
SD647	File register capacity	File register capacity	Stores the data capacity of the currently selected file register in 1 k word units.	S (Status change)	New	QnA Qn(H) QnPH QnPRH QnU																		
				S (Initial)		Q00J/Q00/Q01																		
SD648	File register block number	File register block number	Stores the currently selected file register block number.	S (Status change) *10	D9035	○																		
SD650	Comment drive	Comment drive number	Stores the comment drive number selected at the parameters or by the QCDSET instruction.	S (Status change)	New	QnA Qn(H) QnPH QnPRH QnU																		
SD651	Comment file name	Comment file name	Stores the comment file name (with extension) selected at the parameters or by the QCDSET instruction in ASCII code. b15to b8b7to b0 <table><tr><td>SD651</td><td>2nd character</td><td>1st character</td></tr><tr><td>SD652</td><td>4th character</td><td>3rd character</td></tr><tr><td>SD653</td><td>6th character</td><td>5th character</td></tr><tr><td>SD654</td><td>8th character</td><td>7th character</td></tr><tr><td>SD655</td><td>1st character of the extension</td><td>2EH(.)</td></tr><tr><td>SD656</td><td>3rd character of the extension</td><td>2nd character of the extension</td></tr></table>	SD651	2nd character		1st character	SD652	4th character	3rd character	SD653	6th character	5th character	SD654	8th character	7th character	SD655	1st character of the extension	2EH(.)	SD656	3rd character of the extension	2nd character of the extension	S (Status change)	New
SD651				2nd character	1st character																			
SD652				4th character	3rd character																			
SD653				6th character	5th character																			
SD654				8th character	7th character																			
SD655				1st character of the extension	2EH(.)																			
SD656	3rd character of the extension	2nd character of the extension																						
SD652																								
SD653																								
SD654																								
SD655																								
SD656																								
SD660	Boot operation designation file	Boot designation file drive number	Stores the drive number where the boot designation file (*.QBT) is being stored.	S (Initial)	New	QnA Qn(H) QnPH QnPRH QnU																		
SD661		File name of boot designation file	Stores the file name of the boot designation file (*.QBT). b15to b8b7to b0 <table><tr><td>SD661</td><td>2nd character</td><td>1st character</td></tr><tr><td>SD662</td><td>4th character</td><td>3rd character</td></tr><tr><td>SD663</td><td>6th character</td><td>5th character</td></tr><tr><td>SD664</td><td>8th character</td><td>7th character</td></tr><tr><td>SD665</td><td>1st character of the extension</td><td>2EH(.)</td></tr><tr><td>SD666</td><td>3rd character of the extension</td><td>2nd character of the extension</td></tr></table>	SD661	2nd character		1st character	SD662	4th character	3rd character	SD663	6th character	5th character	SD664	8th character	7th character	SD665	1st character of the extension	2EH(.)	SD666	3rd character of the extension	2nd character of the extension	S (Initial)	New
SD661				2nd character	1st character																			
SD662				4th character	3rd character																			
SD663				6th character	5th character																			
SD664				8th character	7th character																			
SD665				1st character of the extension	2EH(.)																			
SD666	3rd character of the extension	2nd character of the extension																						
SD662																								
SD663																								
SD664																								
SD665																								
SD666																								

*10: On the Basic model QCPU, data is set at STOP to RUN or RSET instruction execution after parameter execution.

Table App. 3.7. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU																					
SD670	Parameter enable drive information	Parameter enable drive No.	Stores information of parameter storage destination drive which is enabled. 0: Drive 0 (Program memory) 1: Drive 1 (SRAM card) 2: Drive 2 (Flash card/ATA card) 4: Drive 4 (Standard ROM)	S (Initial)	New	QnU																					
SD671	Status of latch data backup function	Status display	Indicates the status of the latch data backup function. <table><thead><tr><th colspan="2">Status</th><th>Presence/ absence of backup data</th><th>Restore operation at turning power supply ON from OFF</th></tr></thead><tbody><tr><td>0</td><td>No backup data</td><td>Absent</td><td>Restoring not executed</td></tr><tr><td>1</td><td>Restore ready completion</td><td rowspan="4">Present</td><td>Restoring executed when turning power supply ON from OFF the following time</td></tr><tr><td>2</td><td>Restore execution completion</td><td>Restoring not executed</td></tr><tr><td>3</td><td>Backup execution wait</td><td>Restoring not executed</td></tr><tr><td>4</td><td>Restore repeated execution ready completion</td><td>Restoring executed when turning power supply ON from OFF</td></tr></tbody></table> "2 Restore ready completion" is a status immediately after restoring data. "3 Backup execution wait" is a status after turning power supply ON from OFF at "2 Restore ready completion".	Status		Presence/ absence of backup data	Restore operation at turning power supply ON from OFF	0	No backup data	Absent	Restoring not executed	1	Restore ready completion	Present	Restoring executed when turning power supply ON from OFF the following time	2	Restore execution completion	Restoring not executed	3	Backup execution wait	Restoring not executed	4	Restore repeated execution ready completion	Restoring executed when turning power supply ON from OFF	S (Status change)	New	QnU
Status		Presence/ absence of backup data	Restore operation at turning power supply ON from OFF																								
0	No backup data	Absent	Restoring not executed																								
1	Restore ready completion	Present	Restoring executed when turning power supply ON from OFF the following time																								
2	Restore execution completion		Restoring not executed																								
3	Backup execution wait		Restoring not executed																								
4	Restore repeated execution ready completion		Restoring executed when turning power supply ON from OFF																								
SD672	Backup information	Backup time (Year and month)	Stores the last 2 digits of year and month when backup is performed in 2-digit BCD code. b15 to b12b11 to b8b7 to b4b3 to b0 YearMonth Example: July, 1993 9307_H <td rowspan="4">S (At write)</td> <td rowspan="4">New</td> <td rowspan="4">QnU</td>	S (At write)	New	QnU																					
Backup time (Day and hour)		Stores the day and hour when backup is performed in 2-digit BCD code. b15 to b12b11 to b8b7 to b4b3 to b0 DayHour Example: 31st, 10 a.m. 3110_H																									
Backup time (Minute and second)		Stores the minute and second when backup is performed in 2-digit BCD code. b15 to b12b11 to b8b7 to b4b3 to b0 MinuteSecond Example: 35 min., 48 sec. 3548_H																									
Backup time (Year and day of week)		Stores the first 2 digits of year and day of week when backup is performed in BCD code. b15 to b12b11 to b8b7 to b4b3 to b0 Higher digits of year (0 to 99) Example: 1993, Friday 1905_H Day of the week <table><tr><td>0</td><td>Sunday</td></tr><tr><td>1</td><td>Monday</td></tr><tr><td>2</td><td>Tuesday</td></tr><tr><td>3</td><td>Wednesday</td></tr><tr><td>4</td><td>Thursday</td></tr><tr><td>5</td><td>Friday</td></tr><tr><td>6</td><td>Saturday</td></tr></table>	0				Sunday	1	Monday	2	Tuesday	3	Wednesday	4	Thursday	5	Friday	6	Saturday								
0	Sunday																										
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3	Wednesday																										
4	Thursday																										
5	Friday																										
6	Saturday																										

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU																
SD676	Backup data restore information	Restore time (Year and month)	Stores the last 2 digits of year and month when data is restored in 2-digit BCD code. b15 to b12b11 to b8b7 to b4b3 to b0 <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> Example: July, 1993 9307H Year Month													S (Initial)	New	QnU				
SD677		Restore time (Day and time)	Stores the day and time when data is restored in 2-digit BCD code. b15 to b12b11 to b8b7 to b4b3 to b0 <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> Example: 31st, 10 a.m. 3110H Day Hour																			
SD678	Restore time (Minute and second)	Stores the minute and second when data is restored in 2-digit BCD code. b15 to b12b11 to b8b7 to b4b3 to b0 <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> Example: 35 min., 48 sec. 3548H Minute Second																				
SD679	Restore time (Year and day of week)	Stores the first 2 digits of year and day of week when data is restored in BCD code. b15 to b12b11 to b8b7 to b4b3 to b0 <table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> Example: 1993, Friday 1905H Higher digits of year (0 to 99) <table><tr><th>Day of the week</th></tr><tr><td>0 Sunday</td></tr><tr><td>1 Monday</td></tr><tr><td>2 Tuesday</td></tr><tr><td>3 Wednesday</td></tr><tr><td>4 Thursday</td></tr><tr><td>5 Friday</td></tr><tr><td>6 Saturday</td></tr></table>													Day of the week	0 Sunday	1 Monday	2 Tuesday	3 Wednesday	4 Thursday	5 Friday	6 Saturday
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0 Sunday																						
1 Monday																						
2 Tuesday																						
3 Wednesday																						
4 Thursday																						
5 Friday																						
6 Saturday																						
SD681	Program memory write (transfer) status	Write (transfer) status display (percentage)	Displays the status of writing (transferring) the program memory (flash ROM) in percentage. (0 to 100%) "0" is set when the write direction is set.	S (At write)	New	QnU																
SD682	Program memory write count index	Write count index up to present	- Stores the index value for the number of write operations to the program memory (flash ROM) up to the present in BIN 32-bit value. - When the index value exceeds 100 thousand times, "FLASH ROM ERROR" (error code: 1610) occurs. (The index value is calculated even when exceeding 100 thousand times.) Note) The write count does not equal to the index value.(Since a flash ROM write life is prolonged by the system, 1 is added to the write count index when writing is performed twice or so.).	S (At write)	New	QnU																
SD683																						
SD686	Standard ROM write (transfer) status	Write (transfer) status display (percentage)	Displays the status of writing (transferring) the standard ROM (flash ROM) in percentage. (0 to 100%) "0" is set when the write direction is set.	S (At write)	New	QnU																
SD687	Standard ROM write count index	Write count index up to present	- Stores the index value for the number of write operations to the standard ROM (flash ROM) up to the present in BIN 32-bit value. - When the index value exceeds 100 thousand times, "FLASH ROM ERROR" (error code: 1610) occurs. (The index value is calculated even when exceeding 100 thousand times.) Note) The write count does not equal to the index value. (Since a flash ROM write life is prolonged by the system, 1 is added to the write count index when the total write capacity after the previous count up reaches about 1M byte.)	S (At write)	New	QnU																
SD688																						
SD695	Specification of writing to standard ROM instruction count	Specification of writing to standard ROM instruction count	- Specifies the maximum number of executing the instruction (SP.DEVST) to write to the standard ROM per day. - When the number of execution of writing to the standard ROM instruction exceeds the number of times set by SD695, [OPERATION ERROR] (error code: 4113) occurs. - The setting range for SD695 is 0 to 32767. If 0 or value outside the range is set, [OPERATION ERROR] (error code: 4113) occurs when executing the writing to standard ROM instruction.	U	New	QnU																

(6) Instruction-Related Registers

Table App. 3.8. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD705	Mask pattern	Mask pattern	• During block operations, turning SM705 ON makes it possible to use the mask pattern being stored at SD705 (or at SD705 and SD706 if double words are being used) to operate on all data in the block with the masked values.	U	New	Q00.J/Q00/Q01 Qn(H) QnPH QnPRH QnA
SD706						
SD714	Number of empty communication request registration areas	0 to 32	• Stores the number of empty blocks in the communications request area for remote terminal modules connected to the MELSECNET/MINI-S3.	S (During execution)	D9081	QnA
SD715	IMASK instruction mask pattern	Mask pattern	• Patterns masked by use of the IMASK instruction are stored in the following manner: SD715 b15 I15 to I1 b1 I0 SD716 I31 to I17 I16 SD717 I47 to I33 I32	S (During execution)	New	O
SD716						
SD717						
SD718	Accumulator	Accumulator	• For use as replacement for accumulators used in A series programs.	S/U	New	
SD719						
SD720	Program No. designation for PLOADP instruction	Program No. designation for PLOADP instruction	Stores the program number of the program to be loaded by the PLOADP instruction when designated. Designation range: 1 to 124	U	New	Qn(H) QnPH
SD730	No. of empty areas for CC-Link communication request register area	0 to 32	• Stores the number of empty registration area for the request for communication with the intelligent device station connected to A(1S)J61QBT61.	S (During execution)	New	QnA
SD736	PKEY input	PKEY input	• Special register that temporarily stores keyboard data input by means of the PKEY instruction.	S (During execution)	New	

Table App. 3.8. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU																																																																																																																																																																																																																																							
SD738	Message storage	Message storage	• Stores the message designated by the MSG instruction. <table><thead><tr><th></th><th>b15</th><th>to</th><th>b8</th><th>b7</th><th>to</th><th>b0</th></tr></thead><tbody><tr><td>SD738</td><td colspan="2">2nd character</td><td colspan="4">1st character</td></tr><tr><td>SD739</td><td colspan="2">4th character</td><td colspan="4">3rd character</td></tr><tr><td>SD740</td><td colspan="2">6th character</td><td colspan="4">5th character</td></tr><tr><td>SD741</td><td colspan="2">8th character</td><td colspan="4">7th character</td></tr><tr><td>SD742</td><td colspan="2">10th character</td><td colspan="4">9th character</td></tr><tr><td>SD743</td><td colspan="2">12th character</td><td colspan="4">11th character</td></tr><tr><td>SD744</td><td colspan="2">14th character</td><td colspan="4">13th character</td></tr><tr><td>SD745</td><td colspan="2">16th character</td><td colspan="4">15th character</td></tr><tr><td>SD746</td><td colspan="2">18th character</td><td colspan="4">17th character</td></tr><tr><td>SD747</td><td colspan="2">20th character</td><td colspan="4">19th character</td></tr><tr><td>SD748</td><td colspan="2">22nd character</td><td colspan="4">21st character</td></tr><tr><td>SD749</td><td colspan="2">24th character</td><td colspan="4">23rd character</td></tr><tr><td>SD750</td><td colspan="2">26th character</td><td colspan="4">25th character</td></tr><tr><td>SD751</td><td colspan="2">28th character</td><td colspan="4">27th character</td></tr><tr><td>SD752</td><td colspan="2">30th character</td><td colspan="4">29th character</td></tr><tr><td>SD753</td><td colspan="2">32nd character</td><td colspan="4">31st character</td></tr><tr><td>SD754</td><td colspan="2">34th character</td><td colspan="4">33rd character</td></tr><tr><td>SD755</td><td colspan="2">36th character</td><td colspan="4">35th character</td></tr><tr><td>SD756</td><td colspan="2">38th character</td><td colspan="4">37th character</td></tr><tr><td>SD757</td><td colspan="2">40th character</td><td colspan="4">39th character</td></tr><tr><td>SD758</td><td colspan="2">42nd character</td><td colspan="4">41st character</td></tr><tr><td>SD759</td><td colspan="2">44th character</td><td colspan="4">43rd character</td></tr><tr><td>SD760</td><td colspan="2">46th character</td><td colspan="4">45th character</td></tr><tr><td>SD761</td><td colspan="2">48th character</td><td colspan="4">47th character</td></tr><tr><td>SD762</td><td colspan="2">50th character</td><td colspan="4">49th character</td></tr><tr><td>SD763</td><td colspan="2">52nd character</td><td colspan="4">51st character</td></tr><tr><td>SD764</td><td colspan="2">54th character</td><td colspan="4">53rd character</td></tr><tr><td>SD765</td><td colspan="2">56th character</td><td colspan="4">55th character</td></tr><tr><td>SD766</td><td colspan="2">58th character</td><td colspan="4">57th character</td></tr><tr><td>SD767</td><td colspan="2">60th character</td><td colspan="4">59th character</td></tr><tr><td>SD768</td><td colspan="2">62nd character</td><td colspan="4">61st character</td></tr><tr><td>SD769</td><td colspan="2">64th character</td><td colspan="4">63rd character</td></tr></tbody></table>		b15	to	b8	b7	to	b0	SD738	2nd character		1st character				SD739	4th character		3rd character				SD740	6th character		5th character				SD741	8th character		7th character				SD742	10th character		9th character				SD743	12th character		11th character				SD744	14th character		13th character				SD745	16th character		15th character				SD746	18th character		17th character				SD747	20th character		19th character				SD748	22nd character		21st character				SD749	24th character		23rd character				SD750	26th character		25th character				SD751	28th character		27th character				SD752	30th character		29th character				SD753	32nd character		31st character				SD754	34th character		33rd character				SD755	36th character		35th character				SD756	38th character		37th character				SD757	40th character		39th character				SD758	42nd character		41st character				SD759	44th character		43rd character				SD760	46th character		45th character				SD761	48th character		47th character				SD762	50th character		49th character				SD763	52nd character		51st character				SD764	54th character		53rd character				SD765	56th character		55th character				SD766	58th character		57th character				SD767	60th character		59th character				SD768	62nd character		61st character				SD769	64th character		63rd character				S (During execution)	New	QnA
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SD774 to SD775	PID limit setting (for complete derivative)	0: With limit 1: Without limit	• Specify the limit of each PID loop as shown below. <table><thead><tr><th></th><th>b15</th><th>to</th><th>b1</th><th>b0</th></tr></thead><tbody><tr><td>SD774</td><td>Loop16</td><td>to</td><td>Loop2</td><td>Loop1</td></tr><tr><td>SD775</td><td>Loop32</td><td>to</td><td>Loop18</td><td>Loop17</td></tr></tbody></table>		b15	to	b1	b0	SD774	Loop16	to	Loop2	Loop1	SD775	Loop32	to	Loop18	Loop17	U	New	Qn(H) QnPRH QnU																																																																																																																																																																																																																								
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*9: Function version is B or later.

Table App. 3.8. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD778	Refresh processing selection when the COM instruction is executed	b0 to b14: 0: Do not refresh 1: Refresh b15 bit 0: Communication with CPU module is executed 1: Communication with CPU module is nonexecuted	- Selects whether or not the data is refreshed when the COM instruction is executed. - Designation of SD778 is made valid when SM775 turns ON. SD778	U	New	Q00J/Q00/Q01 ^{*9} Qn(H) ^{*11} QnPH ^{*12} QnPRH
			- Refresh between multiple CPUs by COM instruction is performed under the following occasion. Receiving operation from other device: b4 of SD778(refresh in the CPU shared memory) is turned to 1. Sending operation from host CPU : b15 of SD778(communication with peripheral device is executed/nonexecuted) is turned to 0. - Selects whether or not the data is refreshed when the COM instruction is executed. - Designation of SD778 is made valid when SM775 turns ON. SD778	U	New	Qn(H) ^{*13}

*9: Function version is B or later.

*11: The module whose first 5 digits of serial No. is 04012 or later.

*12: The module whose first 5 digits of serial No. is 07032 or later.

*13: The module whose first 5 digits of serial No. is 09012 or later.

Table App. 3.8. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD778	Refresh processing selection when the COM instruction is executed	b0 to b14: 0: Do not refresh 1: Refresh b15 bit 0: communication with peripheral device is executed 1: communication with peripheral device is nonexecuted	- Selects whether or not the data is refreshed when the COM instruction is executed. - Designation of SD778 is made valid when SM775 turns ON.	U	New	QnU
SD780	Remaining No. of simultaneous execution of CC-Link dedicated instruction	0 to 32	Stores the remaining number of simultaneous execution of the CC-Link dedicated instructions.	U	New	QnA
SD781 to SD793	Mask pattern of IMASK instruction	Mask pattern	Stores the mask patterns masked by the IMASK instruction as follows:	S (During execution)	New	Qn(H) QnPH QnPRH QnU
SD781 to SD785	Mask pattern of IMASK instruction	Mask pattern	Stores the mask patterns masked by the IMASK instruction as follows:	S (During execution)	New	Q00J/Q00/Q01
SD794 to SD795	PID limit setting (for incomplete derivative)	0: With limit 1: Without limit	Specify the limit of each PID loop as shown below.	U	New	Qn(H)*13 QnPRH QnU
SD794	PID limit setting (for incomplete derivative)	0: With limit 1: Without limit	Specify the limit of each PID loop as shown below.	U	New	Q00J/Q00/Q01*9

*9: Function version is B or later.

*13: The module whose first 5 digits of serial No. is 09012 or later.

Table App. 3.8. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD796	Maximum number of blocks used for dedicated instruction of Multiple CPU high speed bus setting (for CPU No.1)	Maximum number of blocks used for dedicated instruction range 1 to 9 (Default: 2) *When value other than 1 to 9 is set, operation is performed as if 9 is set.	Specifies the maximum number of blocks used for the dedicated instruction of Multiple CPU high speed bus (target CPU=CPU No.1). When the dedicated instruction of Multiple CPU transmission is executed to the CPU No.1, and the number of empty blocks of the dedicated instruction transmission area is less than the setting value of this register, SM796 is turned ON, which is used as the interlock signal for consecutive execution of the dedicated instruction of Multiple CPU transmission.	U (At 1 scan after RUN)	New	QnU
SD797	Maximum number of blocks used for dedicated instruction of Multiple CPU high speed bus setting (for CPU No.2)	Maximum number of blocks used for dedicated instruction range 1 to 9 (Default: 2) *When value other than 1 to 9 is set, operation is performed as if 9 is set.	Specifies the maximum number of blocks used for the dedicated instruction of Multiple CPU high speed bus (target CPU=CPU No.2). When the dedicated instruction of Multiple CPU transmission is executed to the CPU No.2, and the number of empty blocks of the dedicated instruction transmission area is less than the setting value of this register, SM797 is turned ON, which is used as the interlock signal for consecutive execution of the dedicated instruction of Multiple CPU transmission.	U (At 1 scan after RUN)	New	QnU
SD798	Maximum number of blocks used for dedicated instruction of Multiple CPU high speed bus setting (for CPU No.3)	Maximum number of blocks used for dedicated instruction range 1 to 9 (Default: 2) *When value other than 1 to 9 is set, operation is performed as if 9 is set.	Specifies the maximum number of blocks used for the dedicated instruction of Multiple CPU high speed bus (target CPU=CPU No.3). When the dedicated instruction of Multiple CPU transmission is executed to the CPU No.3, and the number of empty blocks of the dedicated instruction transmission area is less than the setting value of this register, SM798 is turned ON, which is used as the interlock signal for consecutive execution of the dedicated instruction of Multiple CPU transmission.	U (At 1 scan after RUN)	New	QnU
SD799	Maximum number of blocks used for dedicated instruction of Multiple CPU high speed bus setting (for CPU No.4)	Maximum number of blocks used for dedicated instruction range 1 to 9 (Default: 2) *When value other than 1 to 9 is set, operation is performed as if 9 is set.	Specifies the maximum number of blocks used for the dedicated instruction of Multiple CPU high speed bus (target CPU=CPU No.4). When the dedicated instruction of Multiple CPU transmission is executed to the CPU No.4, and the number of empty blocks of the dedicated instruction transmission area is less than the setting value of this register, SM799 is turned ON, which is used as the interlock signal for consecutive execution of the dedicated instruction of Multiple CPU transmission.	U (At 1 scan after RUN)	New	QnU ^{*14}

*14: The Universal model QCPU except the Q02UCPU.

(7) Debug

Table App. 3.9. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU																												
SD806	Status latch file name	Status latch file name	Stores file name (with extension) from point in time when status latch was conducted as ASCII code. <table><tr><td></td><td>b15 to b8</td><td>b7 to b0</td></tr><tr><td>SD806</td><td>2nd character</td><td>1st character</td></tr><tr><td>SD807</td><td>4th character</td><td>3rd character</td></tr><tr><td>SD808</td><td>6th character</td><td>5th character</td></tr><tr><td>SD809</td><td>8th character</td><td>7th character</td></tr><tr><td>SD810</td><td>1st character of the extension</td><td>2EH(.)</td></tr><tr><td>SD811</td><td>3rd character of the extension</td><td>2nd character of the extension</td></tr></table>		b15 to b8	b7 to b0	SD806	2nd character	1st character	SD807	4th character	3rd character	SD808	6th character	5th character	SD809	8th character	7th character	SD810	1st character of the extension	2EH(.)	SD811	3rd character of the extension	2nd character of the extension	S (During execution)	New								
				b15 to b8	b7 to b0																													
SD806				2nd character	1st character																													
SD807				4th character	3rd character																													
SD808				6th character	5th character																													
SD809				8th character	7th character																													
SD810	1st character of the extension	2EH(.)																																
SD811	3rd character of the extension	2nd character of the extension																																
SD807																																		
SD808																																		
SD809																																		
SD810																																		
SD811																																		
SD812	Status latch step	Status latch step	Stores step number from point in time when status latch was conducted. <table><tr><td>SD812</td><td>Pattern*</td></tr><tr><td>SD813</td><td>Block No.</td></tr><tr><td>SD814</td><td>Step No./transition condition No.</td></tr><tr><td>SD815</td><td>Sequence step No. (L)</td></tr><tr><td>SD816</td><td>Sequence step No. (H)</td></tr></table> *: Contents of pattern data <table><tr><td>15</td><td>14</td><td>to</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>← (Bit number)</td></tr><tr><td>0</td><td>0</td><td>to</td><td>0</td><td>0</td><td>*</td><td>*</td><td>*</td><td></td></tr></table> (Not used) SFC block designation present (1)/absent (0) SFC step designation present (1)/absent (0) SFC transition designation present (1)/absent (0)	SD812	Pattern*	SD813	Block No.	SD814	Step No./transition condition No.	SD815	Sequence step No. (L)	SD816	Sequence step No. (H)	15	14	to	4	3	2	1	0	← (Bit number)	0	0	to	0	0	*	*	*		S (During execution)	D9055 format change	QnA
SD812				Pattern*																														
SD813				Block No.																														
SD814				Step No./transition condition No.																														
SD815				Sequence step No. (L)																														
SD816				Sequence step No. (H)																														
15	14	to	4	3	2	1	0	← (Bit number)																										
0	0	to	0	0	*	*	*																											
SD813																																		
SD814																																		
SD815																																		
SD816																																		

(8) Latch area

Table App. 3.10. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD900	Drive where power was interrupted	Access file drive number during power loss	• Stores drive number if file was being accessed during power loss.	S (Status change)	New	QnA
SD901	File name active during power loss	Access file name during power loss	• Stores file name (with extension) in ASCII code if file was being accessed during power loss. b15 to b8 b7 to b0 SD901 2nd character 1st character SD902 4th character 3rd character SD903 6th character 5th character SD904 8th character 7th character SD905 1st character of the extension 2EH(.) SD906 3rd character of the extension 2nd character of the extension	S (Status change)	New	
SD902						
SD903						
SD904						
SD905						
SD906						
SD910	RKEY input	RKEY input	• Stored in sequence that PU key code was entered. b15 to b8 b7 to b0 SD910 2nd character 1st character SD911 4th character 3rd character SD912 6th character 5th character SD913 8th character 7th character SD914 10th character 9th character SD915 12th character 11th character SD916 14th character 13th character SD917 16th character 15th character SD918 18th character 17th character SD919 20th character 19th character SD920 22nd character 21st character SD921 24th character 23rd character SD922 26th character 25th character SD923 28th character 27th character SD924 30th character 29th character SD925 32nd character 31st character	S (During execution)	New	
SD911						
SD912						
SD913						
SD914						
SD915						
SD916						
SD917						
SD918						
SD919						
SD920						
SD921						
SD922						
SD923						
SD924						
SD925						

(9) Redundant CPU information (host system CPU information*1)

Table App. 3.11. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD952	History of memory copy from control system to standby system	Latest status of memory copy from control system to standby system	Stores the completion status of the memory copy from control system to standby system executed last. 1) Stores the same value as stored into SD1596 at normal completion/ abnormal completion of the memory copy from control system to standby system. 2) Backed up for a power failure, this special register holds the status of memory copy from control system to standby system executed last. 3) Cleared to 0 by latch clear operation.	S (Status change)	New	QnPRH

*1: The host system CPU information is stored.

(10)A to Q/QnA conversion

ACPU special registers D9000 to D9255 correspond to Q/QnA special registers SD1000 to SD1255 after A to Q/QnA conversion.

(However, the Basic model QCPU, Redundant CPU, and Universal model QCPU do not support the A to Q/QnA conversion.)

These special registers are all set by the system, and cannot be set by the user program.

To set data by the user program, correct the program for use of the Q/QnACPU special registers.

However, some of SD1200 to SD1255 (corresponding to D9200 to 9255 before conversion) can be set by the user program if they could be set by the user program before conversion.

For details on the ACPUs special registers, refer to the user's manual for the corresponding CPU, and MELSECNET or MELSECNET/B Data Link System Reference Manuals.

REMARK

Supplemental explanation on "Special Register for Modification" column

- ① For the device numbers for which a special register for modification is specified, modify it to the special register for QCPU/QnACPU.
- ② For the device numbers for which ☐ is specified, special register after conversion can be used.
- ③ Device numbers for which ☒ is specified do not function for QCPU/QnACPU.

Table App. 3.11. Special register

ACPU Special Register	Special Register after Conversion	Special Register for Modification	Name	Meaning	Details	Corresponding CPU																																																																																																																
D9000	SD1000	—	Fuse blown	Number of module with blown fuse	- When fuse blown modules are detected, the first I/O number of the lowest number of the detected modules is stored in hexadecimal. (Example: When fuses of Y50 to 6F output modules have blown, "50" is stored in hexadecimal) - To monitor the number by peripheral devices, perform monitor operation given in hexadecimal. (Cleared when all contents of SD1100 to SD1107 are reset to 0.) - Fuse blow check is executed also to the output modules of remote I/O stations.	QnA Qn(H) QnPH																																																																																																																
D9001	SD1001	—	Fuse blown	Number of module with blown fuse	- Stores the module numbers corresponding to setting switch numbers or base slot numbers when fuse blow occurred. <table><tr><th colspan="2">AJ02 I/O module</th><th colspan="2">Extension base unit</th></tr><tr><th>Setting switch</th><th>Stored data</th><th>Base unit slot No.</th><th>Stored data</th></tr><tr><td>0</td><td>0</td><td>0</td><td>4</td></tr><tr><td>1</td><td>1</td><td>1</td><td>5</td></tr><tr><td>2</td><td>2</td><td>2</td><td>6</td></tr><tr><td>3</td><td>3</td><td>3</td><td>7</td></tr><tr><td>4</td><td>4</td><td></td><td></td></tr><tr><td>5</td><td>5</td><td></td><td></td></tr><tr><td>6</td><td>6</td><td></td><td></td></tr><tr><td>7</td><td>7</td><td></td><td></td></tr></table> - For the remote I/O station, the value of (module I/O No./10H) + 1 is stored.		AJ02 I/O module		Extension base unit		Setting switch	Stored data	Base unit slot No.	Stored data	0	0	0	4	1	1	1	5	2	2	2	6	3	3	3	7	4	4			5	5			6	6			7	7																																																																										
AJ02 I/O module		Extension base unit																																																																																																																				
Setting switch	Stored data	Base unit slot No.	Stored data																																																																																																																			
0	0	0	4																																																																																																																			
1	1	1	5																																																																																																																			
2	2	2	6																																																																																																																			
3	3	3	7																																																																																																																			
4	4																																																																																																																					
5	5																																																																																																																					
6	6																																																																																																																					
7	7																																																																																																																					
D9002	SD1002	—	I/O module verify error	I/O module verify error module number	- If I/O modules, of which data are different from data entered, are detected when the power is turned on, the first I/O number of the lowest number unit among the detected units is stored in hexadecimal. (Storing method is the same as that of SD1000.) - To monitor the number by peripheral devices, perform monitor operation given in hexadecimal. (Cleared when all contents of SD1116 to SD1123 are reset to 0.) - I/O module verify check is executed also to the modules of remote I/O terminals.	QnA Qn(H) QnPH																																																																																																																
D9004	SD1004	—	MINI link master module errors	Stores setting status made at parameters	- Error status of the MINI(S3) link detected on loaded AJ71PT32(S3) is stored. <table><tr><td colspan="8">b15</td><td colspan="8">to</td><td colspan="8">b8</td><td colspan="8">b7</td><td colspan="8">to</td><td colspan="8">b0</td></tr><tr><td colspan="2">8th</td><td colspan="2">7th</td><td colspan="2">6th</td><td colspan="2">5th</td><td colspan="2">4th</td><td colspan="2">3rd</td><td colspan="2">2nd</td><td colspan="2">1st</td><td colspan="2">8th</td><td colspan="2">7th</td><td colspan="2">6th</td><td colspan="2">5th</td><td colspan="2">4th</td><td colspan="2">3rd</td><td colspan="2">2nd</td><td colspan="2">1st</td></tr><tr><td colspan="16"> Bits which correspond to faulty AJ71PT32(S3) are turned on. </td><td colspan="16"> Bits which correspond to the signals of AJ71PT32(S3), shown below, are turned on as the signals are turned on. - Hardware error (X0/X20) - MINI(S3) link error detection (X6/X26) - MINI(S3) link communication error (X7/X27) </td></tr></table>	b15								to								b8								b7								to								b0								8th		7th		6th		5th		4th		3rd		2nd		1st		8th		7th		6th		5th		4th		3rd		2nd		1st		Bits which correspond to faulty AJ71PT32(S3) are turned on.																Bits which correspond to the signals of AJ71PT32(S3), shown below, are turned on as the signals are turned on. - Hardware error (X0/X20) - MINI(S3) link error detection (X6/X26) - MINI(S3) link communication error (X7/X27)																QnA
b15								to								b8								b7								to								b0																																																																														
8th		7th		6th		5th		4th		3rd		2nd		1st		8th		7th		6th		5th		4th		3rd		2nd		1st																																																																																								
Bits which correspond to faulty AJ71PT32(S3) are turned on.																Bits which correspond to the signals of AJ71PT32(S3), shown below, are turned on as the signals are turned on. - Hardware error (X0/X20) - MINI(S3) link error detection (X6/X26) - MINI(S3) link communication error (X7/X27)																																																																																																						
D9005	SD1005	—	AC DOWN counter	Number of times for AC DOWN	When the AC power supply module is used, 1 is added at occurrence of an instantaneous power failure of within 20ms. (The value is stored in BIN code.) It is reset when the power supply is switched from OFF to ON.	QnA Qn(H) QnPH																																																																																																																
					When the DC power supply module is used, 1 is added at occurrence of an instantaneous power failure of within 10ms. (The value is stored in BIN code.) It is reset when the power supply is switched from OFF to ON.	Qn(H) QnPH																																																																																																																
					When the DC power supply module is used, 1 is added at occurrence of an instantaneous power failure of within 1ms. (The value is stored in BIN code.) It is reset when the power supply is switched from OFF to ON.	QnA																																																																																																																
D9008	SD1008	SD0	Self-diagnostic error	Self-diagnostic error number	When error is found as a result of self-diagnosis, error number is stored in BIN code.	QnA Qn(H) QnPH																																																																																																																

Table App. 3.11. Special register

ACPU Special Register	Special Register after Conversion	Special Register for Modification	Name	Meaning	Details	Corresponding CPU
D9009	SD1009	SD62	Annunciator detection	F number at which external failure has occurred	- When one of F0 to 2047 is turned on by [OUT F] or [SET F], the F number, which has been detected earliest among the F numbers which have turned on, is stored in BIN code. - SD62 can be cleared by [RST F] or [LEDR] instruction. If another F number has been detected, the clearing of SD62 causes the next number to be stored in SD62.	Qn(H) QnPH Q2AS Q2A
					- When one of F0 to 2047 is turned on by [OUT F] or [SET F], the F number, which has been detected earliest among the F numbers which have turned on, is stored in BIN code. - SD62 can be cleared by executing [RST F] or [LEDR] instruction or moving INDICATOR RESET switch on CPU module front to ON position. If another F number has been detected, clearing of SD62 stores the next F number into SD62.	Q3A Q4A Q4AR
D9010	SD1010	x	Error step	Step number at which operation error has occurred.	- When operation error has occurred during execution of application instruction, the step number, at which the error has occurred, is stored in BIN code. Thereafter, each time operation error occurs, the contents of SD1010 are renewed. - When operation error has occurred during execution of application instruction, the step number, at which the error has occurred, is stored in BIN code. Since the step number is stored into SD1011 when SM1011 turns from OFF to ON, the data of SD1011 is not updated unless SM1011 is cleared by a user program. - The I/O control mode set is returned in any of the following numbers: 0: Both input and output in direct mode 1: Input in refresh mode, output in direct mode 3: Both input and output in refresh mode	Qn(H) QnPH
D9011	SD1011	x	Error step	Step number at which operation error has occurred.		
D9014	SD1014	x	I/O control mode	I/O control mode number		
D9015	SD1015	SD203	Operating status of CPU	Operating status of CPU	The operation status of CPU as shown below are stored in SD203. b15 to b12 b11 to b8 b7 to b4 b3 to b0 Remote RUN/STOP by computer 0 RUN 1 STOP 2 PAUSE*1 CPU key switch 0 RUN 1 STOP 2 PAUSE*1 3 STEP RUN (Remains the same in remote RUN/STOP mode.) Status in program 0 Except below 1 [STOP] Instruction execution Remote RUN/STOP by parameter setting 0 RUN 1 STOP 2 PAUSE*1 *1: When the CPU module is in RUN mode and SM1040 is off, the CPU module remains in RUN mode if changed to PAUSE mode.	QnA Qn(H) QnPH

Table App. 3.11. Special register

ACPU Special Register	Special Register after Conversion	Special Register for Modification	Name	Meaning	Details	Corresponding CPU
D9016	SD1016	×	Program number	0: Main program (ROM) 1: Main program (RAM) 2: Subprogram 1 (RAM) 3: Subprogram 2 (RAM) 4: Subprogram 3 (RAM) 5: Subprogram 1 (ROM) 6: Subprogram 2 (ROM) 7: Subprogram 3 (ROM) 8: Main program (E ² PROM) 9: Subprogram 1 (E ² PROM) A: Subprogram 2 (E ² PROM) B: Subprogram 3 (E ² PROM)	Indicates which sequence program is run presently. One value of 0 to B is stored in BIN code.	QnA Qn(H) QnPH
D9017	SD1017	SD520	Scan time	Minimum scan time (10 ms units)	If scan time is smaller than the content of SD520, the value is newly stored at each END. Namely, the minimum value of scan time is stored into SD520 in BIN code.	
D9018	SD1018	SD524	Scan time	Scan time (10 ms units)	At every END, the scan time is stored in BIN code and always rewritten.	
D9019	SD1019	SD526	Scan time	Maximum scan time (10 ms units)	If scan time is larger than the content of SD526, the value is newly stored at each END. Namely, the maximum value of scan time is stored into SD526 in BIN code.	
D9020	SD1020	×	Constant scan	Constant scan time (User sets in 10 ms units)	Sets the interval between consecutive program starts in multiples of 10 ms. 0 : No setting 1 to 200 : Set. Program is executed at intervals of (set value) × 10 ms.	
D9021	SD1021	—	Scan time	Scan time (1 ms units)	At every END, the scan time is stored in BIN code and always rewritten.	
D9022	SD1022	SD412	1 second counter	Count in units of 1s.	- When the PC CPU starts running, it starts counting 1 every second. - It starts counting up from 0 to 32767, then down to -32768 and then again up to 0. Counting repeats this routine.	
D9025	SD1025	—	Clock data	Clock data (year, month)	The year (last two digits) and month are stored as BCD code as shown below. b15 to b12 b11 to b8 b7 to b4 b3 to b0 Example: 1987, July H8707 Year Month	
D9026	SD1026	—	Clock data	Clock data (day, hour)	The day and hour are stored as BCD code as shown below. b15 to b12 b11 to b8 b7 to b4 b3 to b0 Example: 31st, 10 a.m. H3110 Day Hour	
D9027	SD1027	—	Clock data	Clock data (minute, second)	The minute and second are stored as BCD code as shown below. b15 to b12 b11 to b8 b7 to b4 b3 to b0 Example: 35 min, 48 sec. H3548 Minute Second	

Table App. 3.11. Special register

ACPU Special Register	Special Register after Conversion	Special Register for Modification	Name	Meaning	Details	Corresponding CPU
D9028	SD1028	—	Clock data	Clock data (day of week)	The day of the week is stored as BCD code as shown below. b15 to b12b11 to b8b7 to b4b3 to b0 Example: Friday H0005 Always set "0". Day of the week 0 Sunday 1 Monday 2 Tuesday 3 Wednesday 4 Thursday 5 Friday 6 Saturday	QnA Qn(H) QnPH
D9035	SD1035	SD648	Extension file register	Use block No.	• Stores the block No. of the extension file register being used in BCD code.	
D9036	SD1036	x	Extension file registerfor designation of device number	Device number when individual devices from extension file register are directly accessed	• Designate the device number for the extension file register for direct read and write in 2 words at SD1036 and SD1037 in BIN data. Use consecutive numbers beginning with R0 of block No. 1 to designate device numbers. Extension file register 0 to 16383 Block No.1 area 16384 to Block No.2 area SD1037,SD1036 Device No. (BIN data) to	
D9037	SD1037	x				
D9038	SD1038	SD207	LED display priority ranking	Priorities 1 to 4	• Sets priority of ERROR LEDs which illuminate (or flicker) to indicate errors with error code numbers. • Configuration of the priority setting areas is as shown below. b15 to b12b11 to b8b7 to b4b3 to b0 SD207 Priority 4 Priority 3 Priority 2 Priority 1 SD208 Priority 7 Priority 6 Priority 5	
D9039	SD1039	SD208		Priorities 5 to 7	• For details, refer to the applicable CPUs User's Manual and the ACPU Programming manual (Fundamentals).	
D9044	SD1044	x	For sampling trace	Step or time during sampling trace	• Turned on/off with a peripheral device. When [STRA] or [STRAR] is executed, the value stored in SD1044 is used as the sampling trace condition. At scanning-----0 At time-----Time (10 msec unit) The value is stored into SD1044 in BIN code.	
D9049	SD1049	x	Work area for SFC	Block number of extension file register	• Stores the block number of the expansion file register which is used as the work area for the execution of a SFC program in a binary value. • Stores "0" if an empty area of 16K bytes or smaller, which cannot be expansion file register No. 1, is used or if SM320 is OFF.	
D9050	SD1050	x	SFC program error number	Error code generated by SFC program	• Stores error code of errors occurred in the SFC program in BIN code. 0 : No error 80: SFC program parameter error 81: SFC code error 82: Number of steps of simultaneous execution exceeded 83: Block start error 84: SFC program operation error	
D9051	SD1051	x	Error block	Block number where error occurred	• Stores the block number in which an error occurred in the SFC program in BIN code. In the case of error 83 the starting block number is stored.	
D9052	SD1052	x	Error step	Step number where error occurred	• Stores the step number, where error code 84 occurred in an SFC program, in BIN value. • Stores "0" when error code 80, 81 or 82 occurred. • Stores the block stating step number when error code 83 occurs.	

Table App. 3.11. Special register

ACPU Special Register	Special Register after Conversion	Special Register for Modification	Name	Meaning	Details	Corresponding CPU
D9053	SD1053	x	Error transition	Transition condition number where error occurred	Stores the transition condition number, where error code 84 occurred in an SFC program, in BIN value. Stores "0" when error code 80, 81, 82 or 83 occurred.	QnA Qn(H) QnPH
D9054	SD1054	x	Error sequence step	Sequence step number where error occurred	Stores the sequence step number of transfer condition and operation output in which error 84 occurred in the SFC program in BIN code.	
D9055	SD1055	SD812	Status latch execution step number	Status latch step	- Stores the step number when status latch is executed. - Stores the step number in a binary value if status latch is executed in a main sequence program. - Stores the block number and the step number if status latch is executed in a SFC program. Block No. (BIN) Step No. (BIN) ← Upper 8 bits → ← Lower 8 bits →	
D9060	SD1060	SD392	Software version	Software version of internal software	Stores the software version of the internal system in ASCII code. Upper byte Lower byte ↑ Stored into lower byte Undefined value in higher byte For version "A", for example, "41H" is stored. Note: The software version of the initial system may differ from the version indicated by the version information printed on the rear of the case.	QnA
D9072	SD1072	x	PLC communication check	Data check of serial communication module	In the self-loopback test of the serial communication module, the serial communication module writes/reads data automatically to make communication checks.	QnA Qn(H) QnPH
D9081	SD1081	SD714	Number of empty blocks in communications request registration area	Number of empty blocks in communications request registration area	Stores the number of empty blocks in the communication request registration area to the remote terminal module connected to the MELSECNET/MINI-S3 master unit, A2CCPU or A52GCPU.	QnA
D9085	SD1085	x	Register for setting time check value	1 s to 65535 s	- Sets the time check time of the data link instructions (ZNRD, ZNWR) for the MELSECNET/10. - Setting range : 1 s to 65535 s (1 to 65535) - Setting unit: 1 s - Default value : 10 s (If 0 has been set, default 10 s is applied)	QnA Qn(H) QnPH
D9090	SD1090	x	Number of special functions modules over	Number of special functions modules over	For details, refer to the manual of each microcomputer program package.	
D9091	SD1091	x	Detailed error code	Self-diagnosis detailed error code	Stores the detail code of cause of an instruction error.	
D9094	SD1094	SD251	Head I/O number of I/O module to be replaced	Head I/O number of I/O module to be replaced	Stores the first two digits of the head I/O number of the I/O module, which will be dismantled/mounted online (with power on), in BIN value. Example) Input module X2F0 → H2F	Qn(H) QnPH
D9095	SD1095	SD200	DIP switch information	DIP switch information	The DIP switch information of the CPU module is stored in the following format. 0: OFF 1: ON D9095 b15 tob5b4b3b2b1b0 0 ↑ ↑ ↑ ↑ ↑ ↑ SW1 SW2 SW3 SW4 SW5	

Table App. 3.11. Special register

ACPU Special Register	Special Register after Conversion	Special Register for Modification	Name	Meaning	Details	Corresponding CPU
D9100	SD1100	-	Fuse blown module	Bit pattern in units of 16 points, indicating the modules whose fuses have blown	- Output module numbers (in units of 16 points), of which fuses have blown, are entered in bit pattern. (Preset output module numbers when parameter setting has been performed.) b15 b14 b13 b12 b11 b10 b9 b8 b7 b6 b5 b4 b3 b2 b1 b0 SD1100 0 0 0 1 (YCO) 0 0 0 1 (Y80) 0 0 0 0 0 0 0 SD1101 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 SD1107 0 0 0 0 1 (Y7) 0 0 0 0 0 0 0 0 1 (Y7) 0 0 0 ↑ Indicates fuse blow. - Fuse blow check is executed also to the output module of remote I/O station. (If normal status is restored, clear is not performed. Therefore, it is required to perform clear by user program.)	QnA Qn(H) QnPH
D9101	SD1101					
D9102	SD1102					
D9103	SD1103					
D9104	SD1104					
D9105	SD1105					
D9106	SD1106					
D9107	SD1107					
D9108	SD1108	-	Step transfer monitoring timer setting	Timer setting valve and the F number at time out	- Set the value of the step transition monitoring timer and the annunciator number (F number) that will be turned ON when the monitoring timer times out. b15 to b8 b7 to b0 ↑ ↑ F number setting Timer time limit setting (02 to 255) (1 to 255 s: (1 s units)) - By turning ON any of SM1108 to SM1114, the monitoring timer starts. If the transition condition following a step which corresponds to the timer is not established within set time, set annunciator (F) is turned on.)	QnA Qn(H) QnPH
D9109	SD1109					
D9110	SD1110					
D9111	SD1111					
D9112	SD1112					
D9113	SD1113					
D9114	SD1114					
D9116	SD1116	-	I/O module verification error	Bit pattern, in units of 16 points, indicating the modules with verification errors.	- When I/O modules, of which data are different from those entered at power-ON, have been detected, the I/O module numbers (in units of 16 points) are entered in bit pattern. (Preset I/O module numbers set in parameters when parameter setting has been performed.) b15 b14 b13 b12 b11 b10 b9 b8 b7 b6 b5 b4 b3 b2 b1 b0 SD1116 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 (XV) SD1117 0 0 0 0 0 0 0 1 (XV) 0 0 0 0 0 0 0 0 SD1123 0 0 0 0 1 (XV) 0 0 0 0 0 0 0 0 0 0 0 0 ↑ Indicates an I/O module verify error. - I/O module verify check is executed also to remote I/O station modules. (If normal status is restored, clear is not performed. Therefore, it is required to perform clear by user program.)	QnA Qn(H) QnPH
D9117	SD1117					
D9118	SD1118					
D9119	SD1119					
D9120	SD1120					
D9121	SD1121					
D9122	SD1122					
D9123	SD1123					
D9124	SD1124	SD63	Number of annunciator detections	Number of annunciator detections	- When one of F0 to 255 (F0 to 2047 for AuA and AnU) is turned on by [SET F] 1 is added to the contents of SD63. When [RST F] or [LEDR] instruction is executed, 1 is subtracted from the contents of SD63. (If the INDICATOR RESET switch is provided to the CPU module, pressing the switch can execute the same processing.) - Quantity, which has been turned on by [SET F] is stored into SD63 in BIN code. The value of SD63 is maximum 8.	

Table App. 3.11. Special register

ACPU Special Register	Special Register after Conversion	Special Register for Modification	Name	Meaning	Details	Corresponding CPU
D9125	SD1125	SD64	Annunciator detection number	Annunciator detection number	- When any of F0 to 2047 is turned on by [SET F], the annunciator numbers (F numbers) that are turned on in order are registered into D9125 to D9132. - The F number turned off by [RST F] is erased from any of D9125 to D9132, and the F numbers stored after the erased F number are shifted to the preceding registers. By executing [LEDR] instruction, the contents of SD64 to SD71 are shifted upward by one. (For A3N, A3HCPU, it can be performed by use of INDICATOR RESET switch on front of CPU module.) When there are 8 annunciator detections, the 9th one is not stored into SD64 to SD71 even if detected. SET SET SET RST SET SET SET SET SET SET SET SET SET F50 F25 F99 F25 F15 F70 F65 F38 F110 F151 F210 LEDR	QnA Qn(H) QnPH
D9126	SD1126	SD65				
D9127	SD1127	SD66				
D9128	SD1128	SD67				
D9129	SD1129	SD68				
D9130	SD1130	SD69				
D9131	SD1131	SD70				
D9132	SD1132	SD71				

SD62	0	50	50	50	50	50	50	50	50	50	50	50	99
SD63	0	1	2	3	2	3	4	5	6	7	8	8	8
SD64	0	50	50	50	50	50	50	50	50	50	50	50	99
SD65	0	0	25	25	99	99	99	99	99	99	99	99	15
SD66	0	0	0	99	0	15	15	15	15	15	15	15	70
SD67	0	0	0	0	0	0	70	70	70	70	70	70	65
SD68	0	0	0	0	0	0	0	65	65	65	65	65	38
SD69	0	0	0	0	0	0	0	0	38	38	38	38	110
SD70	0	0	0	0	0	0	0	0	0	110	110	110	151
SD71	0	0	0	0	0	0	0	0	0	0	151	151	210

(11) Special register list dedicated for QnA

Table App. 3.12. Special register

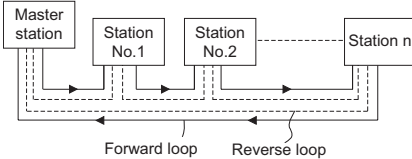
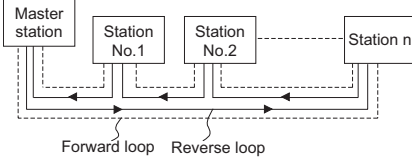
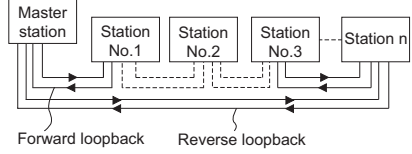
ACPU Special Register	Special Register after Conversion	Special Register for Modification	Name	Meaning	Details	Corresponding CPU																																																																																																			
D9200	SD1200	—	ZNRD instruction processing result (LRDP for ACPU)	0 : Normal end 2 : ZNRD instruction setting fault 3 : Error at relevant station 4 : Relevant station ZNRD execution disabled	Stores the execution result of the ZNRD (word device read) instruction • ZNRD instruction setting faultFaulty setting of the ZNRD instruction constant, source, and/or destination. • Corresponding station errorOne of the stations is not communicating. • ZNRD cannot be executed in the corresponding station The specified station is a remote I/O station.	QnA																																																																																																			
D9201	SD1201	—	ZNWR instruction processing result (LWTP for ACPU)	0 : Normal end 2 : ZNWR instruction setting fault 3 : Error at relevant station 4 : Relevant station ZNWR execution disabled	Stores the execution result of the ZNWR (word device write) instruction. • ZNWR instruction setting faultFaulty setting of the ZNWR instruction constant, source, and/or destination. • Corresponding station errorOne of the stations is not communicating. • ZNWR cannot be executed in the corresponding station The specified station is a remote I/O station.																																																																																																				
D9202	SD1202	—	Local station link type	Stores conditions for up to numbers 1 to 16	Stores whether the slave station corresponds to MELSECNET or MELSECNET II. • Bits corresponding to the MELSECNET II stations become "1." • Bits corresponding to the MELSECNET stations or unconnected become "0."																																																																																																				
D9203	SD1203	—		Stores conditions for up to numbers 17 to 32	<table><tr><th rowspan="2">Device number</th><th colspan="16">Bit</th></tr><tr><th>b15</th><th>b14</th><th>b13</th><th>b12</th><th>b11</th><th>b10</th><th>b9</th><th>b8</th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th></tr><tr><td>SD1202</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>SD1203</td><td>L32</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr><tr><td>SD1241</td><td>L48</td><td>L47</td><td>L46</td><td>L45</td><td>L44</td><td>L43</td><td>L42</td><td>L41</td><td>L40</td><td>L39</td><td>L38</td><td>L37</td><td>L36</td><td>L35</td><td>L34</td><td>L33</td></tr><tr><td>SD1242</td><td>L64</td><td>L63</td><td>L62</td><td>L61</td><td>L60</td><td>L59</td><td>L58</td><td>L57</td><td>L56</td><td>L55</td><td>L54</td><td>L53</td><td>L52</td><td>L51</td><td>L50</td><td>L49</td></tr></table> • If a local station goes down during the operation, the contents before going down are retained. Contents of SD1224 to SD1227 and SD1228 to SD1231 are ORed. If the corresponding bit is "0", the corresponding bit of the special register above becomes valid. • If the host (master) station goes down, the contents before going down are also retained.		Device number	Bit																b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	SD1202	L16	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	SD1203	L32	L31	L30	L29	L28	L27	L26	L25	L24	L23	L22	L21	L20	L19	L18	L17	SD1241	L48	L47	L46	L45	L44	L43	L42	L41	L40	L39	L38	L37	L36	L35	L34	L33	SD1242	L64	L63	L62	L61	L60	L59	L58	L57	L56	L55	L54	L53	L52	L51
Device number	Bit																																																																																																								
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0																																																																																									
SD1202	L16	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1																																																																																									
SD1203	L32	L31	L30	L29	L28	L27	L26	L25	L24	L23	L22	L21	L20	L19	L18	L17																																																																																									
SD1241	L48	L47	L46	L45	L44	L43	L42	L41	L40	L39	L38	L37	L36	L35	L34	L33																																																																																									
SD1242	L64	L63	L62	L61	L60	L59	L58	L57	L56	L55	L54	L53	L52	L51	L50	L49																																																																																									
D9204	SD1204	—	Link status	0 : Forward loop, during data link 1 : Reverse loop, during data link 2 : Loopback implemented in forward/reverse directions 3 : Loopback implemented only in forward direction 4 : Loopback implemented only in reverse direction 5 : Data link disabled	Stores the present path status of the data link. • Data link in forward loop  • Data link in reverse loop  • Loopback implemented in forward/reverse directions 																																																																																																				

Table App. 3.12. Special register

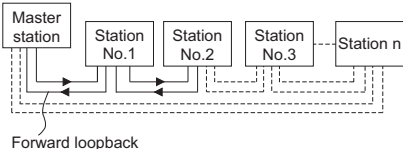
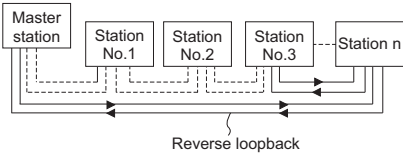
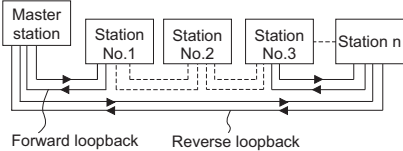
ACPU Special Register	Special Register after Conversion	Special Register for Modification	Name	Meaning	Details	Corresponding CPU																																																																																					
D9204	SD1204	—	Link status	0 : Forward loop, during data link 1 : Reverse loop, during data link 2 : Loopback implemented in forward/reverse directions 3 : Loopback implemented only in forward direction 4 : Loopback implemented only in reverse direction 5 : Data link disabled	• Loopback in forward loop only  Forward loopback • Loopback in reverse loop only  Reverse loopback	QnA																																																																																					
D9205	SD1205	—	Station implementing loopback	Station that implemented forward loopback	Stores the local or remote I/O station number at which loopback is being executed.  Forward loopback																																																																																						
D9206	SD1206	—	Station implementing loopback	Station that implemented reverse loopback	In the above example, 1 is stored into D9205 and 3 into D9206. If data link returns to normal status (data link in forward loop), values in D9205 and D9206 remain 1 and 3. To return them to "0", therefore, use a sequence program or perform reset operation.																																																																																						
D9210	SD1210	—	Number of retries	Stored as cumulative value	Stores the number of retry times due to transmission error. Count stops at maximum of "FFFFH". To return the value to "0", perform reset operation.																																																																																						
D9211	SD1211	—	Number of times loop selected	Stored as cumulative value	Stores the number of times the loop line has been switched to reverse loop or loopback. Count stops at maximum of "FFFFH". To return the value to "0", perform reset operation.																																																																																						
D9212	SD1212	—	Local station operation status	Stores conditions for up to numbers 1 to 16	Stores the local station numbers which are in STOP or PAUSE mode. <table><tr><th>Device number</th><th>b15</th><th>b14</th><th>b13</th><th>b12</th><th>b11</th><th>b10</th><th>b9</th><th>b8</th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th></tr><tr><td>SD1212</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>SD1213</td><td>L32</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr><tr><td>SD1214</td><td>L48</td><td>L47</td><td>L46</td><td>L45</td><td>L44</td><td>L43</td><td>L42</td><td>L41</td><td>L40</td><td>L39</td><td>L38</td><td>L37</td><td>L36</td><td>L35</td><td>L34</td><td>L33</td></tr><tr><td>SD1215</td><td>L64</td><td>L63</td><td>L62</td><td>L61</td><td>L60</td><td>L59</td><td>L58</td><td>L57</td><td>L56</td><td>L55</td><td>L54</td><td>L53</td><td>L52</td><td>L51</td><td>L50</td><td>L49</td></tr></table>		Device number	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	SD1212	L16	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	SD1213	L32	L31	L30	L29	L28	L27	L26	L25	L24	L23	L22	L21	L20	L19	L18	L17	SD1214	L48	L47	L46	L45	L44	L43	L42	L41	L40	L39	L38	L37	L36	L35	L34	L33	SD1215	L64	L63	L62	L61	L60	L59	L58	L57	L56	L55	L54	L53	L52	L51	L50	L49
Device number	b15	b14	b13	b12	b11		b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0																																																																										
SD1212	L16	L15	L14	L13	L12		L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1																																																																										
SD1213	L32	L31	L30	L29	L28		L27	L26	L25	L24	L23	L22	L21	L20	L19	L18	L17																																																																										
SD1214	L48	L47	L46	L45	L44		L43	L42	L41	L40	L39	L38	L37	L36	L35	L34	L33																																																																										
SD1215	L64	L63	L62	L61	L60	L59	L58	L57	L56	L55	L54	L53	L52	L51	L50	L49																																																																											
D9213	SD1213	—	Local station operation status	Stores conditions for up to numbers 17 to 32																																																																																							
D9214	SD1214	—	Local station operation status	Stores conditions for up to numbers 33 to 48	When a local station is switched to STOP or PAUSE mode, the bit corresponding to the station number in the register becomes "1". Example: When station 7 switches to STOP mode, b6 in SD1212 becomes "1", and when SD1212 is monitored, its value is "64 (40H)".																																																																																						
D9215	SD1215	—	Local station operation status	Stores conditions for up to numbers 49 to 64																																																																																							
D9216	SD1216	—	Local station error detect status	Stores conditions for up to numbers 1 to 16	Stores the local station numbers which are in error. <table><tr><th>Device number</th><th>b15</th><th>b14</th><th>b13</th><th>b12</th><th>b11</th><th>b10</th><th>b9</th><th>b8</th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th></tr><tr><td>SD1216</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>SD1217</td><td>L32</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr><tr><td>SD1218</td><td>L48</td><td>L47</td><td>L46</td><td>L45</td><td>L44</td><td>L43</td><td>L42</td><td>L41</td><td>L40</td><td>L39</td><td>L38</td><td>L37</td><td>L36</td><td>L35</td><td>L34</td><td>L33</td></tr><tr><td>SD1219</td><td>L64</td><td>L63</td><td>L62</td><td>L61</td><td>L60</td><td>L59</td><td>L58</td><td>L57</td><td>L56</td><td>L55</td><td>L54</td><td>L53</td><td>L52</td><td>L51</td><td>L50</td><td>L49</td></tr></table>	Device number	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	SD1216	L16	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	SD1217	L32	L31	L30	L29	L28	L27	L26	L25	L24	L23	L22	L21	L20	L19	L18	L17	SD1218	L48	L47	L46	L45	L44	L43	L42	L41	L40	L39	L38	L37	L36	L35	L34	L33	SD1219	L64	L63	L62	L61	L60	L59	L58	L57	L56	L55	L54	L53	L52	L51	L50	L49	
Device number	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0																																																																											
SD1216	L16	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1																																																																											
SD1217	L32	L31	L30	L29	L28	L27	L26	L25	L24	L23	L22	L21	L20	L19	L18	L17																																																																											
SD1218	L48	L47	L46	L45	L44	L43	L42	L41	L40	L39	L38	L37	L36	L35	L34	L33																																																																											
SD1219	L64	L63	L62	L61	L60	L59	L58	L57	L56	L55	L54	L53	L52	L51	L50	L49																																																																											
D9217	SD1217	—	Local station error detect status	Stores conditions for up to numbers 17 to 32																																																																																							
D9218	SD1218	—	Local station error detect status	Stores conditions for up to numbers 33 to 48	If a local station detects an error, the bit corresponding to the station number becomes "1". Example: When station 6 and 12 detect an error, b5 and 11 in SD1216 become "1", and when SD1216 is monitored, its value is "2080 (820H)".																																																																																						
D9219	SD1219	—	Local station error detect status	Stores conditions for up to numbers 49 to 64																																																																																							

Table App. 3.12. Special register

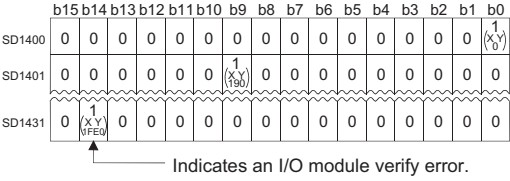
ACPU Special Register	Special Register after Conversion	Special Register for Modification	Name	Meaning	Details	Corresponding CPU																																																																																																						
D9220	SD1220	—	Local station parameters non-conforming; remote I/O station I/O assignment error	Stores conditions for up to numbers 1 to 16	Stores the local station numbers which contain mismatched parameters or of remote station numbers for which incorrect I/O assignment has been made. <table><tr><th>Device number</th><th colspan="16">Bit</th></tr><tr><td></td><td>b15</td><td>b14</td><td>b13</td><td>b12</td><td>b11</td><td>b10</td><td>b9</td><td>b8</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr><tr><td>SD1220</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>SD1221</td><td>L32</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr><tr><td>SD1222</td><td>L48</td><td>L47</td><td>L46</td><td>L45</td><td>L44</td><td>L43</td><td>L42</td><td>L41</td><td>L40</td><td>L39</td><td>L38</td><td>L37</td><td>L36</td><td>L35</td><td>L34</td><td>L33</td></tr><tr><td>SD1223</td><td>L64</td><td>L63</td><td>L62</td><td>L61</td><td>L60</td><td>L59</td><td>L58</td><td>L57</td><td>L56</td><td>L55</td><td>L54</td><td>L53</td><td>L52</td><td>L51</td><td>L50</td><td>L49</td></tr></table>	Device number	Bit																	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	SD1220	L16	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	SD1221	L32	L31	L30	L29	L28	L27	L26	L25	L24	L23	L22	L21	L20	L19	L18	L17	SD1222	L48	L47	L46	L45	L44	L43	L42	L41	L40	L39	L38	L37	L36	L35	L34	L33	SD1223	L64	L63	L62	L61	L60	L59	L58	L57	L56	L55	L54	L53	L52	L51	L50	L49	QnA
Device number	Bit																																																																																																											
	b15	b14	b13	b12		b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0																																																																																											
SD1220	L16	L15	L14	L13		L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1																																																																																											
SD1221	L32	L31	L30	L29	L28	L27	L26	L25	L24	L23	L22	L21	L20	L19	L18	L17																																																																																												
SD1222	L48	L47	L46	L45	L44	L43	L42	L41	L40	L39	L38	L37	L36	L35	L34	L33																																																																																												
SD1223	L64	L63	L62	L61	L60	L59	L58	L57	L56	L55	L54	L53	L52	L51	L50	L49																																																																																												
D9221	SD1221	—	Local station parameters non-conforming; remote I/O station I/O assignment error	Stores conditions for up to numbers 17 to 32																																																																																																								
D9222	SD1222	—	Local station parameters non-conforming; remote I/O station I/O assignment error	Stores conditions for up to numbers 33 to 48																																																																																																								
D9223	SD1223	—	Local station parameters non-conforming; remote I/O station I/O assignment error	Stores conditions for up to numbers 49 to 64																																																																																																								
D9224	SD1224	—	Local station and remote I/O station initial communications underway	Stores conditions for up to numbers 1 to 16	Stores the local or remote station numbers while they are communicating the initial data with their relevant master station. <table><tr><th>Device number</th><th colspan="16">Bit</th></tr><tr><td></td><td>b15</td><td>b14</td><td>b13</td><td>b12</td><td>b11</td><td>b10</td><td>b9</td><td>b8</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr><tr><td>SD1224</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>SD1225</td><td>L32</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr><tr><td>SD1226</td><td>L48</td><td>L47</td><td>L46</td><td>L45</td><td>L44</td><td>L43</td><td>L42</td><td>L41</td><td>L40</td><td>L39</td><td>L38</td><td>L37</td><td>L36</td><td>L35</td><td>L34</td><td>L33</td></tr><tr><td>SD1227</td><td>L64</td><td>L63</td><td>L62</td><td>L61</td><td>L60</td><td>L59</td><td>L58</td><td>L57</td><td>L56</td><td>L55</td><td>L54</td><td>L53</td><td>L52</td><td>L51</td><td>L50</td><td>L49</td></tr></table>	Device number	Bit																	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	SD1224	L16	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	SD1225	L32	L31	L30	L29	L28	L27	L26	L25	L24	L23	L22	L21	L20	L19	L18	L17	SD1226	L48	L47	L46	L45	L44	L43	L42	L41	L40	L39	L38	L37	L36	L35	L34	L33	SD1227	L64	L63	L62	L61	L60	L59	L58	L57	L56	L55	L54	L53	L52	L51	L50	L49	QnA
Device number	Bit																																																																																																											
	b15	b14	b13	b12		b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0																																																																																											
SD1224	L16	L15	L14	L13		L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1																																																																																											
SD1225	L32	L31	L30	L29	L28	L27	L26	L25	L24	L23	L22	L21	L20	L19	L18	L17																																																																																												
SD1226	L48	L47	L46	L45	L44	L43	L42	L41	L40	L39	L38	L37	L36	L35	L34	L33																																																																																												
SD1227	L64	L63	L62	L61	L60	L59	L58	L57	L56	L55	L54	L53	L52	L51	L50	L49																																																																																												
D9225	SD1225	—	Local station and remote I/O station initial communications underway	Stores conditions for up to numbers 17 to 32																																																																																																								
D9226	SD1226	—	Local station and remote I/O station initial communications underway	Stores conditions for up to numbers 33 to 48																																																																																																								
D9227	SD1227	—	Local station and remote I/O station initial communications underway	Stores conditions for up to numbers 49 to 64																																																																																																								
D9228	SD1228	—	Local station and remote I/O station error	Stores conditions for up to numbers 1 to 16	Stores the local or remote station numbers which are in error. <table><tr><th>Device number</th><th colspan="16">Bit</th></tr><tr><td></td><td>b15</td><td>b14</td><td>b13</td><td>b12</td><td>b11</td><td>b10</td><td>b9</td><td>b8</td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td>b2</td><td>b1</td><td>b0</td></tr><tr><td>SD1228</td><td>L16</td><td>L15</td><td>L14</td><td>L13</td><td>L12</td><td>L11</td><td>L10</td><td>L9</td><td>L8</td><td>L7</td><td>L6</td><td>L5</td><td>L4</td><td>L3</td><td>L2</td><td>L1</td></tr><tr><td>SD1229</td><td>L32</td><td>L31</td><td>L30</td><td>L29</td><td>L28</td><td>L27</td><td>L26</td><td>L25</td><td>L24</td><td>L23</td><td>L22</td><td>L21</td><td>L20</td><td>L19</td><td>L18</td><td>L17</td></tr><tr><td>SD1230</td><td>L48</td><td>L47</td><td>L46</td><td>L45</td><td>L44</td><td>L43</td><td>L42</td><td>L41</td><td>L40</td><td>L39</td><td>L38</td><td>L37</td><td>L36</td><td>L35</td><td>L34</td><td>L33</td></tr><tr><td>SD1231</td><td>L64</td><td>L63</td><td>L62</td><td>L61</td><td>L60</td><td>L59</td><td>L58</td><td>L57</td><td>L56</td><td>L55</td><td>L54</td><td>L53</td><td>L52</td><td>L51</td><td>L50</td><td>L49</td></tr></table>	Device number	Bit																	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	SD1228	L16	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	SD1229	L32	L31	L30	L29	L28	L27	L26	L25	L24	L23	L22	L21	L20	L19	L18	L17	SD1230	L48	L47	L46	L45	L44	L43	L42	L41	L40	L39	L38	L37	L36	L35	L34	L33	SD1231	L64	L63	L62	L61	L60	L59	L58	L57	L56	L55	L54	L53	L52	L51	L50	L49	QnA
Device number	Bit																																																																																																											
	b15	b14	b13	b12		b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0																																																																																											
SD1228	L16	L15	L14	L13		L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1																																																																																											
SD1229	L32	L31	L30	L29	L28	L27	L26	L25	L24	L23	L22	L21	L20	L19	L18	L17																																																																																												
SD1230	L48	L47	L46	L45	L44	L43	L42	L41	L40	L39	L38	L37	L36	L35	L34	L33																																																																																												
SD1231	L64	L63	L62	L61	L60	L59	L58	L57	L56	L55	L54	L53	L52	L51	L50	L49																																																																																												
D9229	SD1229	—	Local station and remote I/O station error	Stores conditions for up to numbers 17 to 32																																																																																																								
D9230	SD1230	—	Local station and remote I/O station error	Stores conditions for up to numbers 33 to 48																																																																																																								
D9231	SD1231	—	Local station and remote I/O station error	Stores conditions for up to numbers 49 to 64																																																																																																								

Table App. 3.12. Special register

ACPU Special Register	Special Register after Conversion	Special Register for Modification	Name	Meaning	Details	Corresponding CPU																																																																																																																																																																																																																																																																																																																		
D9232	SD1232	—	Local station and remote I/O station loop error	Stores conditions for up to numbers 1 to 8	Stores the local or remote station number at which a forward or reverse loop error has occurred <table><tr><th>Device number</th><th colspan="16">Bit</th></tr><tr><th></th><th>b15</th><th>b14</th><th>b13</th><th>b12</th><th>b11</th><th>b10</th><th>b9</th><th>b8</th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th></tr><tr><td>SD1232</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td>L/R8</td><td>L/R7</td><td>L/R6</td><td>L/R5</td><td>L/R4</td><td>L/R3</td><td>L/R2</td><td>L/R1</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>SD1233</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td>L/R16</td><td>L/R15</td><td>L/R14</td><td>L/R13</td><td>L/R12</td><td>L/R11</td><td>L/R10</td><td>L/R9</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>SD1234</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td>L/R24</td><td>L/R23</td><td>L/R22</td><td>L/R21</td><td>L/R20</td><td>L/R19</td><td>L/R18</td><td>L/R17</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>SD1235</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td>L/R32</td><td>L/R31</td><td>L/R30</td><td>L/R29</td><td>L/R28</td><td>L/R27</td><td>L/R26</td><td>L/R25</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>SD1236</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td>L/R40</td><td>L/R39</td><td>L/R38</td><td>L/R37</td><td>L/R36</td><td>L/R35</td><td>L/R34</td><td>L/R33</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>SD1237</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td>L/R48</td><td>L/R47</td><td>L/R46</td><td>L/R45</td><td>L/R44</td><td>L/R43</td><td>L/R42</td><td>L/R41</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>SD1238</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td>L/R56</td><td>L/R55</td><td>L/R54</td><td>L/R53</td><td>L/R52</td><td>L/R51</td><td>L/R50</td><td>L/R49</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>SD1239</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td><td>R</td><td>F</td></tr><tr><td></td><td>L/R64</td><td>L/R63</td><td>L/R62</td><td>L/R61</td><td>L/R60</td><td>L/R59</td><td>L/R58</td><td>L/R57</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table> "F" in the above table indicates a forward loop line, and "R" a reverse loop line. The bit of the device number corresponding to the station number of the local station or remote I/O station that has a forward loop line or reverse loop line error. Example: When the forward loop line of station 5 has an error, b8 of SD1232 become "1", and when SD1232 is monitored, its value is "256 (100H)".	Device number	Bit																	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	SD1232	R	F	R	F	R	F	R	F	R	F	R	F	R	F	R	F		L/R8	L/R7	L/R6	L/R5	L/R4	L/R3	L/R2	L/R1									SD1233	R	F	R	F	R	F	R	F	R	F	R	F	R	F	R	F		L/R16	L/R15	L/R14	L/R13	L/R12	L/R11	L/R10	L/R9									SD1234	R	F	R	F	R	F	R	F	R	F	R	F	R	F	R	F		L/R24	L/R23	L/R22	L/R21	L/R20	L/R19	L/R18	L/R17									SD1235	R	F	R	F	R	F	R	F	R	F	R	F	R	F	R	F		L/R32	L/R31	L/R30	L/R29	L/R28	L/R27	L/R26	L/R25									SD1236	R	F	R	F	R	F	R	F	R	F	R	F	R	F	R	F		L/R40	L/R39	L/R38	L/R37	L/R36	L/R35	L/R34	L/R33									SD1237	R	F	R	F	R	F	R	F	R	F	R	F	R	F	R	F		L/R48	L/R47	L/R46	L/R45	L/R44	L/R43	L/R42	L/R41									SD1238	R	F	R	F	R	F	R	F	R	F	R	F	R	F	R	F		L/R56	L/R55	L/R54	L/R53	L/R52	L/R51	L/R50	L/R49									SD1239	R	F	R	F	R	F	R	F	R	F	R	F	R	F	R	F		L/R64	L/R63	L/R62	L/R61	L/R60	L/R59	L/R58	L/R57									
Device number	Bit																																																																																																																																																																																																																																																																																																																							
	b15	b14	b13	b12		b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0																																																																																																																																																																																																																																																																																																							
SD1232	R	F	R	F		R	F	R	F	R	F	R	F	R	F	R	F																																																																																																																																																																																																																																																																																																							
	L/R8	L/R7	L/R6	L/R5		L/R4	L/R3	L/R2	L/R1																																																																																																																																																																																																																																																																																																															
SD1233	R	F	R	F		R	F	R	F	R	F	R	F	R	F	R	F																																																																																																																																																																																																																																																																																																							
	L/R16	L/R15	L/R14	L/R13		L/R12	L/R11	L/R10	L/R9																																																																																																																																																																																																																																																																																																															
SD1234	R	F	R	F		R	F	R	F	R	F	R	F	R	F	R	F																																																																																																																																																																																																																																																																																																							
	L/R24	L/R23	L/R22	L/R21		L/R20	L/R19	L/R18	L/R17																																																																																																																																																																																																																																																																																																															
SD1235	R	F	R	F		R	F	R	F	R	F	R	F	R	F	R	F																																																																																																																																																																																																																																																																																																							
	L/R32	L/R31	L/R30	L/R29	L/R28	L/R27	L/R26	L/R25																																																																																																																																																																																																																																																																																																																
SD1236	R	F	R	F	R	F	R	F	R	F	R	F	R	F	R	F																																																																																																																																																																																																																																																																																																								
	L/R40	L/R39	L/R38	L/R37	L/R36	L/R35	L/R34	L/R33																																																																																																																																																																																																																																																																																																																
SD1237	R	F	R	F	R	F	R	F	R	F	R	F	R	F	R	F																																																																																																																																																																																																																																																																																																								
	L/R48	L/R47	L/R46	L/R45	L/R44	L/R43	L/R42	L/R41																																																																																																																																																																																																																																																																																																																
SD1238	R	F	R	F	R	F	R	F	R	F	R	F	R	F	R	F																																																																																																																																																																																																																																																																																																								
	L/R56	L/R55	L/R54	L/R53	L/R52	L/R51	L/R50	L/R49																																																																																																																																																																																																																																																																																																																
SD1239	R	F	R	F	R	F	R	F	R	F	R	F	R	F	R	F																																																																																																																																																																																																																																																																																																								
	L/R64	L/R63	L/R62	L/R61	L/R60	L/R59	L/R58	L/R57																																																																																																																																																																																																																																																																																																																
D9233	SD1233	—	Local station and remote I/O station loop error	Stores conditions for up to numbers 9 to 16																																																																																																																																																																																																																																																																																																																				
D9234	SD1234	—	Local station and remote I/O station loop error	Stores conditions for up to numbers 17 to 24																																																																																																																																																																																																																																																																																																																				
D9235	SD1235	—	Local station and remote I/O station loop error	Stores conditions for up to numbers 25 to 32																																																																																																																																																																																																																																																																																																																				
D9236	SD1236	—	Local station and remote I/O station loop error	Stores conditions for up to numbers 33 to 40																																																																																																																																																																																																																																																																																																																				
D9237	SD1237	—	Local station and remote I/O station loop error	Stores conditions for up to numbers 41 to 48																																																																																																																																																																																																																																																																																																																				
D9238	SD1238	—	Local station and remote I/O station loop error	Stores conditions for up to numbers 49 to 56																																																																																																																																																																																																																																																																																																																				
D9239	SD1239	—	Local station and remote I/O station loop error	Stores conditions for up to numbers 57 to 64																																																																																																																																																																																																																																																																																																																				
D9240	SD1240	—	Number of times communications errors detected	Stores cumulative total of receive errors	Stores the number of times the following transmission errors have been detected: CRC, OVER, AB. IF Count is made to a maximum of FFFFH. To return the value to "0", perform reset operation.	QnA																																																																																																																																																																																																																																																																																																																		
D9241	SD1241	—	Local station link type	Stores conditions for up to numbers 33 to 48	Stores whether the slave station corresponds to MELSECNET or MELSECNET II. • Bits corresponding to the MELSECNET II stations become "1." • Bits corresponding to the MELSECNET stations or unconnected become "0."																																																																																																																																																																																																																																																																																																																			
D9242	SD1242			Stores conditions for up to numbers 49 to 64	• If a local station goes down during the operation, the contents before going down are retained. Contents of SD1224 to SD1227 and SD1228 to SD1231 are ORed. If the corresponding bit is "0", the corresponding bit of the special register above becomes valid. • If the host (master) station goes down, the contents before going down are also retained.																																																																																																																																																																																																																																																																																																																			
D9243	SD1243	—	Station number information for host station	Stores station number (0 to 64)	Allows a local station to confirm its own station number																																																																																																																																																																																																																																																																																																																			
D9244	SD1244	—	Number of link device stations	Stores number of slave stations	Indicates the number of slave stations in one loop.																																																																																																																																																																																																																																																																																																																			
D9245	SD1245	—	Receive error detection count	Stores cumulative total of receive errors	Stores the number of times the following transmission errors have been detected: CRC, OVER, AB. IF Count is made to a maximum of FFFFH. To return the value to "0", perform reset operation.																																																																																																																																																																																																																																																																																																																			

(13) I/O module verification

Table App. 3.14. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD1400	I/O module verify error	Bit pattern, in units of 16 points, indicating the modules with verification errors. 0 : No I/O verification errors 1 : I/O verification error present	- When the I/O modules whose I/O module information differs from that registered at power-ON are detected, the numbers of those I/O modules are entered in bit pattern. (If the I/O numbers are set by parameter, the parameter-set numbers are stored.) - Also detects I/O module information.  - Not cleared even if the blown fuse is replaced with a new one. This flag is cleared by error resetting operation.	S (Error)	D9116	QnA Qn(H) QnPH QnPRH QnU Rem
SD1401					D9117	
SD1402					D9118	
SD1403					D9119	
SD1404					D9120	
SD1405					D9121	
SD1406					D9122	
SD1407					D9123	
SD1408					New	
SD1409 to SD1430					New	
SD1431					New	

(14) Process control instructions

Table App. 3.15. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD1500 SD1501	Basic period	Basic period time	Set the basic period (1 second units) use for the process control instruction using floating point data. Floating point data = SD1501 SD1500	U	New	Q4AR QnPH
SD1502	Process control instruction detail error code	Process control instruction detail error code	Shows the detailed error contents for the error that occurred in the process control instruction.	S (Error)	New	
SD1503	Process control instruction generated error location	Process control instruction generated error location	Shows the error process block that occurred in the process control instruction.	S (Error)	New	
SD1506 SD1507	Dummy device	Dummy device	Used to specify dummy devices by a process control instruction.	U	New	QnPH QnPRH

(15)For redundant systems (Host system CPU information *1)

SD1510 to SD1599 are only valid for redundant systems.

They are all set to 0 for stand-alone systems.

Table App. 3.16. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD1512	Operation mode during CPU module start up	Hot start switch power out time	Shows the power out time (S) during the automatic switch from hot start to initial start in the operation mode when the CPU module is started up.	S (Initial)	New	Q4AR
SD1585	Redundant system LED status	4 LED states • BACKUP • CONTROL • SYSTEM A • SYSTEM B	The LED status for BACKUP, CONTROL, SYSTEM A, SYSTEM B is stored in the following format: b15 to b10 b9 b8 b7 b6 b5 b4 b3 b2 to b0 SYSTEM B 0: Off 1: On 2: Flicker SYSTEM A 0: Off 1: On 2: Flicker CONTROL 0: Off 1: On BACKUP 0: Off 1: On (red) 2: Flicker (red) 3: On (green) 4: Flicker (green) 5: On (orange-yellow) 6: Flicker (orange-yellow)	S (status change)	New	QnPRH
SD1588	Reason(s) for system switching	Reason(s) for system switching that occurred in host station	Stores the reason(s) for system switching on the host system. The following values are stored corresponding to the methods for system switching: Initialized to 0 when the power supply is switched off and then on or the RESET switch is set to the RESET position and then to the neutral position. 0: Initial value (control system has not been switched) 1: Power off, Reset, H/W failure, WDT error, 2: CPU stop error (except WDT) 3: System switching request from network module 16: System switching dedicated instruction 17: System switching request from GX Developer	S (when condition occurs)	○	

*1: The information of the host CPU module is stored.

Table App. 3.16. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD1589	Reason(s) for system switching failure conditions	Reason(s) for system switching failure No.	- Stores the reason(s) for system switching failure. 0: System switching normal (default) 1: Tracking cable is not connected , tracking cable error, FPGA circuit failure. 2: H/W failure, power-OFF, Reset, WDT error on the standby system 3: H/W failure, power-OFF, Reset, WDT error on the Control system 4: Tracking data transfer initialization 5: Communication timeout 6: Serious error(except WDT error) on the Standby system 7: There is difference between both systems (detected as Backup mode only) 8: During memory copy from control system to standby system 9: During online program change 10: During detection of intelligent function module failure on the standby system 11: System switching being executed - Resets to "0" when host system is powered on. - Resets to "0" once system has been switched successfully.	S(when system is switched)	○	QnPRH
SD1590	Switch request network No.	Request source network No.	Stores the request source at work No. when the SM1590 is turned on.	S (Error)	New	Q4AR
	Network module head address, which requested system switching	Network module head address, which requested system switching	- Stores head address of network module which a system switch request was initiated. - Turns off automatically by system, after network error is reset by user. SD1590 Each bit 0:OFF 1:ON Module 0: CPU module is invalid as it is 2-slot model. Module 1: Module on the right side of the CPU module to Module11: Module at the rightmost end of the 12-slot base (Q312B) - Please refer to SD1690 which stores the corresponding head address of network module on other system.	S (Error/Status change)	New	QnPRH
SD1595	Memory copy target I/O number	Memory copy target I/O number	Stores the memory copy target I/O No.(Standby system CPU module: 3D1H) of before SM1595 is turned from OFF to ON.	U	New	
SD1596	Memory copy status	Memory copy status	- Stores the execution result of Memory copy function. 0 : Memory copy successfully completed 4241H : Standby system power supply off 4242H : Tracking cable is disconnected or is damaged 4247H : Memory copy function is being executed 4248H : Unsupported memory copy destination I/O Number	S (Status change)	New	

(16)For redundant systems (Other system CPU information *1)

SD1600 to SD1659 is only valid during the back up mode for redundant systems, and refresh cannot be done when in the separate mode.

SD1651 to SD1699 are valid in either the backup mode or separate mode.

When a stand-alone system SD1600 to SD1699 are all 0.

Table App. 3.17. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU SD□□*2	Corresponding CPU
SD1600	Diagnosis error	Diagnosis error No.	- Stores as BIN code the error No. of the error that occurred during the other system CPU module diagnosis. - Stores the latest error currently occurring.	S (Each END)	SD0	Q4AR
SD1601	Diagnosis error occurrence time	Diagnosis error occurrence time	- SD1600 stores the updated date and time. - Stores each of the BCD two digits. - Refer to SD1 to SD3 for the storage status. (SD1→SD1601, SD2→SD1602, SD3→SD1603)	S (Each END)	SD1 to SD3	
SD1602						
SD1603						
SD1604	Error information classification	Error information classification	- Stores the error comment information/individual information classification code. - Refer to SD4 for the storage status.	S (Each END)	SD4	
SD1605	Error common information	Error common information	- Stores the common information for the error code. - Refer to SD5 to SD15 for the storage status. (SD5→SD1605, SD6→SD1606, SD7→SD1607, SD8→SD1608, SD9→SD1609, SD10→SD1610, SD11→SD1611, SD12→SD1612, SD13→SD1613, SD14→SD1614, SD15→SD1615)	S (Each END)	SD5 to SD15	
SD1606						
SD1607						
SD1608						
SD1609						
SD1610						
SD1611						
SD1612						
SD1613						
SD1614						
SD1615						
SD1616	Error individual information	Error individual information	- Stores the individual information for the error code. - Refer to SD16 to SD26 for the storage status. (SD16→SD1616, SD17→SD1617, SD18→SD1618, SD19→SD1619, SD20→SD1620, SD21→SD1621, SD22→SD1622, SD23→SD1623, SD24→SD1624, SD25→SD1625, SD26→SD1626)	S (Each END)	SD16 to SD26	
SD1617						
SD1618						
SD1619						
SD1620						
SD1621						
SD1622						
SD1623						
SD1624						
SD1625						
SD1626						
SD1650	Switch status	CPU module switch status	- Stores the CPU module switch status. - Refer to SD200 for the storage status. (SD1650→SD200)	S (Each END)	SD200	
SD1651	LED status	CPU module-LED status	- Stores the CPU module's LED status. - Shows 0 when turned off, 1 when turned on, and 2 when flicking. - Refer to SD201 for the storage status. (SD1651→SD201)	S (Each END)	SD201	
SD1653	CPU module operation status	CPU module operation status	- Stores the CPU module operation status. - Refer to SD203 for the storage status. (SD1653→SD203)	S (Each END)	SD203	

*1 : Stores other system CPU module diagnostics information and system information.

*2 : Shows the special register (SD□□) for the host system CPU module.

Table App. 3.17. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU SD□□*2	Corresponding CPU
SD1600	System error information	System error information	- If an error is detected by the error check for redundant system, the corresponding bit shown below turns ON. That bit turns OFF when the error is cleared after that. SD1600 b15 Fixed to 0 b2 b1 b0 Each bit 0: OFF 1: ON Tracking cable is not connected or damaged Power-OFF, reset, watchdog timer error or hardware failure occurred in other system Other system stop error (except watchdog timer error) Bit turns on when failing to connect with other system. The following causes are shown below: - Tracking H/W failure - Host system WDT error - Cannot recognize other system therefore causing error - If any of b0, b1, b2 and b15 is ON, the other bits are all OFF. - In the debug mode, b0, b1, b2 and b15 are all OFF.	S(Every END)	—	QnPRH
SD1601	System switching results	System switching results	Stores the reasons for system switching. - Stores the reasons for system switching into SD1601 of both systems when system switching occurred. - Initialized to 0 at power OFF to ON/reset to unreset. - The following shows values stored into this register. 0: Initial value (System switching has not occurred) 1: Power-OFF, Reset, H/W failure, WDT error, (*) 2: CPU stop error (except WDT) 3: System switching request by network module 16: System switching dedicated instruction 17: System switching request from GX Developer *: When the system is switched by the power OFF/reset of the control system, "1" is not stored into SD1601 of the new standby system.	S(when system is switched)		
SD1602	System switching dedicated instruction parameter	System switching dedicated instruction parameter	- Stores the parameters for system switching dedicated instruction SP.CONTSW. (The parameters (SD1602) for SP.CONTSW are stored in both systems A&B) - SD1602 is only valid when "16" is stored in SD1601. - This SD1602 is updated once system switch instruction SP.CONTSW is activated.	S(when system is switched)		
SD1610	Other system diagnostic error	Diagnostic error code	- The error value sorted in BIN code. - Stores SD0 of the other system CPU module	S(Every END)	SD0	
SD1611	Other system diagnostic error occurrence time	Diagnostic error occurrence time	- Stores the date and time when diagnostics error occurred corresponding to error code stored in SD1610. - Data format is the same as SD1 to SD3. - Also, stores the value to SD1 to SD3.	S(Every END)	SD1 to SD3	
SD1612						
SD1613						
SD1614	Other system error information category	Error information category code	- Stores the category code corresponding to the error comment information/individual information code. - Data format is the same as SD4. - Also, stores the value to SD4.	S(Every END)	SD4	
SD1615 to SD1625	Other system error common information	Error common information	- Stores the common information corresponding to the error code stored in this system CPU. - Data composition is the same as SD5 to SD15. - Also, stores the value to SD5 to SD15.	S(Every END)	SD5 to SD15	
SD1626 to SD1636	Other system error individual information	Error individual information	- Stores the individual information corresponding to the error code stored in this system CPU. - Data composition is the same as SD16 to SD26. - Also, stores the value to SD16 to SD26.	S(Every END)	SD16 to SD26	
SD1649	Standby system error cancel command	Error code of error to be cleared	- Stores the error code of the error to be cleared by clearing a standby system error. - Stores the error code of the error to be cleared into this register and turn SM1649 from OFF to ON to clear the standby system error. - The value in the lowest digit (1 place) of the error code is ignored when stored into this register. (By storing 4100 in this register and resetting the error, errors 4100 to 4109 can be cleared.)	S(Every END)	—	

*2: Shows the special register (SD□□) for the host system CPU module.

Table App. 3.17. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU SD□□*2	Corresponding CPU
SD1650	Other system operating information	Other system operating information	Stores the operation information of the other system CPU module in the following format. "00FFH" is stored when a communication error occurs, or when in debug mode. b15 to b8 b7 to b4 b3 to b0 SD1650 0 0: No error 1: Continue error 2: Stop error F: Communication with other system disabled (*) 0: RUN 2: STOP 3: PAUSE F: Communication with other system disabled (*) *: Communication with other system disabled, debug mode Note : A communication error is caused by the following:. - When the power supply is switched off, or when the other system is reset. - H/W error occurs on either of system A or B. - WDT error occurs. - Tracking cable is not connected. - Tracking cable is disconnected or damaged.	S(Every END)	—	QnPRH
SD1690	Network module head address, which requested system switching on host (control) system	Network module head address, which requested system switching on host (control) system	- Stores head address of network module which a system switch request was initiated, using the following format. - Turns off automatically by system, after network error is reset by user. b15 to b11 to b1 b0 SD1690 0 0/1 ... 0/1 0 Each bit 0: OFF 1: ON Module 0: CPU module is invalid as it is 2-slot model Module 1: Module on the right side of the CPU module to Module 11: Module at the rightmost end of the 12-slot base (Q312B) Please refer to SD1590 which stores the corresponding head address of network module on host system.	S(Every END)		

*2 : Shows the special register (SD□□) for the host system CPU.

(17)For redundant systems (Trucking)

SD1700 to SD1779 is valid only for redundant systems.

These are all 0 for stand-alone systems.

Table App. 3.18. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD1700	Tracking error detection count	Tracking error detection count	When the tracking error is detected, count is added by one.	S(Error)	New	Q4AR QnPRH
SD1710	Waiting time for online program change (standby system)	Waiting time for online program change (standby system)	- Set in seconds the waiting time of the standby system CPU module from when online program change to the control system CPU module is completed by the online program change for redundancy function until the online program change to the standby system CPU module starts. - If no online program change request is issued to the standby system CPU module within the preset time after completion of the online program change to the control system CPU module, both system CPU modules judge it as the failure of the online program change for redundancy. In this case, both system CPU modules resume the consistency check between system A & B suspended during the online program change. Also, the control system CPU module is set to accept a new request of online program change for redundancy. - When both systems are powered on, 90 seconds are set to SD1710 as the default value. - Set the value within the range 90 to 3600 seconds. When the setting is 0 to 89 seconds, it is regarded as 90 seconds for operation. If the setting is outside the allowed range, it is regarded other than 0 to 3600 seconds for operation. - The waiting time for a start of online program change to the standby system CPU module is checked according to the SD1710 setting during online change of multiple blocks and online change of batch of files for redundancy.	U/ S (Initial)		QnPRH

(18) Redundant power supply module information

SD1780 to SD1789 are valid only for a redundant power supply system.

The bits are all 0 for a singular power supply system.

Table App. 3.19. Special register

Number	Name	Meaning	Explanation	Set by (When Set)	Corres- ponding ACPU D9□□□	Corresponding CPU
SD1780	Power supply off detection status	Power supply off detection status	- Stores the status of the redundant power supply module with input power OFF in the following bit pattern. - Stores 0 when the main base unit is not the redundant power main base unit (Q38RB). - When configuring multiple CPU, the status is stored to 1st CPU module.	S(Every END)	New	
SD1781	Power supply failure detection status	Power supply failure detection status	- Stores the failure detection status of the redundant power supply module in the following bit pattern. (The corresponding bit is cleared to 0 when the input power to the faulty redundant power supply module is switched OFF after detection of the redundant power supply module failure.) - Stores 0 when the main base unit is not the redundant power main base unit (Q38RB). - When configuring multiple CPU, the status is stored to 1st CPU module.	S(Every END)	New	Qn(H) ^{*2} QnPH ^{*2} QnPRH Rem
SD1782	Momentary power failure detection counter for power supply 1 ^{*1}	Momentary power failure detection count for power supply 1	- Counts the number of times of momentary power failure of the power supply 1/2. - Monitors the status of the power supply 1/2 mounted on the redundant power main base unit (Q38RB) and counts the number of times of momentary power failure. - Status of power supply 1/power supply 2 mounted on the redundant extension base unit is not monitored. - When the CPU module starts, the counter of the power supply 1/2 is cleared to 0.	S(Every END)	New	
SD1783	Momentary power failure detection counter for power supply 2 ^{*1}	Momentary power failure detection count for power supply 2	- If the input power to one of the redundant power supply modules is turned OFF, the corresponding counter is cleared to 0. - The counter is incremented by 1 every time the momentary power failure of the power supply 1/2 is detected. (0 to 65535: When the count exceeds 65535, it starts with 0.) - Stores 0 when the main base unit is not the redundant power main base unit (Q38RB). - When configuring multiple CPU, the status is stored to 1st CPU module.	S(Every END)	New	

*1: The "power supply 1" indicates the redundant power supply module (Q64RP) mounted on the POWER 1 slot of the redundant base unit (Q38RB/68RB/Q65WRB).
The "power supply 2" indicates the redundant power supply module (Q64RP) mounted on the POWER 2 slot of the redundant base unit (Q38RB/68RB/Q65WRB).

*2: The module whose first 5 digits of serial No. is 04012 or later.
However, for the multiple CPU system configuration, this applies to all CPU modules whose first 5 digits of serial No. are 07032 or later.

APPENDIX 4 PRECAUTIONS FOR UTILIZING THE EXISTING MELSEC-A SERIES PROGRAM FOR QnACPU

To utilize a sequence program, created for AnNCPU, AnACPU, or AnUCPU, for QnACPU, convert it using the "A→QnA Conversion" option of the "Option" menu in the file maintenance mode of the GPP function.

For details on the GPP function operations, refer to the GX Developer Operating Manual or SW□IVD-GPPQ Operating Manual (Offline).

For details on instructions and devices, refer to the QCPU (Q mode)/QnACPU Programming Manual (Common Instructions).

The instructions, devices, and comments, etc. indicated below may require modification in each mode after conversion.

Appendix 4.1 Instructions

An□CPU Instruction	Instruction after A→QnA Conversion	Corrective Action
BMOVR instruction Program example: LEDA BMOVR LEDC D10 LEDC D100 SUB K10 LEDR	OUT SM1255 LEDC D10 LEDC D100 OUT SM1255 LEDR	Modify the instruction to a BMOV instruction. BMOV ZR100 ZR1000 K10
BXCHR instruction Program example: LEDA BXCHR LEDC D10 LEDC D100 SUB K10 LEDR	OUT SM1255 LEDC D10 LEDC D100 OUT SM1255 LEDR	Modify the instruction to a BXCH instruction. BXCH ZR100 ZR1000 K10
CHG instruction	OUT SM1255	Since the QnACPU does not have the main/subsequence program system, it has no CHG instructions. Delete OUT SM1255 as it is not necessary. Modify the main/subsequence program after conversion and set new parameters. (Refer to Appendix 4.5.)
CHK instruction Program example: CHK M10 X100	CHK	Refer to Appendix 4.12
CLC instruction Program example: CLC	RST SM1012	Modify the instruction to SM700, special relay for carry flag. RST SM700
AnA/AnUCPU dedicated instruction IX instruction	OUT SM1255	Refer to Appendix 4.12

An□CPU Instruction	Instruction after A→QnA Conversion	Corrective Action
LEDA instruction (excluding dedicated instructions for AnACPU, AnUCPU) Program example: LEDA ABCDEFGH	OUT SM1255	Modify the instruction to an LED instruction. \$MOV "ABCDEFGH" D0 \$MOV "IJKLMNOP" D10 \$+ D0 D10 D20 LED D20
LEDB instruction (excluding dedicated instructions for AnACPU, AnUCPU) Program example: LEDB IJKLMNOP	OUT SM1255	LED display is performed after adding the right 8 characters and the left 8 characters.
LRDP instruction Program example: LRDP K3 D10 D100 K10	OUT SM1255	Modify the instruction to a ZNRD instruction. J.ZNRD J0 K3 D10 D100 K10 M0
LWTP instruction Program example: LWTP K3 D10 D100 K10	OUT SM1255	Modify the instruction to a ZNWR instruction. J.ZNWR J0 K3 D10 D100 K10 M0
OUT instruction Program example: The number of counter points or the device by which the set value is used is set by parameter. Number of counter points: 512 Setting val. stored dev. start: D3000 OUT C0 K10 OUT C256 D3000	OUT C0 K10 OUT C256 D3000	After conversion, the parameters will be set as defaults, so they must be set again if using an interrupt counter.
RFRP instruction Program example: RFRP H100 K10 W100 K10	OUT SM1255	Modify the instruction to an RFRP instruction for QnACPU. U.RFRP U10 K10 W100 K10 M0
RTOP instruction Program example: RTOP H100 K10 W100 K10	OUT SM1255	Modify the instruction to an RTOP instruction for QnACPU. U.RTOP U10 K10 W100 K10 M0
SCMP instruction Program example: LEDA SCAP LEDC D10 LEDC D100 LEDC M0 LEDR	OUT SM1255 LEDC D10 LEDC D100 LEDC M0	Modify the instruction to an instruction using AND\$= and OUT instructions. AND\$= D0 D100 OUT M0

An□CPU Instruction	Instruction after A→QnA Conversion	Corrective Action
SEG instruction (When used as a partial refresh instruction) Program example: SET M9052 SEG K4Y10 K4B1	SET SM1052 SEG K4Y10 K4B1	Modify the instruction to an RFS instruction. RFS Y10 H8
STC instruction Program example: STC	SET SM1012	Modify the instruction to SM700, special relay for carry flag. SET SM700
SUB instruction	OUT SM1255	As the QnACPU cannot store any microcomputer program, it has no SUB instructions. Delete OUT SM1255 as it is not necessary. Change the microcomputer program for the AnNCPU or A3HCPU to the sequence program using QnACPU instructions. (Refer to Appendix 4.6.)
ZRRD instruction Program example: DMOV K8000 D9036 LEDA ZRRD	DMOV K8000 SD1036 OUT SM1255	Modify the instruction to an MOV instruction. MOV ZR8000 SD718 SD718 is the device resulting from converting accumulator A0.
ZRWR instruction Program example: DMOV K8000 D9036 LEDA ZRWR	DMOV K8000 SD1036 OUT SM1255	Modify the instruction to an MOV instruction. MOV SD718 ZR8000 SD718 is the device resulting from converting accumulator A0.

(a) Instructions for which program modification is unnecessary after conversion

An□CPU Instruction	Instruction after A→QnA Conversion
ASC instruction Program example: ASC ABCDEFGH D10	\$MOV ABCDEFGH D10 Note: Since the \$MOV instruction has 00H appended at the end, 5 data register words (for 9 characters) must be secured.
DFLOAT instruction Program example: LEDA DFLOAT LEDC D10 LEDC D100 LEDR	DFLT D10 D100
DOUT instruction Program example: LEDA DOUT LEDC Y10 LEDR	OUT DY10
DRCL instruction Program example: DRCL K8	DRCL SD718 K8 SD718 is the device resulting from converting accumulator A0.
DRCR instruction Program example: DRCR K8	DRCR SD718 K8 SD718 is the device resulting from converting accumulator A0.
DROL instruction Program example: DROL K8	DROL SD718 K8 SD718 is the device resulting from converting accumulator A0.
DROR instruction Program example: DROR K8	DROR SD718 K8 SD718 is the device resulting from converting accumulator A0.
DRST instruction Program example: LEDA DRST LEDC Y10 LEDR	RST DY10

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An□CPU Instruction	Instruction after A→QnA Conversion
ROR instruction Program example: ROR K8	ROR SD718 K8 SD718 is the device resulting from converting accumulator A0.
SADD instruction Program example: LEDA SADD LEDC D10 LEDC D100 LEDC D200 LEDR	\$+ D10 D100 D200
SER instruction Program example: SER D10 D100 K5	SER D10 D100 SD718 K5 SD718 is the device resulting from converting accumulator A0.
SMOV instruction Program example: LEDA SMOV LEDC D10 LEDC D100 LEDR	\$MOV D10 D100
SUM instruction Program example: SUM D10	SUM D10 SD718 SD718 is the device resulting from converting accumulator A0.
ZRRDB instruction Program example: DMOV K8000 D9036 LEDA ZRRDB	DMOV K8000 SD1036 ZRRDB SD1036 SD718 SD1036 is the device resulting from converting the special register D9036. SD718 is the device resulting from converting accumulator A0.
ZRWRB instruction Program example: DMOV K8000 D9036 LEDA ZRWRB	DMOV K8000 SD1036 ZRWRB SD1036 SD718 SD1036 is the device resulting from converting the special register D9036. SD718 is the device resulting from converting accumulator A0.

An□CPU Instruction	Instruction after A→QnA Conversion
AnA/AnUCPU dedicated instruction LEDA/LEDB instruction name SUB/LEDC device 1 SUB/LEDC device n LEDR Program example 1: SIN instruction LEDA SIN LEDC D10 LEDC D100 LEDR Program example 2: DSER instruction LEDA DSER LEDC D10 LEDC D100 SUB K5 LEDR	Instruction name device 1 device n SIN D10 D100 DSER D10 D100 SD718 K5 SD718 is the device resulting from converting accumulator A0.
AnA/AnUCPU special function module dedicated instruction LEDA/LEDB instruction name SUB/LEDC device 1 SUB/LEDC device n LEDR Program example: LEDA SVWR1 SUB H2 LEDC D10 LEDR	Enter "G." before the instruction. G. instruction name device Un device n G.SVWR1 U2 D10
AnA/AnUCPU data link dedicated instruction LEDA/LEDB instruction name SUB/LEDC device 1 SUB/LEDC device n LEDR Program example: LEDA LRDP SUB K12 LEDC D10 LEDC D100 SUB K5 LEDC M0 LEDR	Enter "J." before the instruction. J. instruction name <u>J0</u> device 1 device n ↑ Network for using MELSECNET II OUT SM1255 J.ZNRD J0 K12 D10 D100 K5M0

An□CPU Instruction	Instruction after A→ QnA Conversion
Index register Z, Z1 to Z6, V, V1 to V6 Index register double word $\frac{Vn}{Upper} \cdot \frac{Zn}{Lower}$	$Z \rightarrow Z0$ $Z1 \text{ to } Z6 \rightarrow Z1 \text{ to } Z6$ $V \rightarrow Z7$ $V1 \text{ to } V6 \rightarrow Z8 \text{ to } Z13$ $\frac{Zn+1}{Upper} \cdot \frac{Zn}{Lower}$ If an index register is used for destination of double word operation or single word multiplication/division, the relation of upper and lower levels may be broken, causing a problem.

Appendix 4.2 Devices

(a) Only devices within the QnACPU range are converted.

An□CPU Device		Device after A→QnA Conversion
X□□□		Same as to left
Y□□□		Same as to left
M□□□	M/L/S is determined by the parameter settings.	Same as to left
L□□□		Same as to left
S□□□		Same as to left (Correct to M□□□.)
M9000 to M9255		SM1000 to SM1255
B□□□		Same as to left
T (low-speed timer)	Low-speed/high-speed/retentive is determined by parameter setting.	Same as to left
T (high-speed timer)		Same as to left
T (retentive timer)		ST□□□
C□□□		Same as to left
F□□□		Same as to left
D□□□		Same as to left
D9000 to D9255		SD1000 to SD1255
W□□□		Same as to left
R□□□		Same as to left
Z□		Z → Z0 Z1 to Z6→ Z1 to Z6
V□		V → Z7 V1 to V6→ Z8 to Z13
A0,A1		SD718,SD719
P□□□		Same as to left*
I□□		Same as to left
N□		Same as to left
K□□□		Same as to left
H□□□		Same as to left

REMARK

* When P254 is used as the CHK instruction pointer, P254 can be converted to P254 as is. (Refer to Appendix 4.12.)

- (b) Devices that are outside the QnACPU range are converted to SM1255 if they are bit devices and to SD1255 if they are word devices.

Appendix 4.3 Parameters

The following parameter settings only are converted to QnACPU use.

- Latch range setting
Converted to the "latch clear key valid" range.
The latch clear key invalid range is made blank (no setting).
- MELSECNET (II, /10) setting
For the MELSECNET setting when the ACPU is an AnN or AnA, the number of modules are stored after conversion, but the network refresh parameters are not converted.
- I/O assignment
Only the head I/O No. is made blank; all other items are converted.
- MELSECNET/MINI auto refresh setting
If only I/O assignment was set in the parameters and MELSECNET/MINI auto refresh settings have not been made, the MELSECNET/MINI data link operates with the default values.

The following items are set for the QnACPU default. If settings have been made, make the settings again.

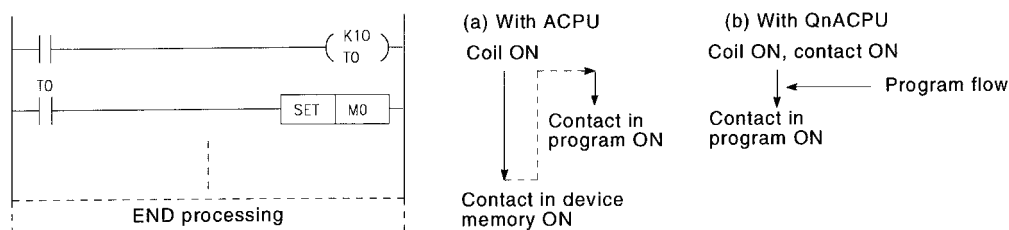
- RUN-PAUSE contacts : No setting
- Output at STOP → RUN : Before operation
- Interrupt counter No. : No setting
- WDT setting : 200ms
- Operation mode when
there is an error : STOP (All items)

Appendix 4.4 Timer and Interrupt Counter Operations

(1) Timer

- (a) The ACPU turns timer coils ON/OFF on execution of the OUT instruction, and updates timer current values and turns contacts ON/OFF on execution of the END instruction. In contrast, the QnACPU turns timer coils ON/OFF, updates current values, and turns contacts ON/OFF on execution of the OUT instruction. Note that after conversion, the turning of contacts ON/OFF may be up to one scan faster.

Example: Timing for turning contact ON



In the case of ACPU, a timer contact will turn ON quickly if it is located in the first step. In the case of QnACPU, it will turn ON quickly if it is located in the step following OUT T.

- (b) Note that processing differs as follows when the set value of a timer is set to K0:
- For ACPU, count is in infinite units (timer does not count up).
 - For QnACPU, the timer counts up instantaneously.

(2) Interrupt counter

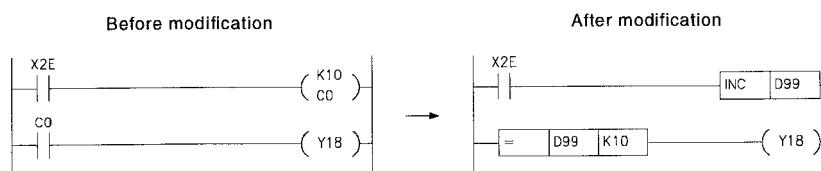
Interrupt counters for QnACPU count the number of interrupt occurrences. However, the counter contact does not turn ON even when the count has reached the set value.

The operation of interrupt counters for ACPU differs according to the CPU type.

- (a) Interrupt counters for A3HCPU, AnACPU, or AnUCPU count the number of interrupts occurrences. When the count reaches the set value, the counter contact turns ON.

In order to achieve the same operation as with interrupt counters for A3HCPU, AnACPU, and AnUCPU when using a QnACPU, the program must be modified after conversion.

An example modification is shown below.



- (b) Interrupt counters for AnCPU and AnNCPU operate as counters used in interrupt programs.

To achieve the same operation as with interrupt counters for AnCPU or AnNCPU when using a QnACPU, the program modification is not needed after conversion.

When ordinary counters are used in an interrupt program with QnACPU, they operate in the same way as with AnNCPU.

Appendix 4.5 Sequence Programs, Statements, Notes

After conversion by A → QnA conversion, sequence programs are stored in the set file. If a subsequence program is included, the main/subsequence program must be modified. There are two types of modification, as indicated below:

- (a) When executing the main sequence program and subsequence program alternately, modify the parameters and programs as follows.

Modification of parameters

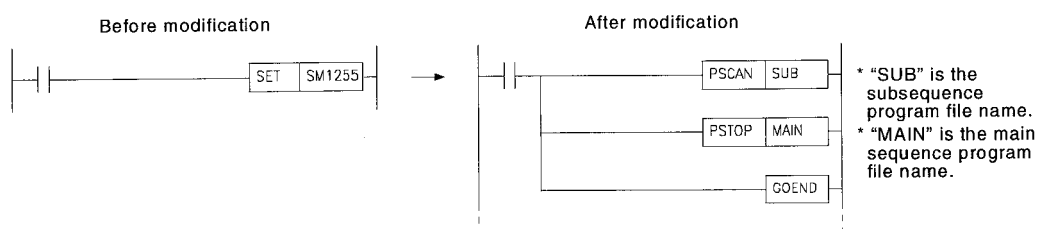
Set file names of the main sequence program and subsequence program in program setting in "Auxiliary setting" in the parameter mode. Select scan execution for the main sequence program and stand-by execution for the subsequence program.

Modification of the sequence program

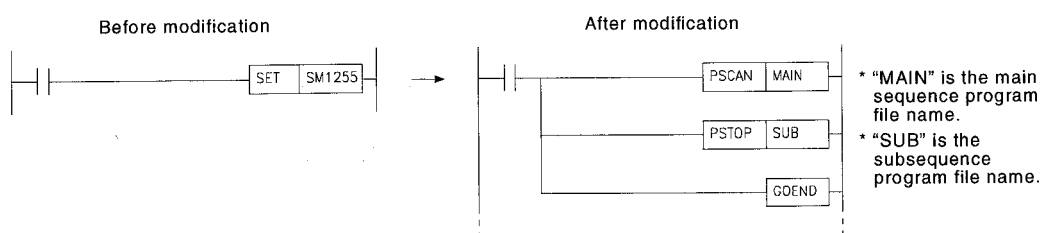
- The CHG instruction that switches between main sequence and subsequence programs is converted to OUT SM1255 after A → QnA conversion. Modify this OUT SM1255 to the PSCAN instruction which converts another sequence program to an scan execution type program.
- Next, add the GOEND instruction that executes a jump to the END instruction to the following step.
- Next, add the PSTOP instruction, which converts another sequence program to a stand-by execution type program, to the first step of the sequence program.

This enables execution of the subsequence program from the main sequence program, and disables execution of the main sequence program when the subsequence program is executed.

- Main sequence program



- Subsequence program



- (b) To execute the main sequence program and subsequence program serially as one program, modify the parameters and program as follows.

Modification of parameters

Set the file names in the order of main sequence program and subsequence program in program setting in "Auxiliary setting" in the parameter mode. Select scan execution as the execution type for both the main sequence program and the subsequence program.

Modification of the sequence program

- The CHG instruction that switches between main sequence and subsequence programs is converted to OUT SM1255 after A → QnA conversion. Delete it as it is not required for QnACPU.
- If the same interrupt program or pointer is used for the main sequence program or subsequence program, use only one interrupt program or pointer.

REMARK

An ACPU executes END processing on switching from execution of the main sequence program to execution of the subsequence program, and also executes END processing after execution of the subsequence program.

Note that END processing is executed only after execution of the second program when a QnACPU executes two programs consecutively.

Statements and notes are entered in the sequence program file after A → QnA conversion.

No modification is required after conversion.

Appendix 4.6 Microcomputer programs

Microcomputer programs and utility software packages cannot be converted as the QnACPU has no microcomputer mode.

When a microcomputer program or utility software package is used with the ACPU, a SUB instruction (microcomputer program call instruction) is written in the sequence program to execute it. The SUB instruction is converted to OUT SM1255 after A → QnA conversion; delete it as it is not necessary.

In the case of user-created microcomputer programs, convert processing contents of the microcomputer programs to sequence programs using operation instructions added for QnACPU.

When using a utility software package of the following, convert processing contents of the utility software package to a sequence program using operation instructions added for QnACPU.

- SW□□□-AD57P Refer to the QnACPU Programming Manual (AD57 Instructions).
 - SW□□□-UTLP-FN0 Refer to the QCPU (Q mode)/QnACPU Programming Manual (Common Instructions).
 - SW□□□-UTLP-FN1 Refer to the QCPU (Q mode)/QnACPU Programming Manual (Common Instructions).
 - SW□□□-UTLP-PID Refer to the QCPU (Q mode)/QnACPU Programming Manual (PID Control Instructions).
 - SW□□□-SIMA
 - SW□□□-UTLP-FD1
 - SW□□□-SAPA
- } Unusable

Appendix 4.7 Comments

Conversions are made for the device range of QnACPU. Devices outside the range are not converted.

Appendix 4.8 Constant Scan Function, Error Check Function

When using the constant scan function or error check function for ACPUs, special registers or special relays are set.

In contrast, for QnACPUs, these functions are set with parameters. To use these functions after conversion, make settings in "PLC RAS" in the parameter mode.

Appendix 4.9 I/O control mode

The I/O control mode for QnACPU is refresh mode (direct I/O is enabled depending on the device).

- As the I/O control mode for AnACPU and AnUCPU is the refresh mode as with QnACPU, there are no problems with the input timing of inputs (X) or the output timing of outputs (Y).
- In the case of AnCPU, AnNCP, and A3HCP, I/O control mode is fixed or selected to direct mode, and the input timing for inputs (X) and output timing for outputs (Y) differs from that for the refresh mode.

The I/O control mode for each CPU module is shown below.

Model Name	I/O control Method
AnCPU	Fixed as the direct mode
AnNCP	Direct mode or refresh mode is selected with the switch on the module.
A3HCP	Direct mode or refresh mode is selected by parameter settings.
AnACPU	Fixed as the refresh mode
AnUCPU	Fixed as the refresh mode

- Modifying programs that generate pulses from SET/RST instructions by using direct devices

Modify programs which, in the direct mode, output pulse output to the external using SET/RST instructions to programs that use direct output devices for QnACPU.

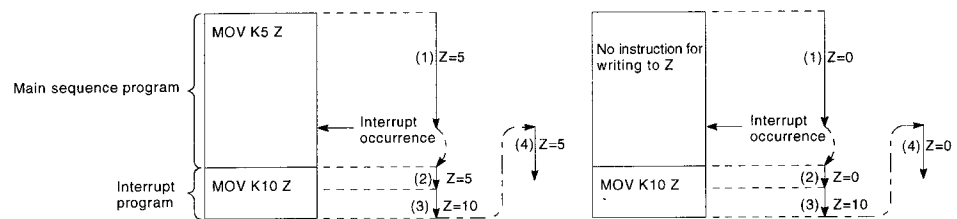
Appendix 4.10 Data Link System

- AnUCPU data link systems
The network settings in the AnUCPU parameters can be converted by A → QnA conversion. Parameter modifications after conversion are not needed.
- CPU modules other than AnUCPU
The link settings in the CPU module parameters cannot be converted by A → QnA conversion. Link settings must be made in the parameters after conversion.

Appendix 4.11 Index Register Processing

For QnACPU, the contents of index registers change when program processing transfers between the main sequence program and interrupt programs.

- Transfer of program processing from main sequence program to interrupt program
The contents of the index registers of the main sequence program are saved, and then these contents are passed to the interrupt program.
- Transfer of program processing from interrupt program to main sequence program
The index registers in the interrupt program are cleared, and the saved main sequence program contents are written to them.



For ACPU, processing differs according to the CPU module type.

- The processing for AnACPU and AnUCPU is the same as for QnACPU, and no program modification is required after conversion.
- In the case of AnCPU, AnNCPU, and A3HCPU, when program processing is transferred from an interrupt program to the main program, the data updated in the interrupt program are passed on to the main program.

When passing a value written to the index register in an interrupt program on to the main sequence program, for example, modify the program so that the value is passed on via a data register.

Appendix 4.12 CHK Instruction, IX Instruction

(1) CHK instruction

The CHK instruction operates as a fault check instruction for QnACPU.

For ACPU, there are two types of processing depending on the CPU type.

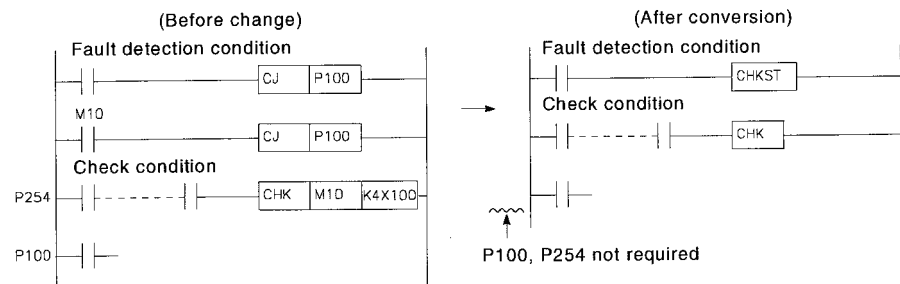
- Fault check AnCPU, AnNCPU (direct I/O control mode),
A3HCPU, AnACPU, AnUCPU
- Bit device output inversion . . . AnNCPU (refresh I/O control mode)

After conversion, program modification is required for each processing.

[For fault check]

Modify the CJ instruction in the step before the CHK instruction to a CHKST instruction.

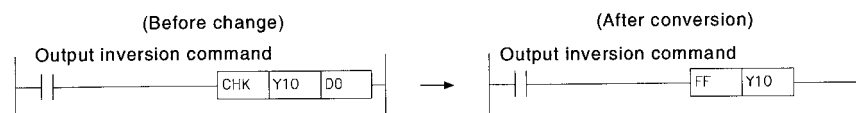
The CHK instruction pointer (P254) and the CJ instruction destination pointer are converted to pointers with the same number. As the above pointers are not used for QnACPU, delete them.



[For bit device output inversion]

The QnACPU has the FF instruction for inverting bit device outputs.

Modify the CHK instruction to the FF instruction.



(2) IX instruction

The IX instruction is converted, but not executed. Modify the program so that all the devices that are objects of the IX instruction are subject to indexing.

Appendix 4.13 Accessing File Register R with Instructions

For QnACPU, no error will occur even if an instruction for accessing file registers outside the setting range is executed.

When reading data, FFFFH is stored to the storage device. When writing data, the instruction is executed but no data is stored in the file register.

For ACPU, execution of such an instruction causes an error.

The capacity of file register R is set by parameter. It is therefore necessary to check the capacities of file registers before executing instructions that access file registers, such as the MOV instruction and + instruction.

APPENDIX 5 ERROR CODES RETURNED TO THE REQUEST SOURCE IN GENERAL DATA PROCESSING

With the QnACPU, when an error occurs while general data processing is requested from a peripheral device, a special function module, or a network system, the error code is returned to the source of the general data processing request.

POINT	
	Since this error code is not an error detected by the QnACPU self-diagnostics function, it is not stored to special relay SD0. If the request source is a peripheral device, the message or the error code is displayed. If the request source is a special function module or a network system, the error code corresponding to the requested processing is returned.

Appendix 5.1 Error Codes

The error code's numbers depends on the location where the error has been detected. The correspondences between the locations where errors are detected and the error codes are indicated in the table below.

Location Where an Error is Detected	Error Code	Reference for Error Contents
CPU module	4000H to 4FFFH	App Appendix 5.2
Serial communication module, etc.	7000H to 7FFFH	Serial Communication Module User's Manual, etc.
CC-Link module	B000H to BFFFH	Control & Communication Link System Master/Local Module User's Manual
Ethernet module	C000H to CFFFH	Ethernet Interface Module User's Manual
MELSECNET/10 network module	F000H to FFFFH	For QnA/Q4AR MELSECNET/10 Network System Reference Manual

Appendix 5.2 Error Contents of Error Codes Detected by the CPU Module (4000H to 4FFFH)

The error contents of error codes detected by the CPU module (4000H to 4FFFH), and the messages displayed on the peripheral device are indicated in the table below.

Error Code (Hexadecimal)	Error	Error Contents	Message Displayed at Peripheral Device	Corrective Action
4000H	CPU module- related error	Sum check error	Message (1) is displayed.	Check the connection between the CPU module and connection cable.
4001H		Remote request that cannot be handled is performed.	Message (1) is displayed.	Check the requested remote operation.
4002H		Command to which a global request is not allowed is performed.	Message (1) is displayed.	Check the requested command.
4003H		Since the QnACPU system is protected, the request contents cannot be performed.	Execution is not allowed during system protection.	Turn the QnACPU system protect switch OFF.
4004H		The data volume is too large for the specified request.	Cannot execute in excess of capacity.	Reduce the data volume so that it can be handled with the request.
4005H		Password has not been cancelled.	Password has not been cancelled.	Cancel the set password.
4006H		CID is different from the QnACPU data.	Message (1) is displayed.	Check the CID.
4007H		The QnACPU is not BUSY. (Buffer is not empty.)	Message (1) is displayed.	Re-perform the request after the elapse of an arbitrary time period.
4008H				
4010H	CPU module mode error	The request contents cannot be performed because the QnACPU is in RUN.	Cannot execute when PLC is in RUN mode.	Perform the request after setting the QnACPU to STOP.
4011H		The request contents cannot be performed because the QnACPU is not in STEP-RUN.	Cannot execute while PLC is not in STEP RUN mode.	Perform the request after setting the QnACPU to STEP-RUN.
4012H		The request contents cannot be performed because the QnACPU is in STEP-RUN.	Not executed due to STEP-RUN of PLC.	Perform the request after setting the QnACPU to RUN/STOP.

Error Code (Hexadecimal)	Error	Error Contents	Message Displayed at Peripheral Device	Corrective Action
4021H	CPU module file-related error	Designated drive memory does not exist or is abnormal.	The target drive contains a fault.	Check the status of the designated drive memory.
4022H		The file with designated file name, and file No. does not exist.	The file name does not exist.	Check the designated file name and file No.
4023H		The file name and file No. of the designated file do not match.	Cannot access files.	Delete the file and create a new one.
4024H		The designated file cannot be accessed by the user.	This file cannot be handled.	Do not access the designated file.
4025H		The designated file is processing a request from another source.	Alert (1) is displayed.	Forcibly perform the request. Or perform the request again after other processing has completed.
4026H		The keyword set for target drive memory has to be designated.	Keyword doesn't match.	Access by designating the keyword set for the target drive memory.
4027H		The designated range exceeds the file range.	File capacity is not enough.	Check the designated range, and access within the permissible range.
4028H		The same file has already existed.	Alert (2) is displayed.	Forcibly perform the request. Or change the file name and then perform the request.
4029H		The capacity of the designated file is not secured.	File capacity is not enough.	Review the capacity of the designated file. Or sort the designated drive memory and re-perform.
402AH		The designated cluster No. does not exist.	Cannot access files.	Check the designated cluster No., and access by designating a cluster No. within the number of clusters of the designated drive memory.
402BH		The request contents cannot be performed with the designated drive memory.	Cannot access files.	Do not make requests which caused an error to the designated drive memory.
402CH		The request contents cannot be currently performed.	Cannot access files.	Re-perform after the elapse of an arbitrary time period.
4030H	CPU module device designation error	The designated device name cannot be handled.	Device is invalid.	Check the designated device name.
4031H		The designated device No. is out of range.	Device No. is out of range.	Check the designated device No.
4032H		A mistake in the designated device qualification.	Device is invalid.	Check the method for qualification of the designated device.
4033H		The designated device is for system use and cannot be written to.	Device is invalid.	Do not write data to the designated device, or turn it ON/OFF.

Error Code (Hexadecimal)	Error	Error Contents	Message Displayed at Peripheral Device	Corrective Action
4040H	Special function module designation error	The designated special function module cannot perform the request contents.	The unit does not exist.	Do not make requests which caused an error to the designated special function module.
4041H		Access range exceeds the buffer memory range of the designated special function module.	The # of devices is too large.	Check the head address and number of accessed points, and access within the actual ranges at the special function module.
4042H		Access to the designated special function module is not possible.	The corresponding unit is faulty.	Check if the designated special function module normally operates.
4043H		The special function module is not at the designated position.	The unit does not exist.	Check the head I/O No. of the designated special function module.
4044H		A control bus error has occurred.	The corresponding unit is faulty.	Check if there is a fault in the hardware of the special function module or other modules.
4045H		Setting required for simulation has not been made.	Data error	Make settings for the simulation.
4046H		The head number of the device or the number of device points designated for simulation is not in 16-point units.	Device No. is not in 16 units.	Check the head number and number of device points and then modify them to 16-point units.
4050H	Protect error	Request contents cannot be performed because the write protect switch of the memory card is ON.	Cannot execute as the memory protect switch is ON.	Turn the write protect switch of the memory card OFF.
4051H		The designated device memory cannot be accessed.	Wrong ROM	Check the following and take corrective action. • Whether the memory is usable • Whether the designated drive memory correctly installed
4052H		Data cannot be written to the designated file because its attribute is read only.	Write is prohibited.	Do not write data to the designated file. Or change the file attribute.
4053H		An error occurred when writing data to the designated drive memory.	Cannot write correctly in ROM.	Check the designated drive memory. Or replace the target drive memory and then rewrite the data.
4054H		An error occurred when deleting data from the designated drive memory.	Cannot erase ROM correctly.	Check the designated drive memory. Or replace the target drive memory and then delete the data again.

Error Code (Hexadecimal)	Error	Error Contents	Message Displayed at Peripheral Device	Corrective Action
4060H	Online registration error	The CPU module system area for registering monitor conditions is being used by another device.	Alert (1) is displayed.	When monitoring of the other device has completed, perform the monitoring again. Or increase the system area of the built-in RAM using a format with an option.
4061H		Communications failed.	Not registered.	Re-perform communications.
4062H		Another device is monitoring using the detailed condition for monitoring.	Alert (1) is displayed.	Do not use the detailed condition for monitoring from the designated device. Or cancel the monitoring detailed condition for other device and perform the monitoring again.
4063H		The number of registrations for file lock is greater than 16.	Cannot access files.	Reduce the number of registrations to 16 or less.
4064H		Incorrect setting contents.	Setting is incorrect.	Check the set contents.
4065H		Device I/O information differs from parameters.	Does not match the parameter.	Check the parameters. Or check the data.
4066H		A keyword that differs from the one set for the designated drive memory was specified.	Keyword doesn't match.	Check the designated keyword.
4067H		The designated monitor file has not been secured.	File capacity is not enough.	Secure the monitor file, then perform monitoring.
4068H		The designated command cannot be registered or cancelled since it is in execution.	Unable to execute due to on going process.	Re-perform the command after requests from other devices has been completed.
4069H		Condition has already satisfied at device.	Setting is incorrect.	Check the monitor condition. Or perform monitor registration again and then monitor.
406AH		Drive other than No.1 to 3 has been designated.	Drive specification is incorrect.	Check the designated drive and specifies a correct drive.
4070H	Ladder verification	The program before modification differs from the registered program.	Program does not match.	Check the registered program and match the program to it.

Error Code (Hexadecimal)	Error	Error Contents	Message Displayed at Peripheral Device	Corrective Action
4080H	Other error	Data error	Data is faulty.	Check the requested data contents.
4081H		The searched target cannot be detected.	Cannot find the find target.	Check the data to be searched.
4082H		The designated command cannot be performed since it is in execution.	Unable to execute due to on going process.	Re-perform the command after requests from other devices has been completed.
4083H		An attempt was made to perform a program not registered in the parameters.	Not registered.	Register the program to be performed to the parameters.
4084H		The designated pointer P, I cannot be detected.	Cannot find the find target.	Check the data to be searched.
4085H		Pointer P, I designation is not possible because the program is not registered in the parameters.	Not registered.	Register the program to be performed in the parameters, then designate the pointer P, I.
4086H		An attempt was made to add a pointer P, I that have already existed.	Device ranges are duplicated.	Check the pointer No. to be added and change it.
4087H		The number of pointers designated is too great.	No pointer exists.	Check and correct the designated pointer.
4088H		The designated step No. is not at the head of the instruction.	Execution position is incorrect.	Check and correct the designated step No.
4089H		The END instruction was inserted/ deleted while the CPU module had been in RUN.	Setting is incorrect.	Insert/Delete the instruction after setting the CPU module to STOP.
408AH		The file capacity has been exceeded by performing write during RUN.	File capacity is not enough.	Set the CPU module to STOP and then write the program.
408BH		Cannot perform a remote request.	Data error.	Set the CPU module to the state for performing a remote request, then reissue the request.

Error Code (Hexadecimal)	Error	Error Contents	Message Displayed at Peripheral Device	Corrective Action
4090H	Online registration error during SFC STEP RUN	Too many block break points.	Setting is out of range.	Check and correct the set number.
4091H		The number of registered block break points is incorrect.	Setting is out of range.	Check and correct the set number.
4092H		Too many step break points.	Setting is out of range.	Check and correct the set number.
4093H		The number of registered step break points is incorrect.	Setting is out of range.	Check and correct the set number.
4094H		An attempt was made to perform a request during block continuous processing.	Unable to execute due to on going process.	Reissue the request after the processing has been completed.
4095H		An attempt was made to perform a request during block forced execution processing.	Unable to execute due to on going process.	Reissue the request after the processing has been completed.
4096H		An attempt was made to perform a request during step continuous processing.	Unable to execute due to on going process.	Reissue the request after the processing has been completed.
4097H		An attempt was made to perform a request during step forced execution processing.	Unable to execute due to on going process.	Reissue the request after the processing has been completed.
4098H		An attempt was made to perform a request during one step continuous processing.	Unable to execute due to on going process.	Reissue the request after the processing has been completed.
4099H		An attempt was made to perform a request during one step forced execution processing.	Unable to execute due to on going process.	Reissue the request after the processing has been completed.
409AH		An attempt was made to perform a request during block forced end processing.	Unable to execute due to on going process.	Reissue the request after the processing has been completed.
409BH		An attempt was made to perform a request during step forced end processing.	Unable to execute due to on going process.	Reissue the request after the processing has been completed.
409CH		An attempt was made to perform a request during holding step reset processing.	Unable to execute due to on going process.	Reissue the request after the processing has been completed.
409DH		A block No. with no created block or out-of-range block No. has been designated.	Setting is incorrect.	Check and correct the set contents.
409EH		A step No. for which no step has been created was designated.	Setting is incorrect.	Check and correct the set contents.
409FH		The designated number of cycles is out of range.	Setting is out of range.	Check and correct the set number.

Error Code (Hexadecimal)	Error	Error Contents	Message Displayed at Peripheral Device	Corrective Action
40A0H	SFC device designation error	Out-of-range block No. is designated.	Setting is incorrect.	Check and correct the set contents.
40A1H		Designation exceeds the range for the number of blocks.	Setting is out of range.	Check and correct the set number.
40A2H		Out-of-range step No. is designated.	Setting is incorrect.	Check and correct the set contents.
40A3H		Designation exceeds the range for number of steps.	Setting is out of range.	Check and correct the set number.
40A4H		Out-of-range sequence step No. is designated.	Setting is incorrect.	Check and correct the set contents.
40A5H		The designated device is out of range.	Setting is out of range.	Check and correct the set number.
40A6H		The block designation pattern or step designation pattern was incorrect.	Setting is incorrect.	Check and correct the set contents.
40B0H	SFC file- related error	The designated drive is incorrect.	Setting is incorrect.	Check and correct the set contents.
40B1H		The designated program does not exist.	The file name does not exist.	Check and correct the designated file name.
40B2H		The designated program was not an SFC program.	This file cannot be handled.	Check and correct the designated file name.
40B3H		The SFC dedicated instruction exists in the write during RUN area.	Setting is incorrect.	Check and correct the set contents.
4A00H	Link-related error	The designated station cannot be accessed because no routing parameters have been set to the relevant station.	Routing parameter does not exist.	Set the routing parameters for accessing to the designated station in the relevant station.
4A01H		No network with the No. set in the routing parameters exists.	The network I/O does not exist.	Check and correct the routing parameters set at the relevant station.
4A02H		Cannot access to the designated station.	Link unit error.	Check if an error has occurred at the network module/link module, or if the online state has not been established.
4B00H	Target- related error	An error occurred at the access target station or the relay station.	The corresponding unit is faulty.	Check and correct the error at the designated access target station or the relay station for the access station.

REMARK

(1) Message (1)

Cannot communicate with PC. Error ## = ****

An error code is displayed in ****.

(2) Alert (1)

Execution was initiated from other station
Essentially, cannot initiate execution.
Do you want to initiate execution?

Yes<Y> No<N>

(3) Alert (2)

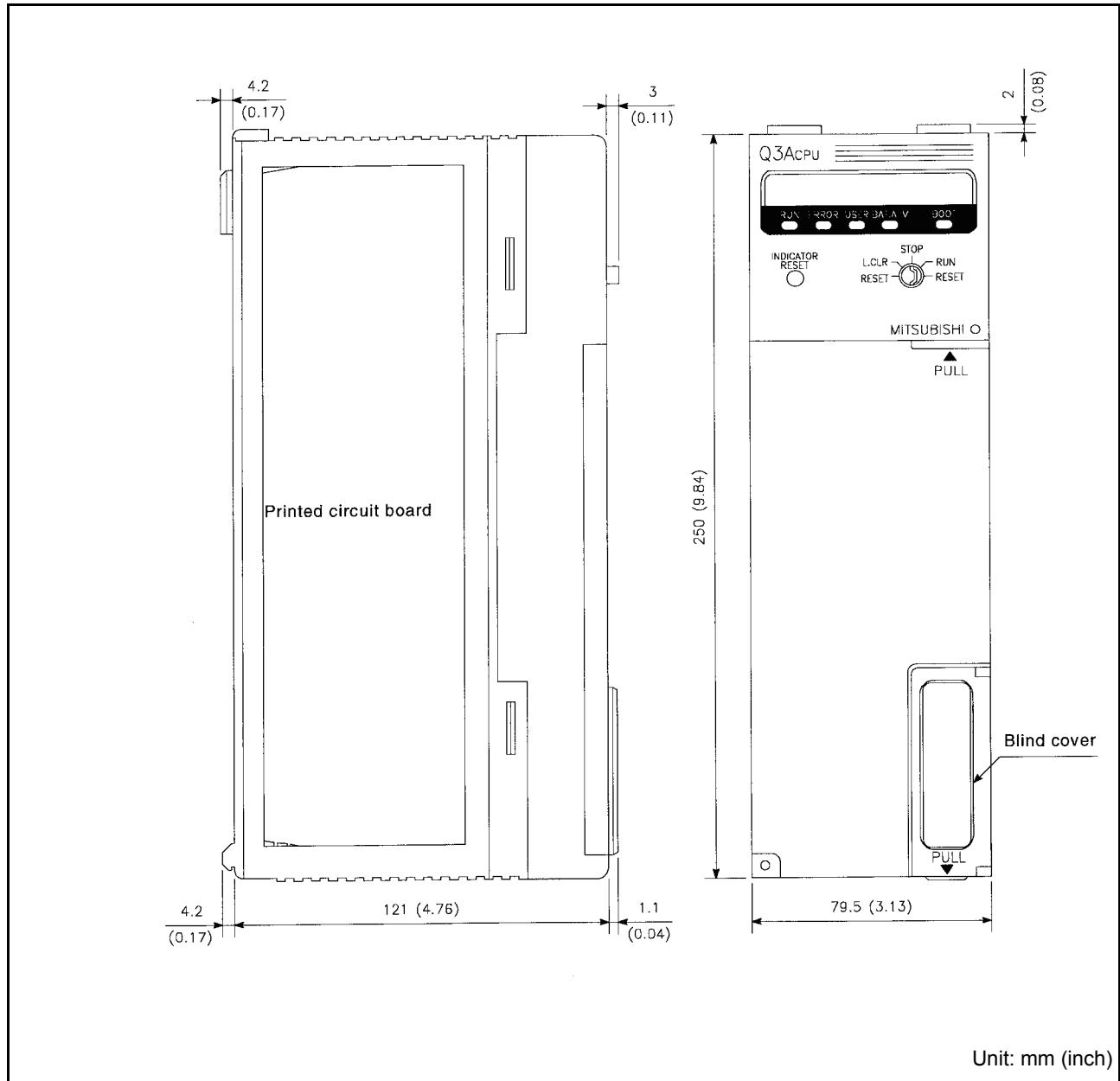
The file 'PARAM<Parameter>' already exists.
Do you want to overwrite it?

Yes<Y> No<N>

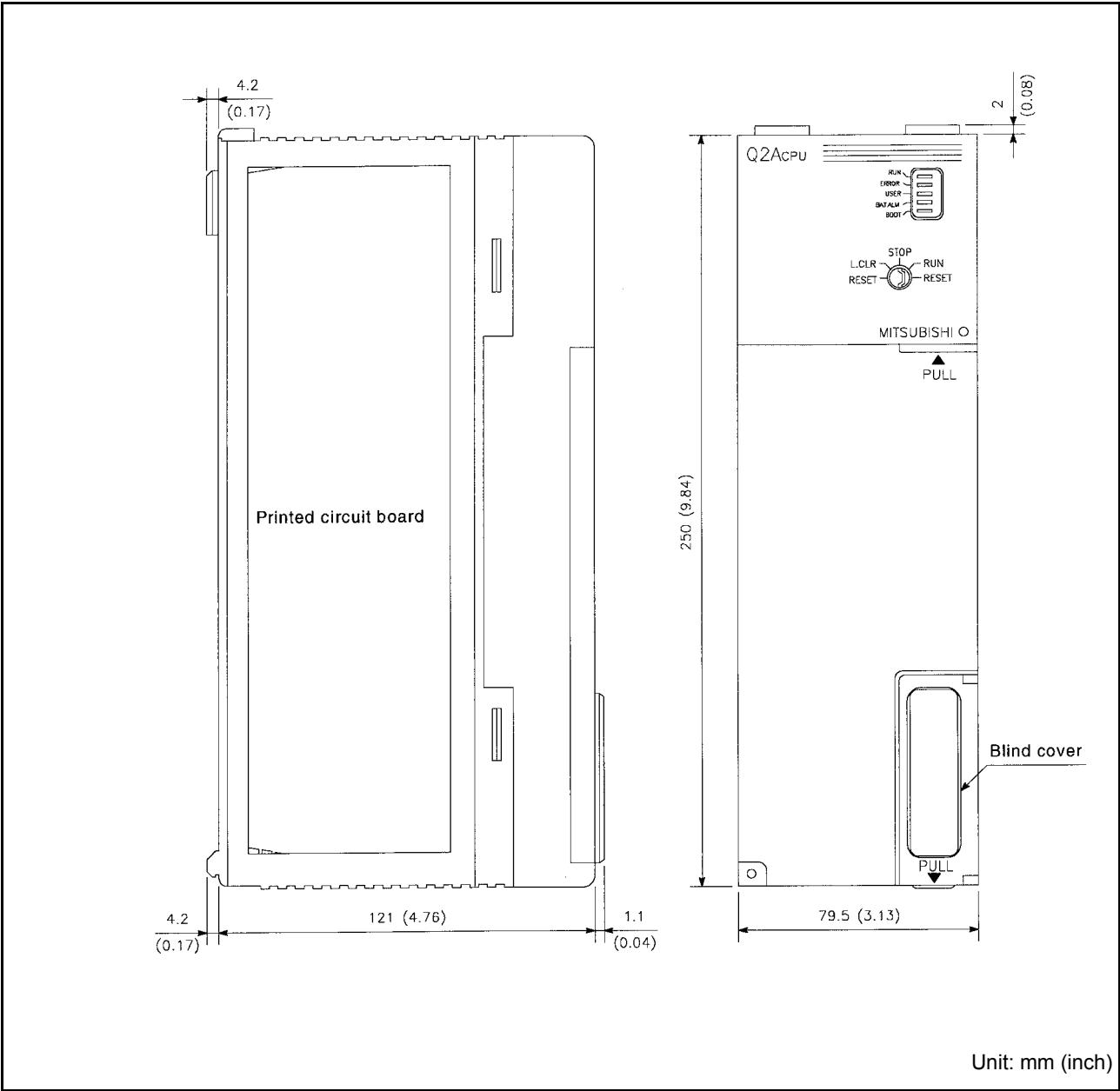
APPENDIX 6 EXTERNAL DIMENSIONS

Appendix 6.1 CPU Module

(1) Q3ACPU, Q4ACPU modules

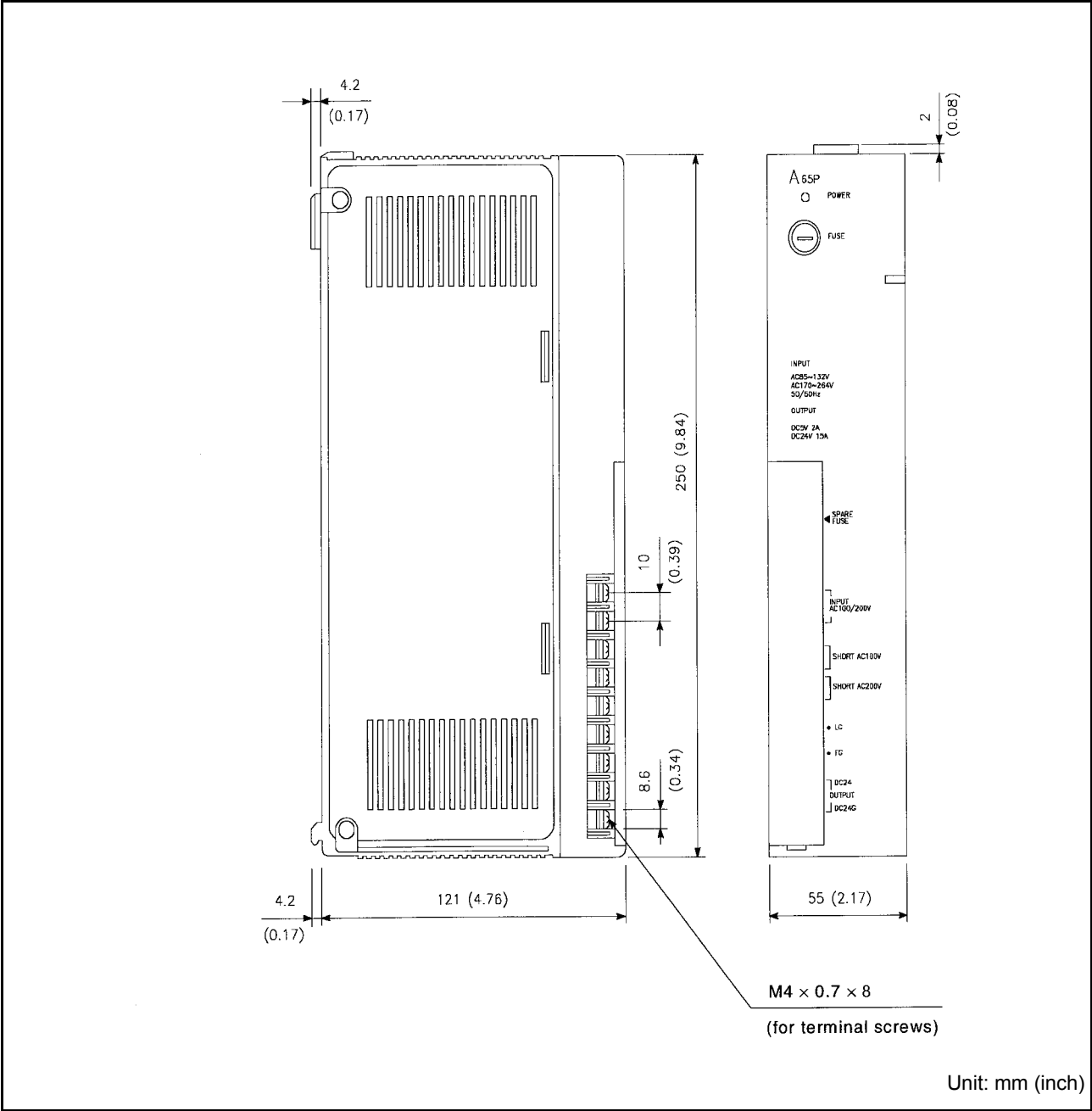


(2) Q2ACPU, Q2ACPU-S1 modules

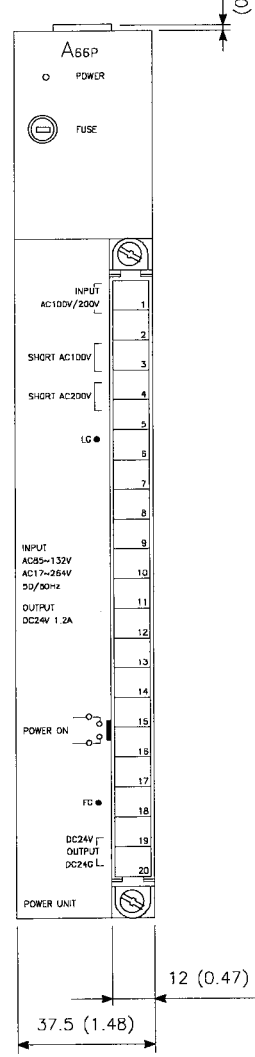


Appendix 6.2 Power Supply Module

(1) A61P, A61PN, A61PEU, A62P, A62PEU, A63P, A65P, A67P power supply modules

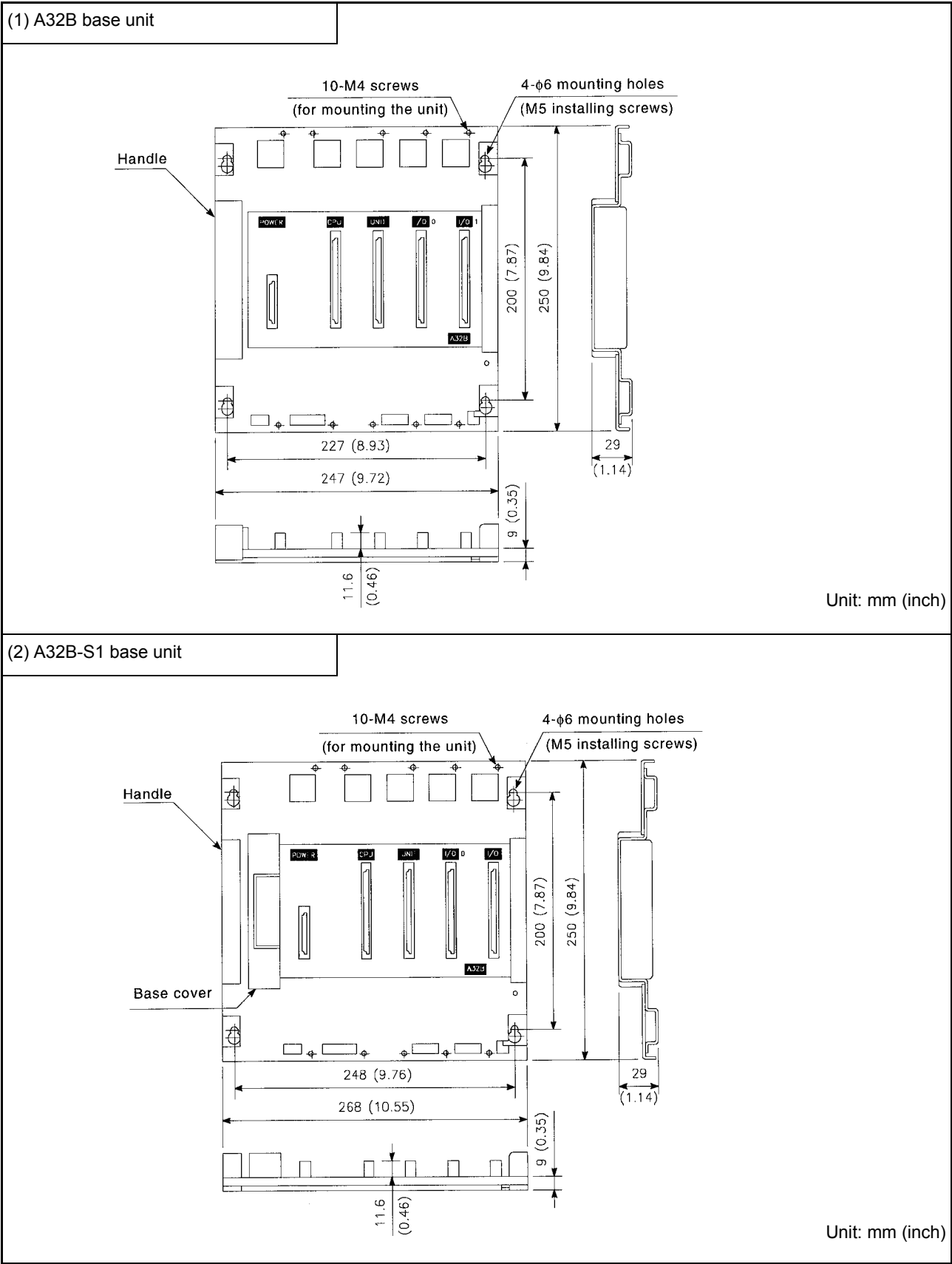


(2) A66P power supply module



Unit: mm (inch)

Appendix 6.3 Main Base Unit

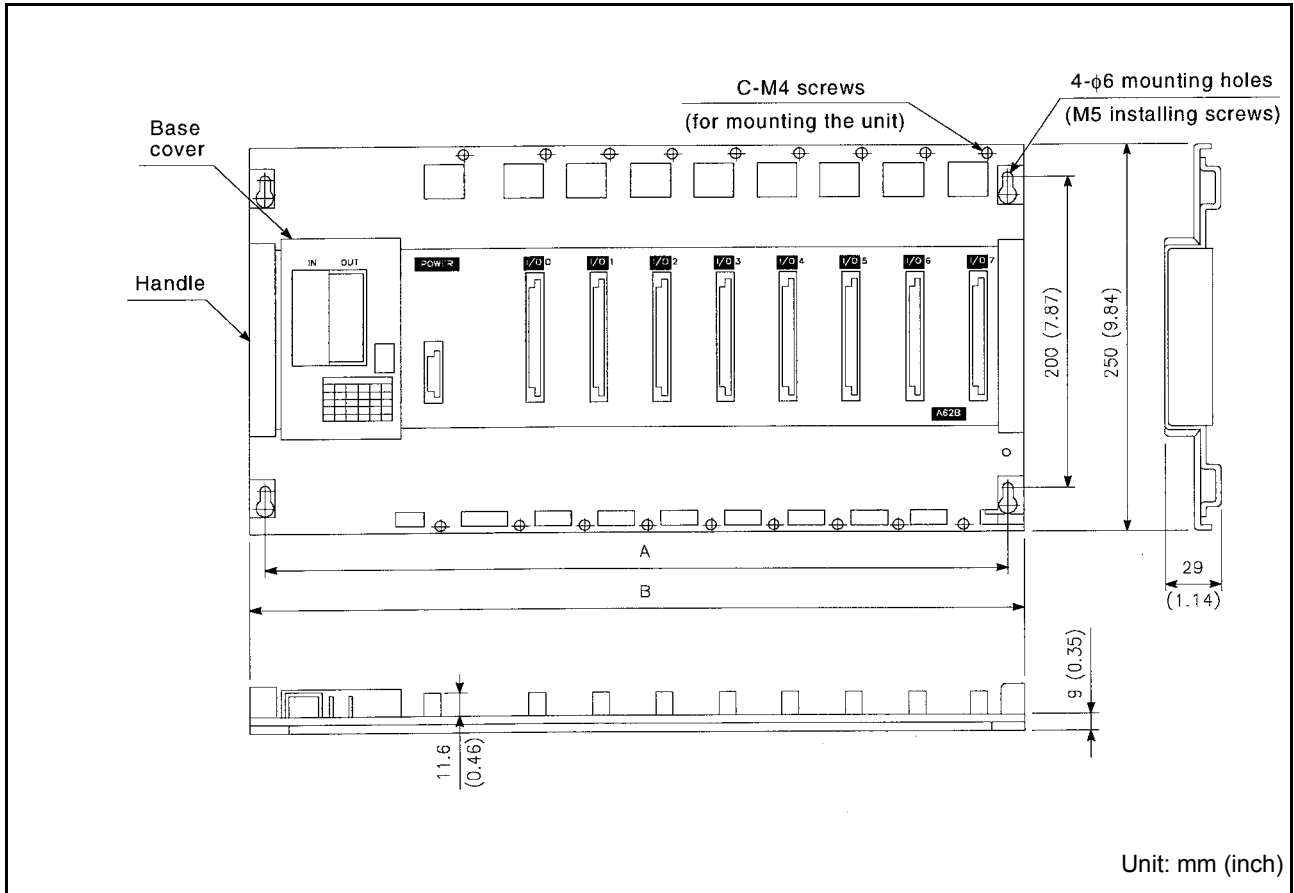


Unit: mm (inch)

Unit: mm (inch)

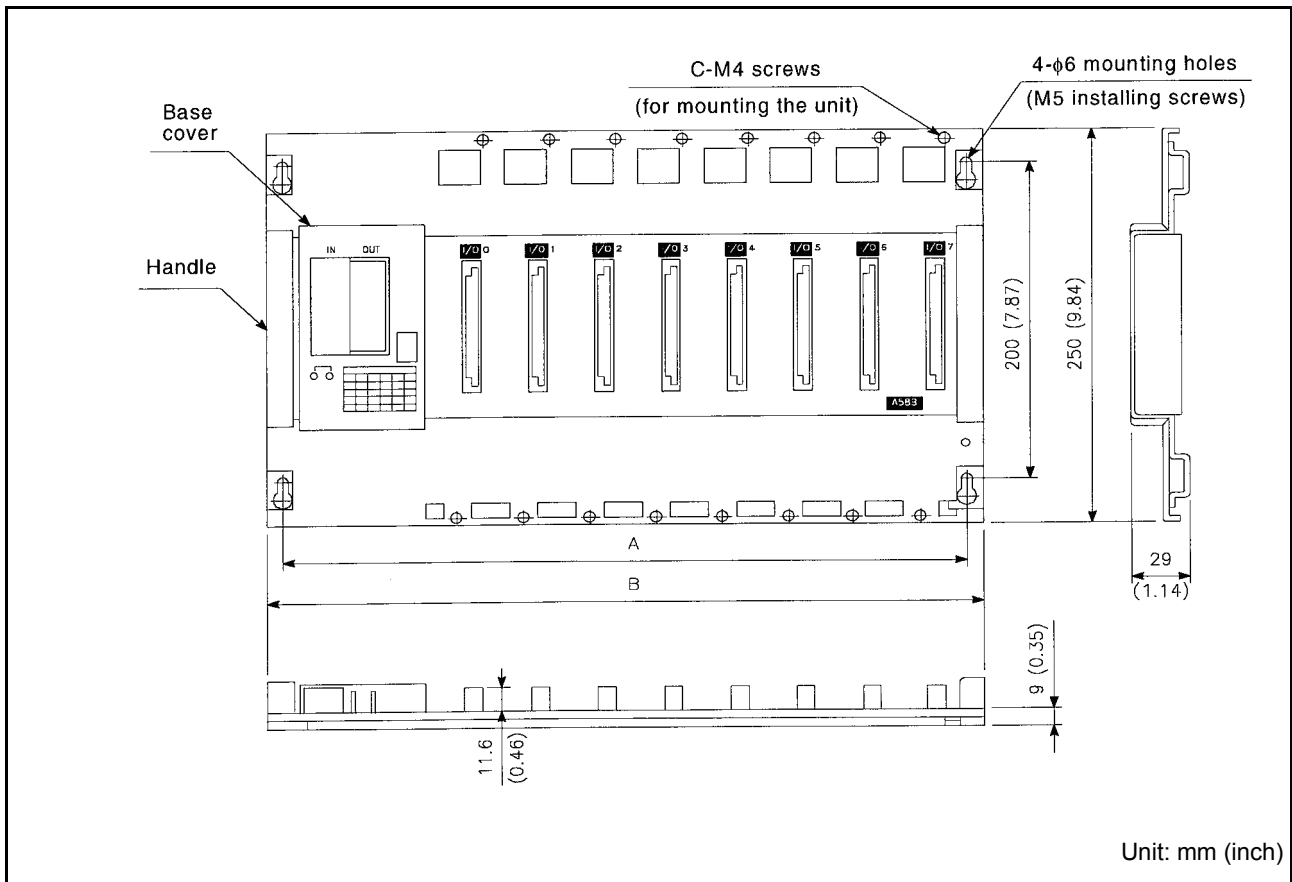
Appendix 6.4 Extension Base Unit

(1) A62B, A65B, A68B base units



Model Name	Variable Dimensions (mm) [inch]			Number of Slots
	A	B	C	
A62B	218 [8.58]	238 [9.37]	6 [0.24]	2 (slots 0, 1)
A65B	332 [13.07]	352 [13.86]	12 [0.47]	5 (slots 0 to 4)
A68B	446 [17.6]	466 [18.35]	18 [0.71]	8 (slots 0 to 7)

(2) A52B, A55B, A58B base units



Model Name	Variable Dimensions (mm) [inch]			Number of Slots
	A	B	C	
A52B	163 [6.42]	183 [7.2]	4 [0.16]	2 (slots 0, 1)
A55B	277 [10.9]	297 [11.69]	10 [0.39]	5 (slots 0 to 4)
A58B	391 [15.4]	411 [16.18]	16 [0.63]	8 (slots 0 to 7)

APPENDIX 7 USE OF LOCAL DEVICE FOR SUBROUTINE/INTERRUPT PROGRAM STORAGE FILE (FUNCTION VERSION B OR LATER)

When the subroutine/interrupt program is executed, the local device for the subroutine/interrupt program storage files can be used.

To use the local device in the storage destination file for the subroutine/interrupt program, set the special relays below:

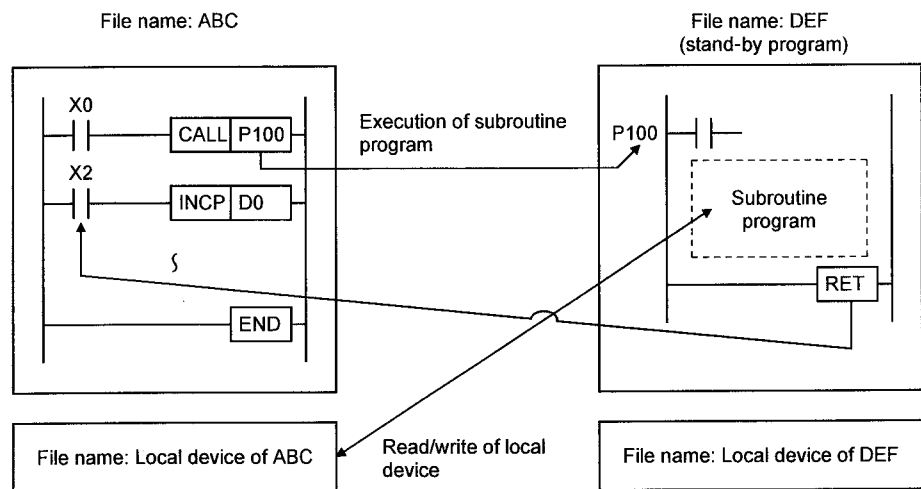
- Subroutine program : SM776
- Interrupt program : SM777

(1) Switching of local device with special relay ON/OFF

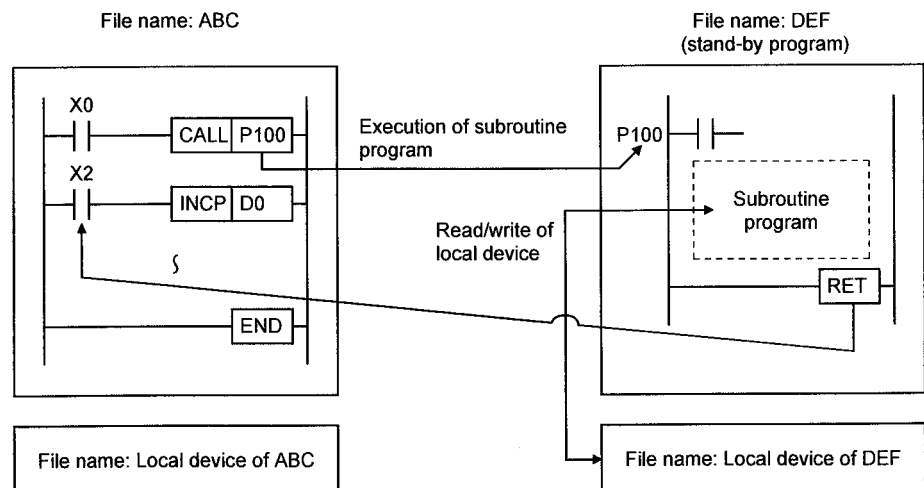
	SM776	SM777
OFF	Operation is performed at the local device of the call source file of the subroutine program.	Operation is performed at the local device of the file executed before execution of the interrupt program.
ON	Operation is performed at the local device of the file where the subroutine program is stored.	Operation is performed at the local device of the file where the interrupt program is stored.

(a) Operation for subroutine program

[SM776 operation: OFF without function version B or with function version B]

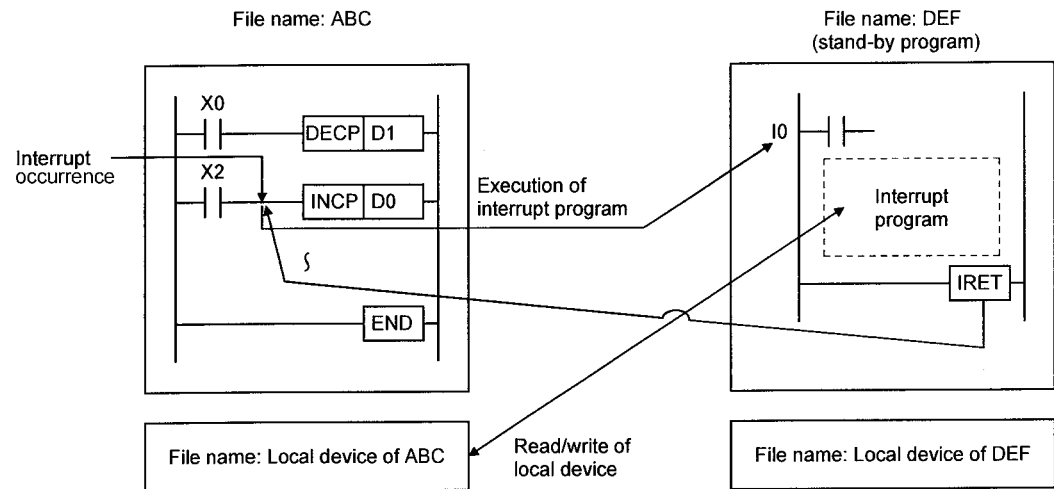


[SM776 operation: ON with function version B]

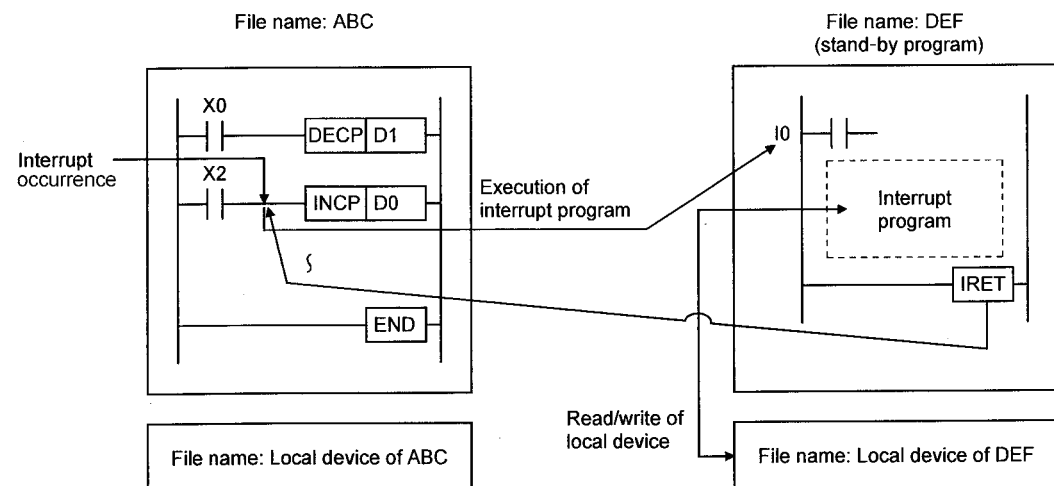


(b) Operation for interrupt program

[SM776 operation: OFF without function version B or with function version B]



[SM776 operation: ON with function version B]



(2) Precautions

- (a) When the SM776 is ON, the local device data can be read while the subroutine program is called. Furthermore, the data will be escaped after performing the RET instruction.

When the SM777 is ON, the local device data is read before performing the interrupt program. The data will be escaped after performing the IRET instruction.

Therefore, when SM776 and SM777 are ON, the scan time is extended by the time below after the subroutine program/interrupt program is executed once.

- Q2ACPU(S1) : $560 + 1.3 \times (\text{Number of words in the local device}) [\mu\text{s}]$
- Q3ACPU : $425 + 1.0 \times (\text{Number of words in the local device}) [\mu\text{s}]$
- Q4ACPU : $220 + 0.8 \times (\text{Number of words in the local device}) [\mu\text{s}]$

- (b) ON/OFF of SM776 and SM777 is set for each CPU module.

It cannot be set for each file.

- (c) When ON/OFF of SM776 and SM777 is changed during execution of the sequence program, the control is performed with the changed information.

APPENDIX 8 NETWORK RELAY FROM ETHERNET MODULE
(FUNCTION VERSION B OR LATER)

This is the network system that mixes Ethernet with MELSECNET/10. The network allows communicating data with the QnACPU in other station via many Ethernet or MELSECNET/10.

To perform the network relay from the Ethernet module, the Ethernet module with function version B or later is required.

- (1) Access range
- Table 8.1 shows the access range of the network relay from the computer/peripheral device with the system:

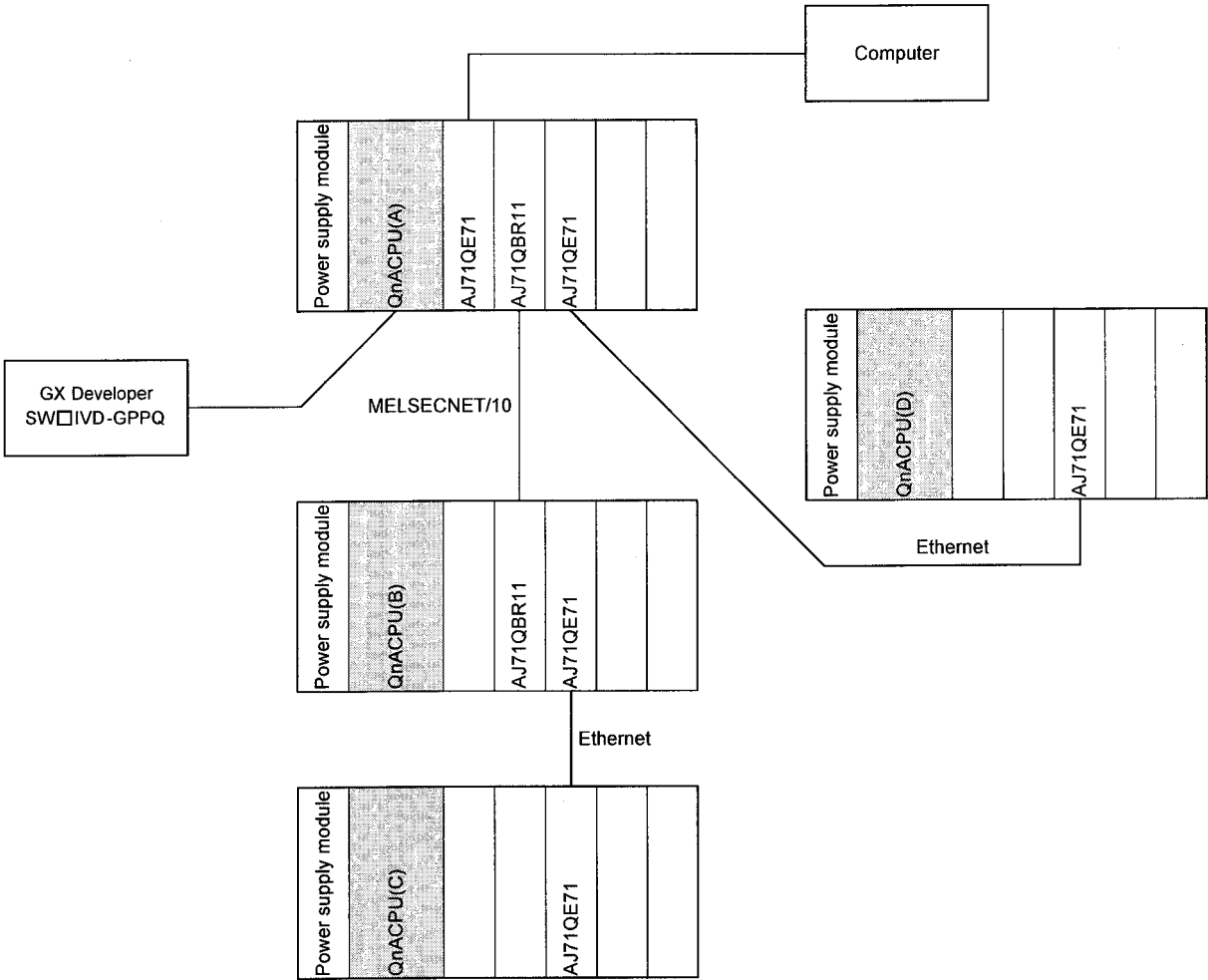


Table 8.1 Comparison table of access range from Ethernet module

Access to	Route	QnACPU "with" Function Version		QnACPU "without" Function Version	
		A	B	A	B
Host access	(Computer)→ QnACPU(A)	○	○	○	○
Other station access in host network (MELSECNET/10)	(Computer)→ QnACPU(B)	○	○	○	○
Other station access of other network (From MELSECNET/10 to Ethernet)	(Computer)→ QnACPU(C)	○	×	×	×
Other station access in host network (Ethernet)	(Computer)→ QnACPU(D)	○	×	×	×
Host access	(Peripheral device) → QnACPU(A)	○	○	○	○
Other station access in host network (MELSECNET/10)	(Peripheral device) → QnACPU(B)	○	○	○	○
Other station access of other network (From MELSECNET/10 to Ethernet)	(Peripheral device) → QnACPU(C)	○	×	×	×
Other station access in host network (Ethernet)	(Peripheral device) → QnACPU(D)	○	×	×	×

○ : Access allowed, × : Access not allowed

A : Ethernet module has indication of the function version.

B : Ethernet module does not have indication of the function version.

(2) Precautions

- (a) With combination of Ethernet module and MELSECNET/10, maximum 7 relays can be performed.
- (b) The following shows other station access with or without setting for other station access:
 - When other station access valid module is set, the set module is used for relay.
 - When other station access valid module is not set, the relay is as follows:
When MELSECNET/10 is available: 1st of MELSECNET/10 is relayed.
When MELSECNET/10 is not available: 1st of Ethernet is relayed.
- (c) When parameters are not registered in the Ethernet module, the QnACPU stores the default parameters in all AJ71QE71.
When multiple Ethernet modules are installed, settings are made in the order of 1st station and 2nd station and so on counting from the QnACPU side.

- (d) Table 8.2 shows operation of the QnACPU for online/offline of the Ethernet module.

Table 8.2 Operation of QnACPU for online/offline of Ethernet module

Ethernet Parameter	Ethernet Module Status	QnACPU Operation
With	Online	Communication with external device is performed with the specified parameter.
	Offline	The QnACPU does not show an error, but communication with external device is not performed.
Without	Online	Communication with external device is performed with the default parameter.
	Offline	The QnACPU does not show an error, but communication with external device is not performed.

- (e) Set the Ethernet module and MELSECNET/10 not to overlap their Network No.s each other. Same network No. cannot be set for them.
The following shows the number of the Ethernet modules and the MELSECNET(/10, /II) modules that can be mounted on one QnACPU:
- (Ethernet module) ≤ 4
 - [(MELSECNET/10) + (MELSECNET/II)] ≤ 4
- (f) When the Ethernet parameters are set for the Ethernet module without function version B, error code "3103" (No Ethernet module in the I/O number set with the parameter) appears and the system stops due to an error.

APPENDIX 9 QnACPU PROCESSING TIME

QnACPU processing time is explained below.

Appendix 9.1 Overview of QnACPU Scan Time

The QnACPU scan time comes to the total of the following values.

- I/O refresh processing
- Total values of instruction execution time
- END processing

(1) I/O refresh time

(a) I/O data refresh time between the following modules, which is mounted in the QnACPU main base unit and extension base unit, and CPU modules

- Input module
- Output module
- Special function module

(b) I/O refresh time can be calculated in the following formula.

$$(\text{I/O refresh time}) = (\text{I/O points} \div 16) \times N1 + (\text{Output points} \div 16) \times N2$$

For N1 and N2, refer to the following table.

CPU Module	N1	N2
Q2ACPU(S1)	5.2 μ s	5.0 μ s
Q3ACPU	4.8 μ s	4.7 μ s
Q4ACPU	4.4 μ s	4.3 μ s

(2) Instruction execution time

(a) Processing time of each instruction used for QnACPU program

For the processing time of each instruction, refer to the following manual.

- QCPU (Q mode)/QnACPU Programming Manual (Common Instructions)

(b) Since interrupt/fixed-cycle execution type program have overhead time, add the overhead time to the instruction execution time.

(3) END processing

(a) QnACPU common processing time except for above (1), (2)

(b) The following table shows values of the END processing time.

	CPU Module	END Proc Time
With error check (SM1084 = OFF)	Q2ACPU	1.7ms
	Q3ACPU	1.3ms
	Q4ACPU	0.7ms
Without error check (SM1084 = ON)	Q2ACPU	1.2ms
	Q3ACPU	0.9ms
	Q4ACPU	0.5ms

Appendix 9.2 Causes of Increasing Scan Time

The following shows the functions that increase the QnACPU scantime.

When using the following functions, add the values calculated in Appendix 9.1 to the following values.

- MELSECNET/10 refresh
 - MELSECNET/MINI-S3 refresh
 - CC-Link auto refresh
 - Sampling trace
 - Monitor using GX Developer
 - Local device
 - Multiple program execution
 - Installation/removal of memory card
 - File register whose file name is the same as the program
- (1) MELSECNET/10 refresh
Refresh time between QnACPU and MELSECNET/10 network module
For MELSECNET/10 refresh time, refer to the following manual.
 - QnA/Q4AR MELSECNET/10 Network System Reference Manual
 - (2) MELSECNET/MINI-S3 refresh
Refresh time between QnACPU and MELSECNET/MINI (S3) network module
For MELSECNET/MINI (S3) refresh time, refer to the following manual.
 - MELSECNET/MINI-S3 Master Module User's Manual
 - (3) CC-Link auto refresh
Refresh time between QnACPU and CC-Link master local module
For the auto refresh processing time of CC-Link, refer to the following manual.
 - Control & Communication Link System Master/Local Module type AJ61QBT11/A1SJ61QBT11 User's Manual
 - (4) Sampling trace
 - (a) Processing time in the case of sampling trace execution
Sampling trace data are set using GX Developer, and the processing time is added when the sampling trace is executed.
 - (b) The following table shows the processing time when internal relay 50 points as a bit device, data register 50 points as a word device are set for sampling trace data.

CPU Module	Processing time
Q2ACPU(S1)	3.2ms
Q3ACPU	2.4ms
Q4ACPU	1.2ms

(5) Monitor using GX Developer

Processing time in the case of monitoring by GX Developer

The processing time is added when monitoring by GX Developer.

(a) The following table shows the processing time when data register 64 points are set for registration monitor:

CPU Module	Processing Time
Q2ACPU(S1)	0.46ms
Q3ACPU	0.35ms
Q4ACPU	0.18ms

(b) The following shows the processing time when monitor conditions are set.

CPU Module	Processing Time	
	Agreement in Designated Step	Agreement in Designated Device
Q2ACPU(S1)	0.38ms	0.38ms
Q3ACPU	0.29ms	0.29ms
Q4ACPU	0.15ms	0.15ms

(6) Local device

Processing time when the local device is used

The processing time is added when the local device is used.

CPU Module	Processing Time
Q2ACPU(S1)	$3.0 \times (n - 1) + 2.8\text{ms}$
Q3ACPU	$2.2 \times (n - 1) + 2.1\text{ms}$
Q4ACPU	$1.1 \times (n - 1) + 1.1\text{ms}$

Condition: local device setting: 1 k point, n: number of program files

(7) Multiple program execution

Overhead time when executing each program that executes several programs in the QnACPU. The processing time is added when several programs are executed..

CPU Module	Processing Time
Q2ACPU(S1)	$0.21 \times n\text{ms}$
Q3ACPU	$0.16 \times n\text{ms}$
Q4ACPU	$0.08 \times n\text{ms}$

Condition: n: number of program files

(8) File register

Processing time when the file register is used

The processing time is added when the file register is used.

CPU Module	Processing Time
Q2ACPU(S1)	$0.87 \times (n - 1) + 0.74\text{ms}$
Q3ACPU	$0.64 \times (n - 1) + 0.60\text{ms}$
Q4ACPU	$0.32 \times (n - 1) + 0.28\text{ms}$

Condition: n:number of program files

APPENDIX 10 TRANSPORTATION PRECAUTIONS

When transporting lithium batteries, make sure to treat them based on the transportation regulations.

Appendix 10.1 Relevant Models

The batteries used for QnACPU are classified as shown in the table below:

Product Name	Model Name	Description	Handled as
QnA series battery	A6BAT	Lithium battery alone	Non-dangerous goods
QnA series memory card	Q1MEM-128S, Q1MEM-128SE, Q1MEM-1MS, Q1MEM-1MSE, Q1MEM-256S, Q1MEM-256SE, Q1MEM-2MS, Q1MEM-512S, Q1MEM-512SE, Q1MEM-64S, Q1MEM-64SE	Packed with lithium coin battery (BR2325)	

Appendix 10.2 Transportation Guidelines

Products are packed properly in compliance with the transportation regulations prior to shipment. When repacking any of the unpacked products to transport it to another location, make sure to observe the IATA Dangerous Goods Regulations, IMDG Code and other local transportation regulations.

For details, please consult your transportation company.

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WARRANTY

Please confirm the following product warranty details before using this product.

1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "Failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be repaired at no cost via the sales representative or Mitsubishi Service Company. However, if repairs are required onsite at domestic or overseas location, expenses to send an engineer will be solely at the customer's discretion. Mitsubishi shall not be held responsible for any re-commissioning, maintenance, or testing on-site that involves replacement of the failed module.

[Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place.

Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months. The gratis warranty term of repair parts shall not exceed the gratis warranty term before repairs.

[Gratis Warranty Range]

- (1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautions, etc., given in the instruction manual, user's manual and caution labels on the product.
- (2) Even within the gratis warranty term, repairs shall be charged for in the following cases.
 1. Failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
 2. Failure caused by unapproved modifications, etc., to the product by the user.
 3. When the Mitsubishi product is assembled into a user's device, Failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
 4. Failure that could have been avoided if consumable parts (battery, backlight, fuse, etc.) designated in the instruction manual had been correctly serviced or replaced.
 5. Failure caused by external irresistible forces such as fires or abnormal voltages, and Failure caused by force majeure such as earthquakes, lightning, wind and water damage.
 6. Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
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- (1) Mitsubishi shall accept onerous product repairs for seven (7) years after production of the product is discontinued. Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.
- (2) Product supply (including repair parts) is not available after production is discontinued.

3. Overseas service

Overseas, repairs shall be accepted by Mitsubishi's local overseas FA Center. Note that the repair conditions at each FA Center may differ.

4. Exclusion of loss in opportunity and secondary loss from warranty liability

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5. Changes in product specifications

The specifications given in the catalogs, manuals or technical documents are subject to change without prior notice.

6. Product application

- (1) In using the Mitsubishi MELSEC programmable logic controller, the usage conditions shall be that the application will not lead to a major accident even if any problem or fault should occur in the programmable logic controller device, and that backup and fail-safe functions are systematically provided outside of the device for any problem or fault.
- (2) The Mitsubishi programmable logic controller has been designed and manufactured for applications in general industries, etc. Thus, applications in which the public could be affected such as in nuclear power plants and other power plants operated by respective power companies, and applications in which a special quality assurance system is required, such as for Railway companies or Public service purposes shall be excluded from the programmable logic controller applications. In addition, applications in which human life or property that could be greatly affected, such as in aircraft, medical applications, incineration and fuel devices, manned transportation, equipment for recreation and amusement, and safety devices, shall also be excluded from the programmable logic controller range of applications. However, in certain cases, some applications may be possible, providing the user consults their local Mitsubishi representative outlining the special requirements of the project, and providing that all parties concerned agree to the special circumstances, solely at the users discretion.

Q2ACPU(S1)/Q3ACPU/Q4ACPU

User's Manual

MODEL	QNACPU-U-E
MODEL CODE	13J821
IB(NA)-66608-D(0705)MEE	



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